FAIRCHILD
A Schlumberger Company

F100107
Quint Exclusive OR/NOR Gate

F100K ECL Product

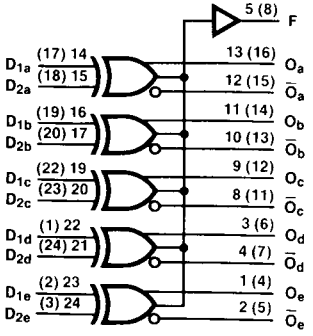
Description

The F100107 is a monolithic quint exclusive-OR/NOR gate. The Function output is the wire-OR of all five exclusive-OR outputs: $F = (D_{1a} \oplus D_{2a}) + (D_{1b} \oplus D_{2b}) + (D_{1c} \oplus D_{2c}) + (D_{1d} \oplus D_{2d}) + (D_{1e} \oplus D_{2e})$.

Pin Names

D_{na} - D_{ne}	Data Inputs
F	Function Input
O_a - O_e	Data Outputs
$\overline{O}_a$ - $\overline{O}_e$	Complementary Data Outputs

Logic Symbol



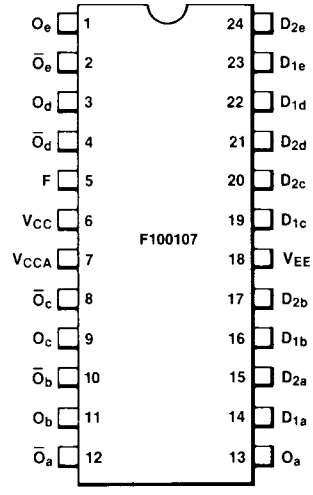
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information

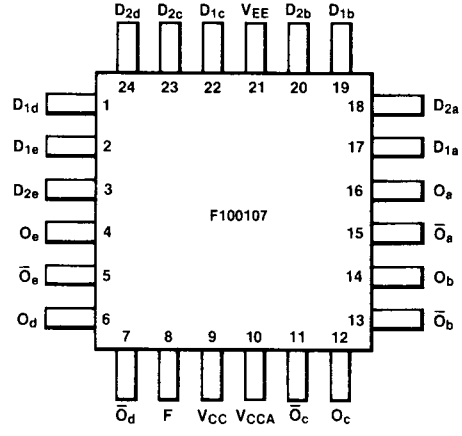
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Connection Diagrams

24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current D_{2a} - D_{2e} D_{1a} - D_{1e}			 250 350	 μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−96	−66	−46	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

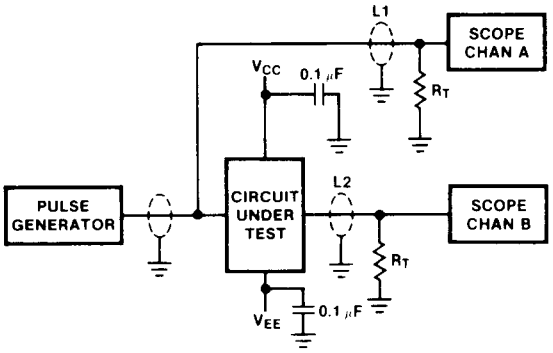
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay D_{2a}-D_{2e} to O, $\overline{O}$	0.55	1.90	0.55	1.80	0.55	1.90	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay D_{1a}-D_{1e} to O, $\overline{O}$	0.55	1.70	0.55	1.60	0.55	1.70	ns	
t_{PLH} t_{PHL}	Propagation Delay Data to F	1.15	2.75	1.15	2.75	1.15	3.00	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.65	0.45	1.80	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay D_{2a}-D_{2e} to O, $\overline{O}$	0.55	1.70	0.55	1.60	0.55	1.70	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay D_{1a}-D_{1e} to O, $\overline{O}$	0.55	1.50	0.55	1.40	0.55	1.50	ns	
t_{PLH} t_{PHL}	Propagation Delay Data to F	1.15	2.55	1.15	2.55	1.15	2.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.55	0.45	1.70	ns	

*See Family Characteristics for other dc specifications.

Fig. 1 AC Test Circuit



Notes

V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Fig. 2 Propagation Delay and Transition Times