Dual operational amplifier with switch, for audio use (3 inputs × 1 output × 2)
BA3131FS

The BA3131FS contains two built-in circuits with operational amplifiers configured of three differential input circuits, an output circuit, and a switch circuit. The three differential input circuits are separate, enabling independent settings to be entered for the gain and frequency characteristics.

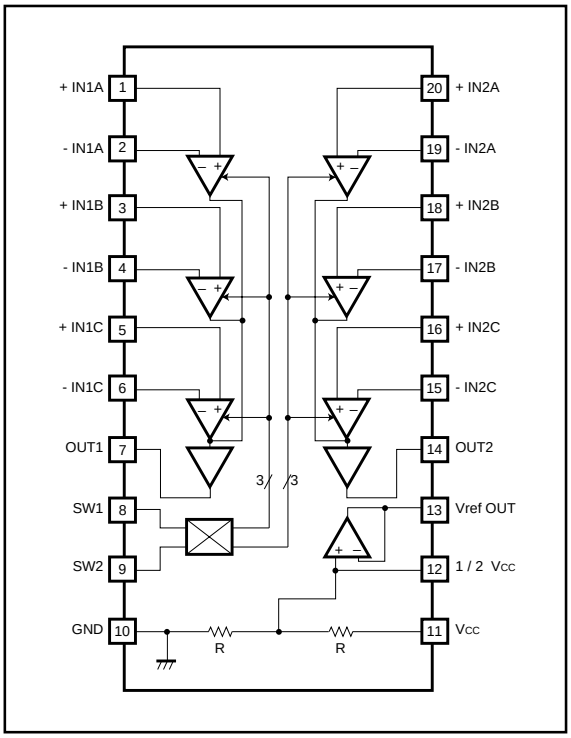
●Applications

Car stereos, audio amplifiers and other electronic circuits

●Features

1) High gain and low distortion. (Gv = 110dB, THD = 0.0015% typ.)
2) Low noise. (Vn = 2μVrms typ.)
3) Switching circuit can be directly coupled to microcomputer port.
4) Small switching noise.
5) Equipped with 1 / 2 Vcc output circuit for single power supply.

●Block diagram



●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	18.0	V
Power dissipation	Pd	750*	mW
Operating temperature	Topr	– 40 ~ + 85	˚C
Storage temperature	Tstg	– 55 ~ + 125	˚C
Common-mode input voltage	Vi	3 ~ V_{CC}	V
Differential input voltage	Vid	V_{CC}	V
Load current	$I_{OMax.}$	± 50.0	mA

* Reduced by 7.5mW for each increase in Ta of 1˚C over 25˚C.
(When mounted on a glass epoxy board (90mm × 50mm × 1.6t))

●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating power supply voltage	V_{CC}	6.0	8.0	16.0	V	single power source

●Electrical characteristics (unless otherwise noted, Ta=25°C, Vcc=8V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement circuit
Quiescent current	Iq	2.0	4.9	7.8	mA	V_{IN} = 0, RL = ∞ , SW pin open	Fig.2
Input offset voltage	Vio	-	0.5	5.0	mV	RS ≤ 10kΩ	Fig.1
Input offset current	Iio	-	5	200	nA		Fig.1
Input bias current	Ib	-	50	500	nA	*1	Fig.1
High-amplitude voltage gain	Avol	86	110	-	dB	RL ≥ 2kΩ, V_O = ± 1.5V	Fig.1
Common-mode input voltage	Vicm	3	6	-	V		Fig.1
In-phase signal rejection ratio	CMRR	60	72	-	dB	RS ≤ 10kΩ	Fig.1
Power supply voltage rejection ratio	PSRR	76	90	-	dB	RS ≤ 10kΩ	Fig.1
Maximum output voltage	V_{OH}	3	6	-	V	RL ≥ 10kΩ	Fig.3 / Fig.4
	V_{OL}	3	6	-	V	RL ≥ 2kΩ	
Input conversion noise voltage	Vn	-	2.0	4.0	μVrms	*2	Fig.7
Reference voltage change	ΔV_{REF}	-	-	± 10	mV	Ioref = ± 1mA	-

*1 Because the first stage is contigured with PNP transistors, input bias current is from the IC.

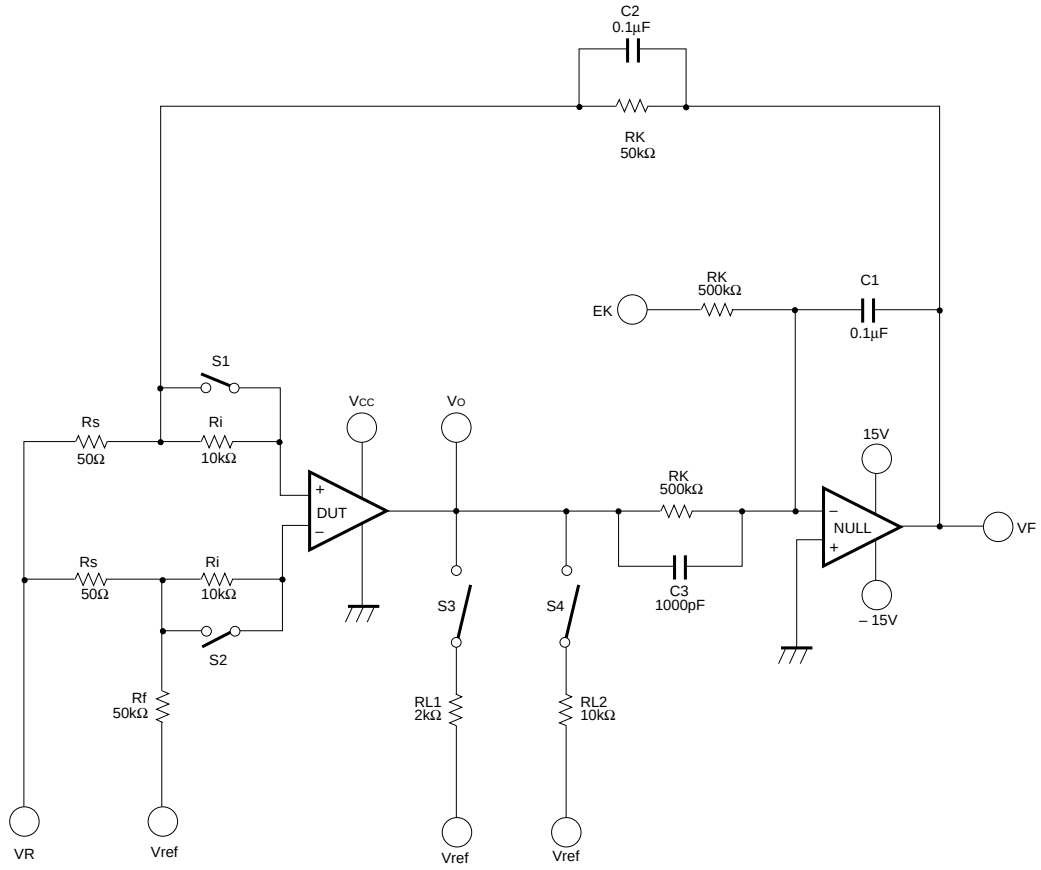
*2 Tested under the following conditions: G_V = 40dB, RS = 2kΩ, Matsushita Tsuko VP-9690A (using DIN audio filter)

●Design guaranteed values (unless otherwise noted, Ta=25°C, Vcc=8V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement circuit
Slew rate	SR	0.5	1.2	-	V / μS	G_V = 0dB, RL = 2kΩ	Fig.5
Gainbandwidth product	GBW	1.5	2.6	-	MHz	f = 10kHz	Fig.6
Crosstalk between A, B and C	CT_{ABC}	60	73	-	dB	f = 1kHz	Fig.8
Total harmonic distortion	THD	-	0.0025	0.01	%	G_V = 0dB, f = 1kHz, V_O = 1Vrms	Fig.9
Channel separation	CS	90	115	-	dB	f = 1kHz, input conversion	Fig.10

* This item is not guaranteed during processes.

●**Measurement circuit**



∗ C2 and C3 are used to prevent oscillation (adjustment required)

Fig.1

●**Measurement conditions** (Figure 1)

Measurement Item	V_{CC}	VR	EK	VF	S1	S2	S3	S4	Equation
Input offset voltage	8	Vref	—	VF1	ON	ON	OFF	OFF	1
Input offset current	8	Vref	—	VF2	OFF	OFF	OFF	OFF	2
Input bias current	8	Vref	—	VF3	OFF	ON	OFF	OFF	3
				VF4	ON	OFF			
High-amplitude voltage gain	8	Vref	5.5	VF5	ON	ON	ON	OFF	4
			2.5	VF6					
Common-mode signal rejection ratio (Common-mode input voltage)	8	6	8	VF7	ON	ON	OFF	OFF	5
	8	2	0	VF8					
Power supply voltage rejection ratio	6	Vref	—	VF9	ON	ON	OFF	OFF	6
	18	Vref	—	VF10					

●**Equations**

(1) Input offset voltage (Vio)

$Vio = | VF1 | / (1 + Rf / Rs)$

(2) Input offset current (Iio)

$Iio = | VF2 - VF1 | / (Ri (1 + Rf / Rs))$

(3) Input bias current (Ib)

$Ib = | VF4 - VF3 | / (2 Ri (1 + Rf / Rs))$

(4) High-amplitude voltage gain (Avol)

$Avol = 20\log (3 (1 + Rf / Rs) / | VF6 - VF5 |)$ (dB)

(5) In-phase signal rejection ratio (CMRR)

$CMRR = 20\log (4 (1 + Rf / Rs) / | VF8 - VF7 |)$ (dB)

(6) (In-phase input voltage range) (PSRR)

$PSRR = 20\log (12 (1 + Rf / Rs) / | VF10 - VF9 |)$ (dB)

●Measurement circuits

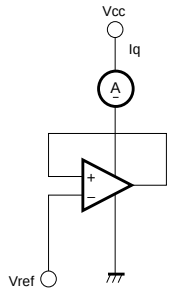


Fig.2 Iq

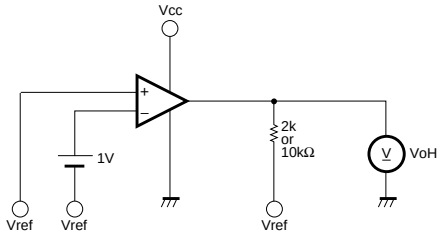


Fig. 3 Maximum output voltage: High

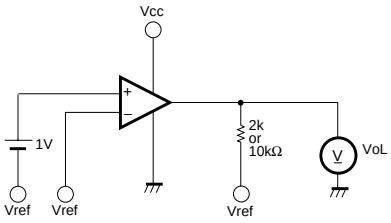


Fig. 4 Maximum output voltage: Low

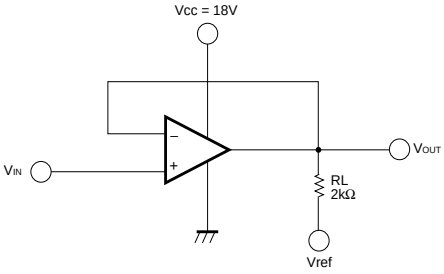


Fig. 5 Slew rate (Ⅰ)

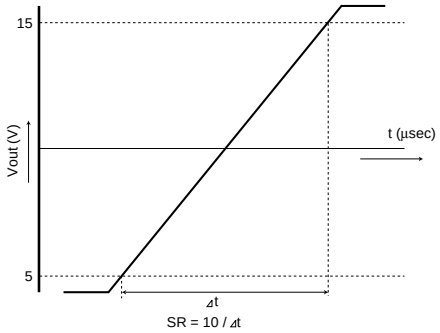


Fig. 6 Slew rate (Ⅱ)

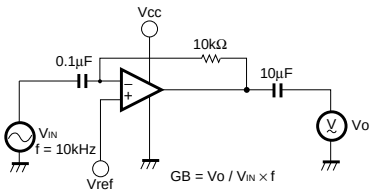


Fig. 7 Band width frequency gain

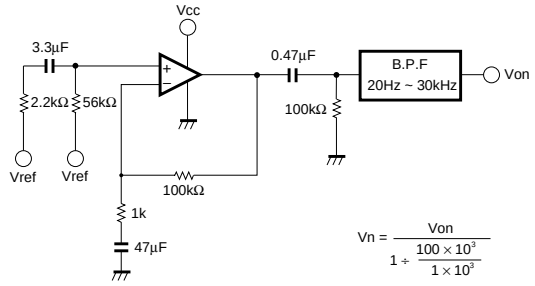


Fig. 8 Input conversion noise voltage

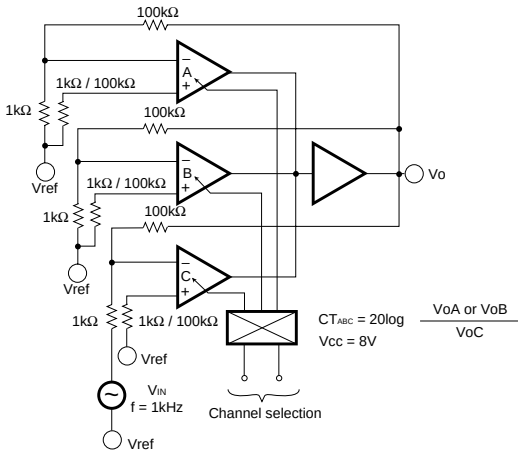


Fig. 9 Crosstalk between A and B

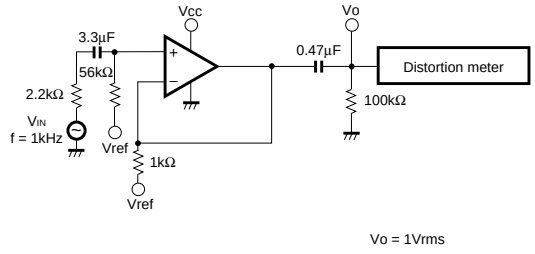


Fig. 10 Total harmonic distortion

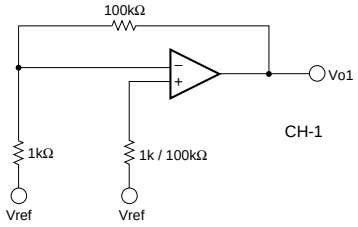


Fig. 11 Channel separation (Ⅰ)

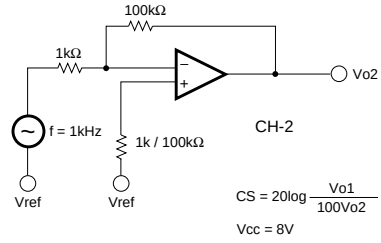


Fig. 12 Channel separation (Ⅱ)

●**Application example**

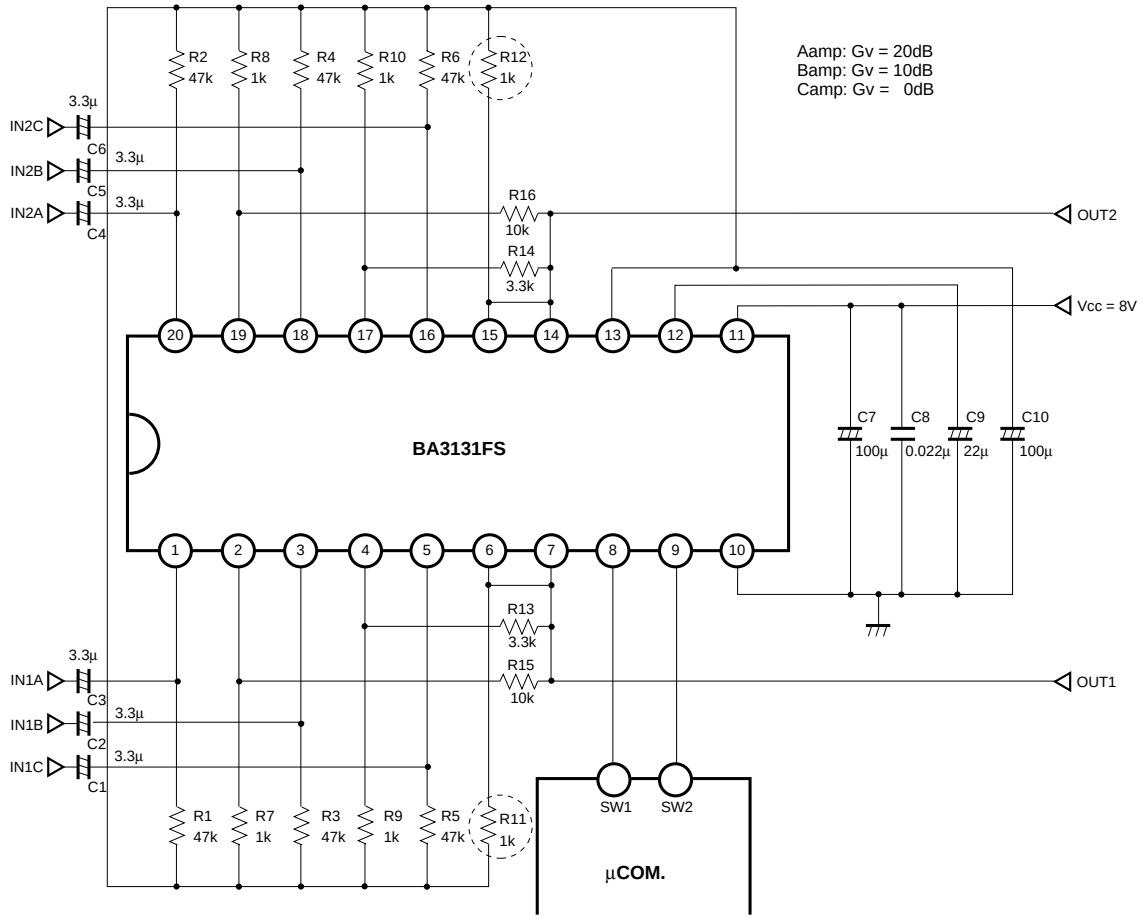


Fig.13

●Operation notes

(1) Pin 13 is the reference output pin, from which 1 / 2 Vcc is output. The value for the bypass capacitor should be determined based on the desired characteristics. A value between 500pF and 1μF may produce oscillation, so if AC grounding is being used, always use a bypass capacitor with a value of at least 10μF.
Also, Pin 12 is designated for reference circuit input, so if reference output is being used, always use a bypass capacitor for AC grounding. (We recommend a bypass capacitor with a value of 22μF.)

•Reference data (these values are intended only as a reference, and performance is not guaranteed)

Pin 12 bypass capacitor (μF)	Ripple rejection ratio (f_{IN} = 100 Hz) (dB)	Output rise time (ms)*
10	– 35	150
22	– 42	300
47	– 48	550

* Test conditions: When power supply is on (V_{CC} = 8V), time equal to 90% of V_{CC} bypass capacitor,Pin 13 bypass capacitor 100μF, output smoothing voltage.

(2) This IC offers stability even at low gain (0 to 20dB), but a capacitance load of 200pF or higher may cause oscillation (the phase margin at a capacitance of 200pF is 10° typ. (Ta = 85°C, 0dB point)). Consequently, please make sure sufficient care is taken in terms of the capacitance load.
When using a 0dB buffer, as shown in the application example (Figure 13), introducing a bias resistance of several kΩ to the negative input (R11 and R12 in Figure 13, indicated as circled items) results in greater stability in terms of the capacitance load.

●Truth value table

	ch1	ch2	ch3	OFF	Conditions
SW1 (8pin)	H	H	L	L	Corresponds to μCOM output
SW2 (9pin)	H	L	H	L	

* “H” when the applied voltage at pins 8 and 9 is 2.0V or more, and “L” when it is 1.0V or less.

●Electrical characteristic curves

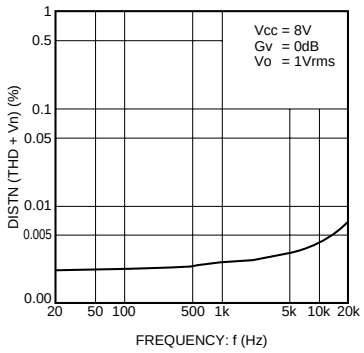


Fig. 14 Distortion vs. frequency

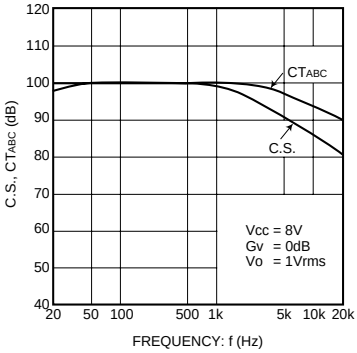


Fig. 15 Channel separation and crosstalk vs. frequency

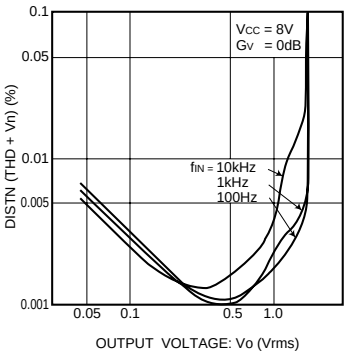


Fig. 16 Distortion vs. output voltage

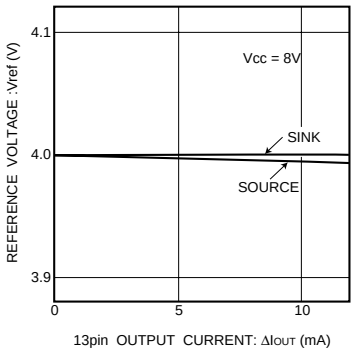
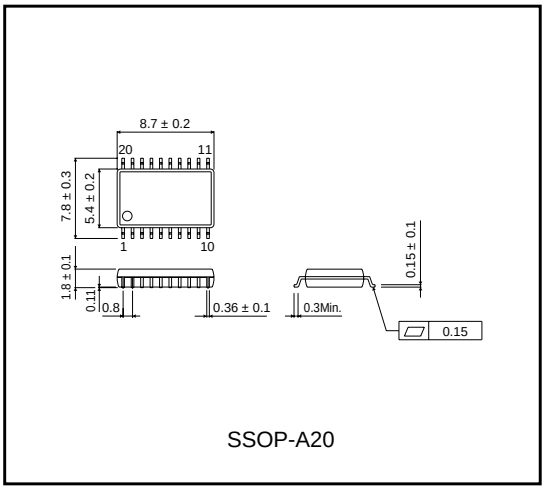


Fig. 17 Reference voltage vs. pin 13 output current

●External dimensions (Units: mm)



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