

Oki, Network Solutions for a Global Society

FEDR27T12800J-02-07

Issue Date: Jul. 9, 2004

OKI Semiconductor MR27T12800J

8M-Word × 16-Bit or 16M-Word × 8-Bit P2ROM

FEATURES

 \cdot 8,388,608-word × 16-bit/16,777,216-word × 8-bit electrically switchable configuration

\cdot Access time

· MR27T12800J-xxxTN, MR27T12	2800J-xxxTY
\cdot 2.7 V to 3.6 V power supply	90 ns MAX
· MR27T12800J-xxxTNE, MR27T	12800J-xxxTYE
\cdot 2.7 V to 3.0 V power supply	120 ns MAX
\cdot 3.0 V to 3.6 V power supply	100 ns MAX

· Operating current

25 mA MAX(5MHz)

- \cdot Standby current 10 μ A MAX
- \cdot Input/Output TTL compatible
- \cdot Three-state output

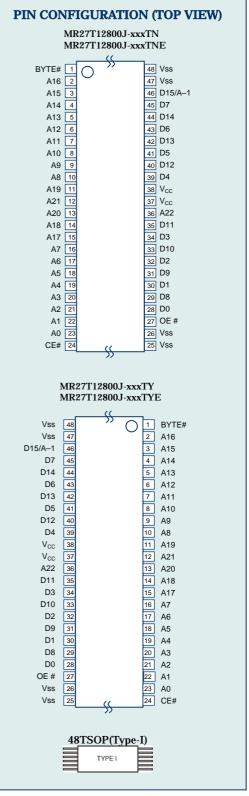
PACKAGES

- · MR27T12800J-xxxTN , MR27T12800J-xxxTNE 48-pin plastic TSOP (TSOP I 48-P-1220-0.50-1K)
- · MR27T12800J-xxxTY, MR27T12800J-xxxTYE 48-pin plastic TSOP (TSOP I 48-P-1220-0.50-L)

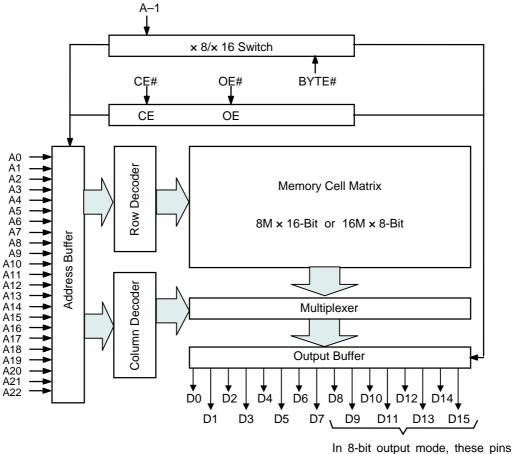
P2ROM ADVANCED TECHNOLOGY

P2ROM stands for Production Programmed ROM. This exclusive Oki technology utilizes factory test equipment for programming the customers code into the P2ROM prior to final production testing. Advancements in this technology allows production costs to be equivalent to MASKROM and has many advantages and added benefits over the other non-volatile technologies, which include the following;

- Short lead time, since the P2ROM is programmed at the final stage of the production process, a large P2ROM inventory "bank system" of un-programmed packaged products are maintained to provide an aggressive lead-time and minimize liability as a custom product.
- No mask charge, since P2ROMs do not utilize a custom mask for storing customer code, no mask charges apply.
- No additional programming charge, unlike Flash and OTP that require additional programming and handling costs, the P2ROM already has the code loaded at the factory with minimal effect on the production throughput. The cost is included in the unit price.
- · Custom Marking is available at no additional charge.
- Pin Compatible with Mask ROM



BLOCK DIAGRAM



In 8-bit output mode, these pins are placed in a high-Z state and pin D15 functions as the A-1 address pin.

PIN DESCRIPTIONS

Pin name	Functions			
D15 / A–1	Data output / Address input			
A0 to A22	Address inputs			
D0 to D14	Data outputs			
CE#	Chip enable input			
OE#	Output enable input			
BYTE#	Word / Byte select input			
V _{cc}	Power supply voltage			
V _{SS}	Ground			

FUNCTION TABLE

Mode	CE#	OE#	BYTE#	V _{CC}	D0 to D7	D8 to D14	D15/A-1
Read (16-Bit)	L	L	Н			D _{OUT}	
Read (8-Bit)	L	L	L	071	D _{OUT}	Hi–Z	L/H
Output dischle			Н	2.7 V		11: 7	
Output disable	L	Н	L	to		Hi–Z	*
Oto a dhu			Н	3.6 V		11: 7	
Standby	Н	*	L			Hi–Z	*

*: Don't Care (H or L)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	Та		0 to 70	°C
Storage temperature	Tstg	—	-55 to 125	°C
Input voltage	VI		–0.5 to V _{CC} +0.5	V
Output voltage	Vo	relative to V_{SS}	–0.5 to V _{CC} +0.5	V
Power supply voltage	Vcc		–0.5 to 5	V
Power dissipation per package	PD	Ta = 25°C	1.0	W
Output short circuit current	l _{os}	_	10	mA

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
V _{CC} power supply voltage	Vcc		2.7		3.6	V
Input "H" level	V _{IH}	V_{CC} = 2.7 to 3.6 V	2.2		V _{CC} +0.5*	V
Input "L" level	V _{IL}		-0.5**		0.6	V

Voltage is relative to V_{SS}.

 $\ast~$: Vcc+1.5V(Max.) when pulse width of overshoot is less than 10ns.

 $\ast\ast$: -1.5V(Min.) when pulse width of undershoot is less than 10ns.

PIN CAPACITANCE

 $(V_{CC} = 3.0 \text{ V}, \text{ Ta} = 25^{\circ}\text{C}, \text{ f} = 1 \text{ MHz})$

				(100 0		<u>, </u>
Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Input	C _{IN1}	$V_1 = 0 V$	—	—	8	
BYTE#	C _{IN2}	$v_1 = 0 v$	_	_	200	pF
Output	C _{OUT}	$V_{O} = 0 V$	—	—	10	

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

				$(V_{CC} = 2.7)$	to 3.6 V, Ta	= 0 to 70°C)
Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Input leakage current	ILI	$V_I = 0$ to V_{CC}	_	—	5	μA
Output leakage current	I _{LO}	$V_{O} = 0$ to V_{CC}	_	—	5	μA
V _{CC} power supply current	Iccsc	$CE\# = V_{CC}$	_	—	10	μA
(Standby)	I _{CCST}	$CE\# = V_{IH}$	_	—	1	mA
V _{CC} power supply current (Read)	I _{CCA}	$CE\# = V_{IL}, OE\# = V_{IH}$ f=5MHz			25	mA
Input "H" level	V _{IH}	—	2.2	—	V _{CC} +0.5*	V
Input "L" level	VIL	—	-0.5**	—	0.6	V
Output "H" level	V _{OH}	I _{OH} = -1 mA	2.4	_	_	V
Output "L" level	V _{OL}	I _{OL} = 2 mA	_	—	0.4	V

Voltage is relative to V_{SS}.

* : Vcc+1.5V(Max.) when pulse width of overshoot is less than 10ns.

** : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

AC CHARACTERISTICS

- MR27T12800J-xxxTN, MR27T	12800J-xxx	$(V_{CC} = 2.7 \text{ to } 3.6 \text{ V}, \text{ Ta} = 0 \text{ to } 70^{\circ}\text{C})$			
Parameter	Symbol	Condition	Min.	Max.	Unit
Address cycle time	t _C	—	90	_	ns
Address access time	t _{ACC}	$CE\# = OE\# = V_{IL}$		90	ns
CE# access time	t _{CE}	$OE\# = V_{IL}$		90	ns
OE# access time	t _{OE}	$CE\# = V_{IL}$		30	ns
Output disable time	t _{CHZ}	$OE\# = V_{IL}$	0	20	ns
Output disable time	t _{OHZ}	$CE\# = V_{IL}$	0	20	ns
Output hold time	t _{он}	$CE\# = OE\# = V_{IL}$	0	—	ns

- MR27T12800J-xxxTN, MR27T12800J-xxxTY

- MR27T12800J-xxxTNE, MR27T12800J-xxxTYE

 $(V_{CC} = 2.7 \text{ to } 3.6 \text{ V}, \text{ Ta} = 0 \text{ to } 70^{\circ}\text{C})$

Parameter	Symbol	Condition	Min.	Max.	Unit	
Addross svala time	+		$120(V_{CC} = 2.7 \text{ to } 3.0 \text{ V})$		20	
Address cycle time	t _C		100(V _{CC} = 3.0 to 3.6 V)	—	ns	
Address access time	+	CE# = OE# = V ₁₁		$120(V_{CC} = 2.7 \text{ to } 3.0 \text{ V})$	-	
	t _{ACC}	$CE# = OE# = V_{IL}$	—	$100(V_{CC} = 3.0 \text{ to } 3.6 \text{ V})$	ns	
CF# access time	1	OE# = V _{IL}		$120(V_{CC} = 2.7 \text{ to } 3.0 \text{ V})$		
CE# access time	t _{CE}		—	$100(V_{CC} = 3.0 \text{ to } 3.6 \text{ V})$	ns	
OE# access time	t _{OE}	$CE\# = V_{IL}$	—	30	ns	
Output dischla time	t _{CHZ}	$OE\# = V_{IL}$	0	20	ns	
Output disable time	t _{OHZ}	$CE\# = V_{IL}$	0	20	ns	
Output hold time	t _{OH}	$CE\# = OE\# = V_{IL}$	0	_	ns	

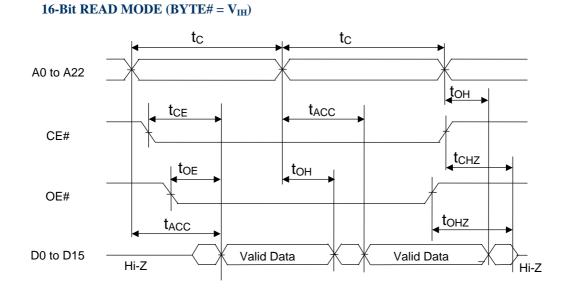
Measurement conditions

Input signal level	0 V/3 V
Input timing reference level	1/2Vcc
Output load	50 pF
Output timing reference level	- 1/2Vcc

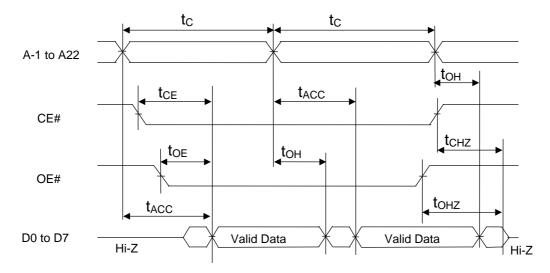
Output load

Output ~ 50 pF \pm (Including scope and jig)

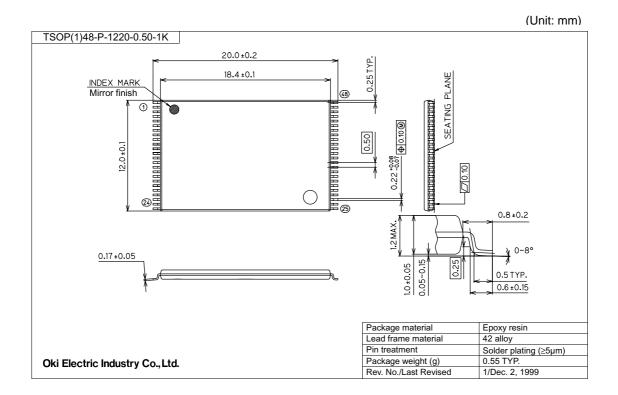
TIMING CHART (READ CYCLE)



8-BIT READ MODE (BYTE# = V_{IL})



PACKAGE DIMENSIONS

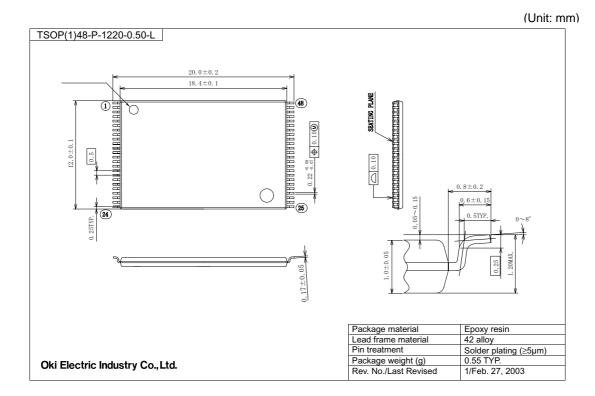


Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).





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REVISION HISTORY

Document		Pa	age	
No.	Date	Previous Current Edition Edition		Description
FEDR27T12800J-02-01	July. 2002	_	Ι	
FEDR27T12800J-02-02	Jan. 2003	1, 5	1, 5	Change tC, tACC, tCE to 120ns
FEDR27T12800J-02-03	Jan. 2003	1	1	Added P/N to MR27T12800J-xxxTNE
FEDR27T12800J-02-04	Feb. 2003	1, 5	1, 5	Added MR27T12800J-xxxTY
FEDR27T12800J-02-05	Mar. 10, 2003	1, 5	1, 5	1.Change tC, tACC, tCE to 90ns(MR27T12800J-xxxTY) 2. Added MR27T12800J-xxxTYE
FEDR27T12800J-02-06	Jun. 4, 2003	3, 4, 5	3, 4, 5	Change Ta to 0°C
FEDR27T12800J-02-07	Jul. 9, 2004	3	3	Add P_D condition and $I_{OS} = 10$ mA

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