TSOP
Commercial Temp
Industrial Temp

1M x 4
4Mb Asynchronous SRAM

8, 10, 12 ns
3.3 V V_{DD}
Center V_{DD} and V_{SS}

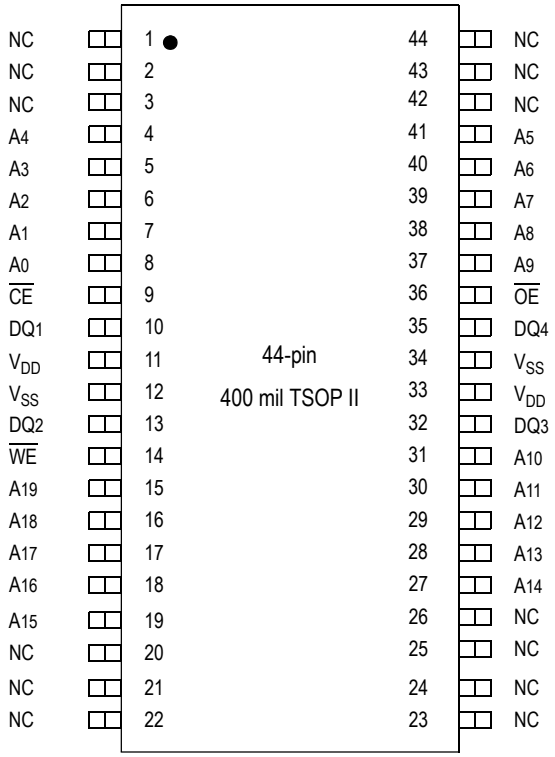
Features

- Fast access time: 8, 10, 12 ns
- CMOS low power operation: 120/95/85 mA at minimum cycle time
- Single 3.3 V power supply
- All inputs and outputs are TTL-compatible
- Fully static operation
- Industrial Temperature Option: –40° to 85°C
- Package line up
  - TP: 400 mil, 44-pin TSOP Type II package
  - GP:RoHS-compliant 400 mil, 44-pin TSOP Type II package

Description

The GS74104A is a high speed CMOS Static RAM organized as 1,048,576 words by 4 bits. Static design eliminates the need for external clocks or timing strobes. The GS74104A operates on a single 3.3 V power supply and all inputs and outputs are TTL-compatible. The GS74104A is available in a 400 mil TSOP Type-II package.

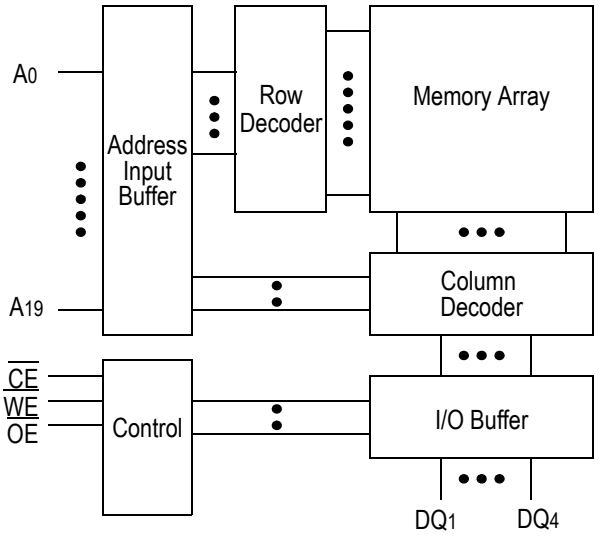
TSOP-II 1M x 4-Pin Configuration



Pin Descriptions

Symbol	Description
A_0–A_{19}	Address input
DQ_1–DQ_4	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
V_{DD}	+3.3 V power supply
V_{SS}	Ground
NC	No connect

Block Diagram



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ1 to DQ8	V_{DD} Current
H	X	X	Not Selected	I_{SB1}, I_{SB2}
L	L	H	Read	I_{DD}
L	X	L	Write	
L	H	H	High Z	

Note:
X: "H" or "L"

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}	–0.5 to +4.6	V
Input Voltage	V_{IN}	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
Output Voltage	V_{OUT}	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
Allowable power dissipation	PD	0.7	W
Storage temperature	T_{STG}	–55 to 150	°C

Note:
Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for -8/-10/-12	V_{DD}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	—	V_{DD} +0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.8	V
Ambient Temperature, Commercial Range	T_{Ac}	0	—	70	°C
Ambient Temperature, Industrial Range	T_{AI}	–40	—	85	°C

Notes:
1. Input overshoot voltage should be less than V_{DD} +2 V and not exceed 20 ns.
2. Input undershoot voltage should be greater than –2 V and not exceed 20 ns.

Capacitance

Parameter	Symbol	Test Condition	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	5	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	7	pF

Notes:
1. Tested at T_A = 25°C, f = 1 MHz
2. These parameters are sampled and are not 100% tested.

DC I/O Pin Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current	I_{IL}	V_{IN} = 0 to V_{DD}	– 1 uA	1 uA
Output Leakage Current	I_{LO}	Output High Z V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH}	I_{OH} = –4mA	2.4	—
Output Low Voltage	V_{OL}	I_{LO} = +4mA	—	0.4 V

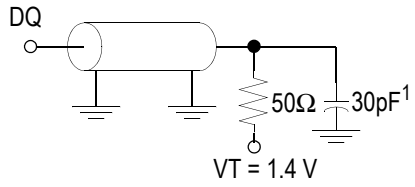
Power Supply Currents

Parameter	Symbol	Test Conditions	0 to 70°C			–40 to 85°C		
			8 ns	10 ns	12 ns	8 ns	10 ns	12 ns
Operating Supply Current	I_{DD}	$\overline{CE} \le V_{IL}$ All other inputs $\ge V_{IH}$ or $\le V_{IL}$ Min. cycle time I_{OUT} = 0 mA	120 mA	95 mA	85 mA	130 mA	105 mA	95 mA
Standby Current	I_{SB1}	$\overline{CE} \ge V_{IH}$ All other inputs $\ge V_{IH}$ or $\le V_{IL}$ Min. cycle time	30 mA	25 mA	22 mA	40 mA	35 mA	32 mA
Standby Current	I_{SB2}	$\overline{CE} \ge V_{DD}$ - 0.2V All other inputs $\ge V_{DD}$ - 0.2V or $\le$ 0.2V	10 mA			20 mA		

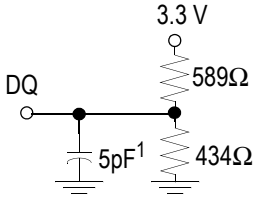
AC Test Conditions

Parameter	Conditions
Input high level	V_{IH} = 2.4 V
Input low level	V_{IL} = 0.4 V
Input rise time	tr = 1 V/ns
Input fall time	tf = 1 V/ns
Input reference level	1.4 V
Output reference level	1.4 V
Output load	**Fig. 1& 2**

Output Load 1



Output Load 2



Notes:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Output load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OHZ}

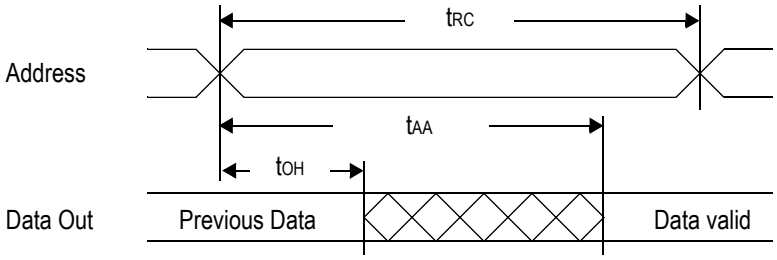
AC Characteristics

Read Cycle

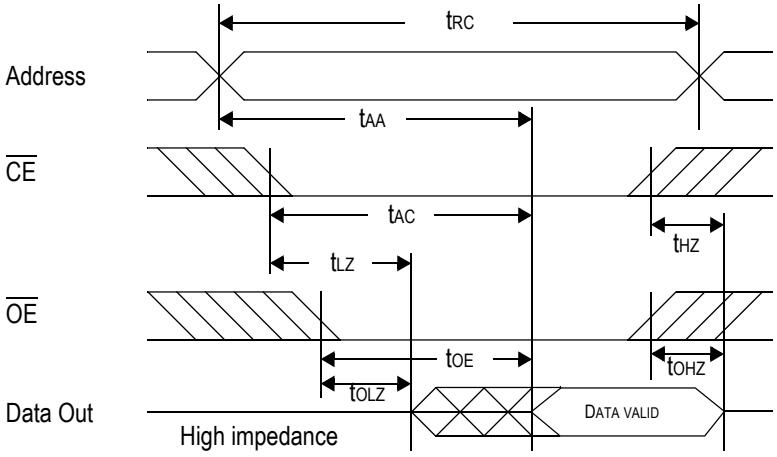
Parameter	Symbol	-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	8	—	10	—	12	—	ns
Address access time	t_{AA}	—	8	—	10	—	12	ns
Chip enable access time ($\overline{CE}$)	t_{AC}	—	8	—	10	—	12	ns
Output enable to output valid ($\overline{OE}$)	t_{OE}	—	3.5	—	4	—	5	ns
Output hold from address change	t_{OH}	3	—	3	—	3	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	3	—	3	—	3	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	—	0	—	0	—	ns
Chip disable to output in High Z ($\overline{CE}$)	t_{HZ}*	—	4	—	5	—	6	ns
Output disable to output in High Z ($\overline{OE}$)	t_{OHZ}*	—	3.5	—	4	—	5	ns

* These parameters are sampled and are not 100% tested.

Read Cycle 1: $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}



Read Cycle 2: $\overline{WE}$ = V_{IH}

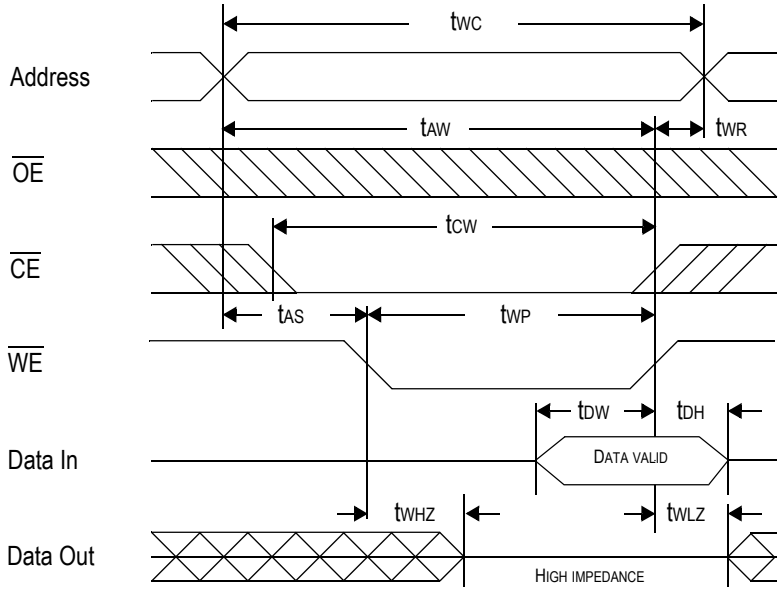


Write Cycle

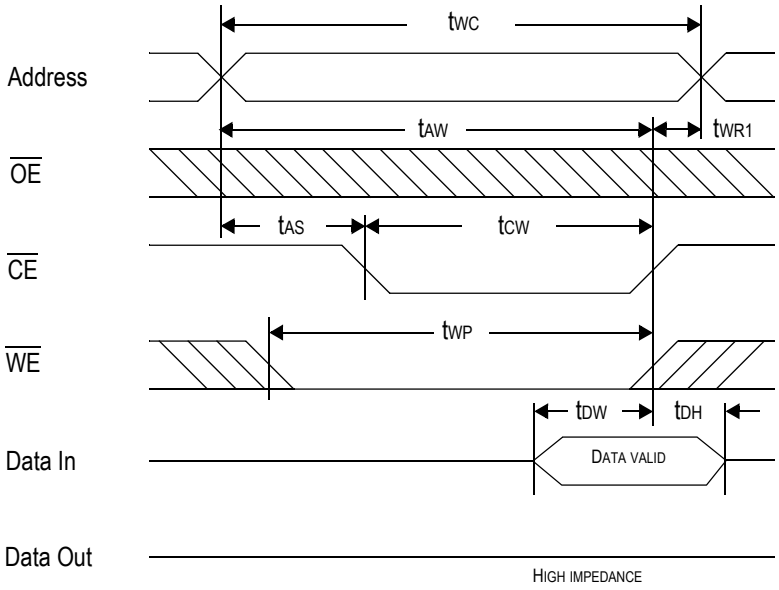
Parameter	Symbol	-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	tWC	8	—	10	—	12	—	ns
Address valid to end of write	tAW	5.5	—	7	—	8	—	ns
Chip enable to end of write	tCW	5.5	—	7	—	8	—	ns
Data set up time	tDW	4	—	5	—	6	—	ns
Data hold time	tDH	0	—	0	—	0	—	ns
Write pulse width	tWP	5.5	—	7	—	8	—	ns
Address set up time	tAS	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	tWR	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE}$)	tWR1	0	—	0	—	0	—	ns
Output Low Z from end of write	tWLZ*	3	—	3	—	3	—	ns
Write to output in High Z	tWHZ*	—	3.5	—	4	—	5	ns

* These parameters are sampled and are not 100% tested.

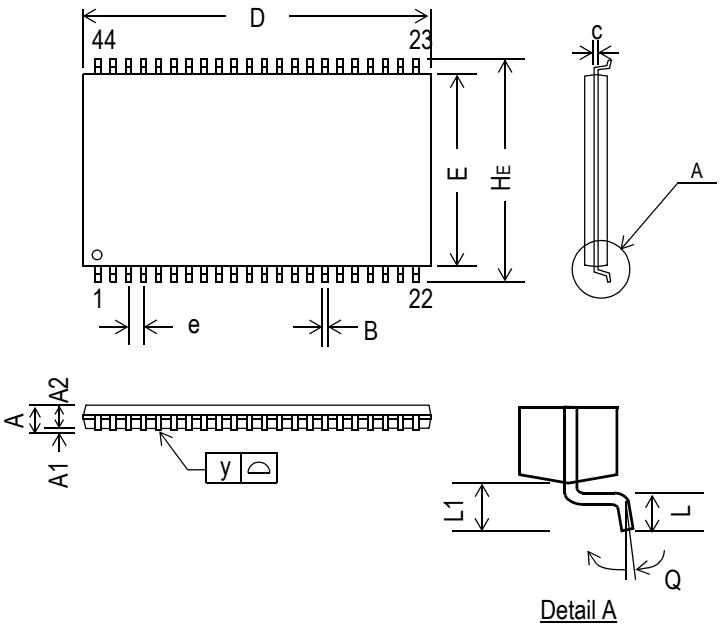
Write Cycle 1: $\overline{WE}$ control



Write Cycle 2: $\overline{CE}$ control



44-Pin, 400 mil TSOP-II



Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	—	—	0.047	—	—	1.20
A1	0.002	—	—	0.05	—	—
A2	0.037	0.039	0.041	0.95	1.00	1.05
B	0.01	0.014	0.018	0.25	0.35	0.45
c	—	0.006	—	—	0.15	—
D	0.721	0.725	0.729	18.31	18.41	18.51
E	0.396	0.400	0.404	10.06	10.16	10.26
e	—	0.031	—	—	0.80	—
HE	0.455	0.463	0.471	11.56	11.76	11.96
L	0.016	0.020	0.024	0.40	0.50	0.60
L1	—	0.031	—	—	0.80	—
y	—	—	0.004	—	—	0.10
Q	0°	—	5°	0°	—	5°

Notes:
1. Dimension D& E do not include interlead flash.
2. Dimension B does not include dambar protrusion/intrusion.
3. Controlling dimension: mm

Ordering Information

Part Number*	Package	Access Time	Temp. Range
GS74104ATP-8	400 mil TSOP-II	8 ns	Commercial
GS74104ATP-10	400 mil TSOP-II	10 ns	Commercial
GS74104ATP-12	400 mil TSOP-II	12 ns	Commercial
GS74104ATP-8I	400 mil TSOP-II	8 ns	Industrial
GS74104ATP-10I	400 mil TSOP-II	10 ns	Industrial
GS74104ATP-12I	400 mil TSOP-II	12 ns	Industrial
GS74104AGP-8	RoHS-compliant 400 mil TSOP-II	8 ns	Commercial
GS74104AGP-10	RoHS-compliant 400 mil TSOP-II	10 ns	Commercial
GS74104AGP-12	RoHS-compliant 400 mil TSOP-II	12 ns	Commercial
GS74104AGP-8I	RoHS-compliant 400 mil TSOP-II	8 ns	Industrial
GS74104AGP-10I	RoHS-compliant 400 mil TSOP-II	10 ns	Industrial
GS74104AGP-12I	RoHS-compliant 400 mil TSOP-II	12 ns	Industrial

Note:
Customers requiring delivery in Tape and Reel should add the character “T” to the end of the part number. For example: GS74104ATP-8T.

4Mb Asynchronous Datasheet Revision History

Rev. Code: Old; New	Types of Changes Format or Content	Page #/Revisions/Reason
74104A_r1	Content/Format	• Created new datasheet
74104A_r1; 74104A_r1_01	Content	• Added 6 ns speed bin • Updated all power numbers
74104A_r1_01; 74104A_r1_02	Content	• Updated Recommended Operating Currents on page 3 • Added 7 ns bin to entire document • Add X package
74104A_r1_02; 74104A_r1_03	Content	• Removed 6 ns speed bin from entire document • Removed all references to “X” package
74104A_r1_03; 74104A_r1_04	Content	• Removed 7 ns speed bin from entire document
74104A_r1_04; 74104A_r1_05	Content/Format	• Updated format • Added RoHS-compliant information for TSOP-II package
74104A_r1_05; 74104A_r1_06	Content6	• Added RoHS-compliant 400 mil, 32-pin SOJ
74104A_r1_06; 74104A_r1_07	Content6	• Removed status column (all parts MP) • (Rev1.07a: Removed SOJ references due to EOL)

