Advance Information

4K X20C05 512 x 8

High Speed AUTOSTORE™ NOVRAM

T-46-23-37

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FEATURES

- Fast Access Time: 35ns, 45ns, 55ns
- High Reliability
  - —Endurance: 1,000,000 Store Operations
  - —Retention: 100 Years Minimum
- Power-on Recall
  - —E^2PROM Data Automatically Recalled Into SRAM Upon Power-up
- AUTOSTORE™ NOVRAM
  - —User Enabled Option
  - —Automatically Stores SRAM Data Into the E^2PROM Array When V_{CC} Low Threshold is Detected
  - —Open Drain AUTOSTORE Status Output Pin
- Software Data Protection
  - —Locks Out Inadvertent Store Operations
- Low Power CMOS
  - —Standby: 250μA
- Infinite E^2PROM Array Recall, and RAM Read and Write Cycles
- Upward compatible with X20C16 (16K)

DESCRIPTION

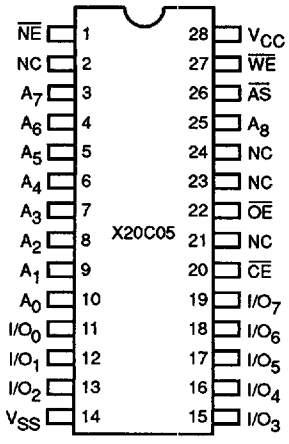
The Xicor X20C05 is a 512 x 8 NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a non-volatile electrically erasable PROM (E^2PROM). The X20C05 is fabricated with advanced CMOS floating gate technology to achieve high speed with low power and wide power-supply margin. The X20C05 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs, EPROMS and E^2PROMs.

The NOVRAM design allows data to be easily transferred from RAM to E^2PROM (store) and E^2PROM to RAM (recall). The store operation is completed in 5 ms or less and the recall operation is completed in 5 μs or less.

Xicor NOVRAMS are designed for unlimited write operations to RAM, either from the host or recalls from E^2PROM, and a minimum 1,000,000 store operations to the E^2PROM. Data retention is specified to be greater than 100 years.

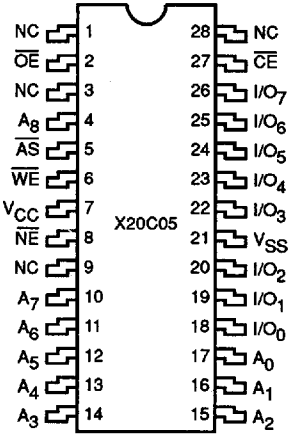
PIN CONFIGURATION

PLASTIC CERDIP



3827 FHD F02

SOIC



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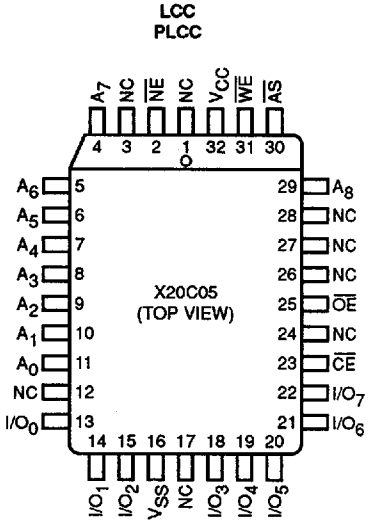
LCC PLCC



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X20C05

PIN DESCRIPTIONS

Addresses (A_0–A_8)

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read and recall operations. Output Enable LOW disables a store operation regardless of the state of $\overline{CE}$, $\overline{WE}$ or $\overline{NE}$.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X20C05 through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is HIGH or when $\overline{NE}$ is LOW.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the static RAM.

Nonvolatile Enable ($\overline{NE}$)

The Nonvolatile Enable input controls the recall function to the E²PROM array.

AUTOSTORE Output ($\overline{AS}$)

$\overline{AS}$ is an open drain output which, when asserted indicates V_{CC} has fallen below the AUTOSTORE threshold (V_{ASTH}). $\overline{AS}$ may be wire-ORed with multiple open drain outputs and used as an interrupt input to a microcontroller or as an input to a low power reset circuit.

PIN NAMES

Symbol	Description
A_0–A_8	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{NE}$	Nonvolatile Enable
$\overline{AS}$	AUTOSTORE Output
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

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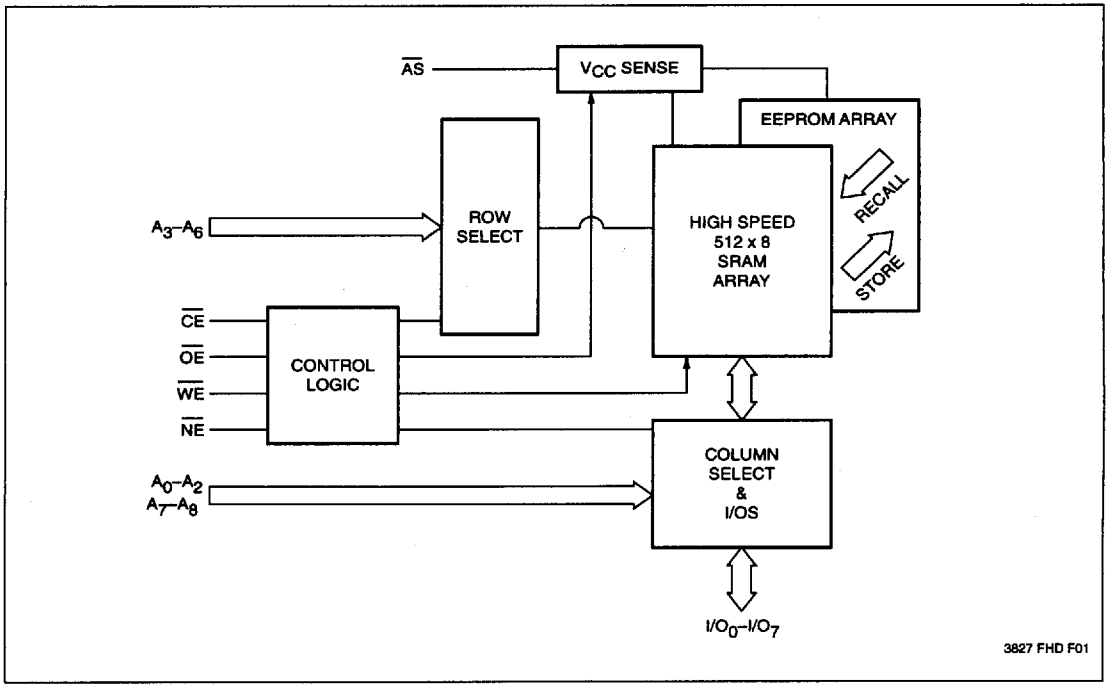
FUNCTIONAL DIAGRAM



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DEVICE OPERATION

The $\overline{CE}$, $\overline{OE}$, $\overline{WE}$ and $\overline{NE}$ inputs control the X20C05 operation. The X20C05 byte-wide NOVRAM uses a 2-line control architecture to eliminate bus contention in a system environment. The I/O bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH, or when $\overline{NE}$ is LOW.

RAM Operations

RAM read and write operations are performed as they would be with any static RAM. A read operation requires $\overline{CE}$ and $\overline{OE}$ to be LOW with $\overline{WE}$ and $\overline{NE}$ HIGH. A write operation requires $\overline{CE}$ and $\overline{WE}$ to be LOW with $\overline{NE}$ HIGH. There is no limit to the number of read or write operations performed to the RAM portion of the X20C05.

MEMORY TRANSFER OPERATIONS

There are two memory transfer operations: a recall operation whereby the data stored in the E²PROM array is transferred to the SRAM array; and a store operation which causes the entire contents of the SRAM array to be stored in the E²PROM array.

Recall operations are performed automatically upon power-up and under host system control when $\overline{NE}$, $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH. The recall operation takes a maximum of 5µs.

There are two methods of initiating a store operation. The first is the software store command. This command takes the place of the hardware store employed on the X20C04. This command is issued by entering into the special command mode: $\overline{NE}$, $\overline{CE}$ and $\overline{WE}$ strobe LOW while at the same time a specific address and data combination is sent to the device. This is a three step operation: the first address/data combination is 155[H]/AA[H]; the second combination is 0AA[H]/55[H]; and the final command combination is 155[H]/33[H]. This sequence of pseudo write operations will immediately initiate a store operation. Refer to the software command timing diagrams for details on set and hold times for the various signals.

The second method of storing data is through the AUTOSTORE command. When enabled, data is automatically stored from the RAM into the E²PROM array whenever V_{CC} falls below the preset AUTOSTORE threshold. This feature is enabled by performing the first two steps for the software store with the command combination being 155[H]/CC[H].

The AUTOSTORE feature is disabled by issuing the three step command sequence with the command combination being 155[H]/CD[H]. The AUTOSTORE feature will also be reset if V_{CC} falls below the power-on reset threshold (approximately 3.5V) and is then raised back into the operating range.

DATA PROTECTION

The X20C05 supports two methods of protecting the nonvolatile data.

—If after power-up neither the software store nor AUTOSTORE feature are enabled, no store can occur.

—If after power-up no SRAM write operations have occurred no store operation can be initiated. The software store and AUTOSTORE commands will be ignored.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
———	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

X20C05

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–65°C to +135°C
Storage Temperature .....–65°C to +150°C
Voltage on any Pin with
Respect to Ground .....–1.0V to +7V
D.C. Output Current 10mA

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

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***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Supply Voltage	Limits
X20C05	5V ±10%

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D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Units	
I_{CC1}	V_{CC} Current (Active)		100	mA	$\overline{NE} = \overline{WE} = V_{IH}$, $\overline{CE} = \overline{OE} = V_{IL}$ Address Inputs = 0.4V/2.4V Levels @ f = 20MHz. All I/Os = Open
I_{CC2}	V_{CC} Current During Store		5	mA	All Inputs = V_{IH}
I_{CC3}	V_{CC} Current During AUTOSTORE		2.5	mA	All I/Os = Open
I_{SB1}	V_{CC} Standby Current (TTL Input)		10	mA	$\overline{CE} = V_{IH}$ All Other Inputs = V_{IH}, All I/Os = Open
I_{SB2}	V_{CC} Standby Current (CMOS Input)		250	µA	All Inputs = $V_{CC} - 0.3$ All I/Os = Open
I_{LI}	Input Leakage Current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}(1)	Input Low Voltage	–1.0	0.8	V	
V_{IH}(1)	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 5mA
V_{OLAS}	AUTOSTORE Output		0.4	V	I_{OLAS} = 1mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = –4mA

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POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(2)	Power-Up to RAM Operation	100	µs
t_{PUW}(2)	Power-Up to Nonvolatile Operation	5	ms

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CAPACITANCE T_A = 25°C, F = 1.0MHZ, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	6	pF	V_{IN} = 0V

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Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

X20C05

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	100,000	Changes/Bit
Store Cycles	1,000,000	Store Cycles
Data Retention	100	Years

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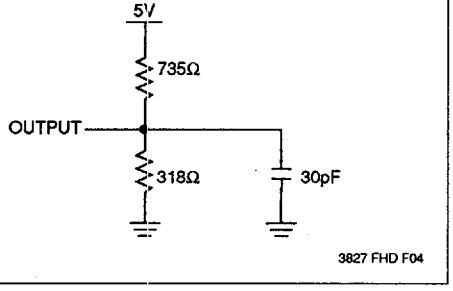
MODE SELECTION

$\overline{CE}$	$\overline{WE}$	$\overline{NE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	X	Not Selected	Output High Z	Standby
L	H	H	L	Read RAM	Output Data	Active
L	L	H	X	Write "1" RAM	Input Data High	Active
L	L	H	X	Write "0" RAM	Input Data Low	Active
L	H	L	L	Array Recall	Output High Z	Active
L	L	L	H	Software Command	Input Data	Active
L	H	H	H	Output Disabled	Output High Z	Active
L	L	L	L	Not Allowed	Output High Z	Active
L	H	L	H	No Operation	Output High Z	Active

3827 PGM T09

EQUIVALENT A.C. LOAD CIRCUIT



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A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing Levels	1.5V

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X20C05

A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified)

Read Cycle Limits

Symbol	Parameter	X20C05-35		X20C05-45		X20C05-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	35		45		55		ns
t_{CE}	Chip Enable Access Time		35		45		55	ns
t_{AA}	Address Access Time		35		45		55	ns
t_{OE}	Output Enable Access Time		20		25		30	ns
t_{LZ}(3)	Chip Enable to Output in Low Z	0		0		0		ns
t_{OLZ}(3)	Output Enable to Output in Low Z	0		0		0		ns
t_{HZ}(3)	Chip Disable to Output in High Z		15		20		25	ns
t_{OHZ}(3)	Output Disable to Output in High Z		15		20		25	ns
t_{OH}	Output Hold From Address Change	0		0		0		ns

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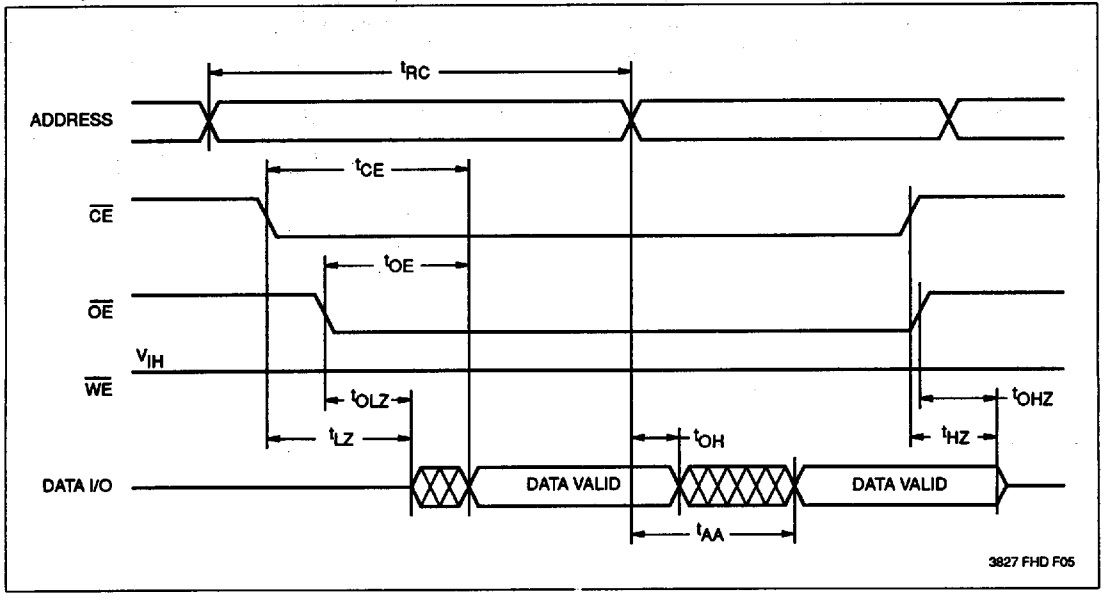
Read Cycle



Note: (3) t_{LZ} min., t_{HZ}, t_{OLZ} min., and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} and t_{OHZ} are measured, with C_L = 5pF, from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outptus are no longer driven.

X20C05

Write Cycle Limits

Symbol	Parameter	X20C05-25		X20C05-35		X20C05-45		X20C05-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	25		35		45		55		ns
t_{CW}	Chip Enable to End of Write Input	25		30		35		40		ns
t_{AS}	Address Setup Time	0		0		0		0		ns
t_{WP}	Write Pulse Width	30		30		35		40		ns
t_{WR}	Write Recovery Time	0		0		0		0		ns
t_{DW}	Data Setup to End of Write	15		15		20		25		ns
t_{DH}	Data Hold Time	0		0		3		3		ns
t_{WZ}(4)	Write Enable to Output in High Z				15		20		25	ns
t_{OW}(4)	Output Active from End of Write	5		5		5		5		ns
t_{OZ}(4)	Output Enable to Output in High Z				15		20		25	ns

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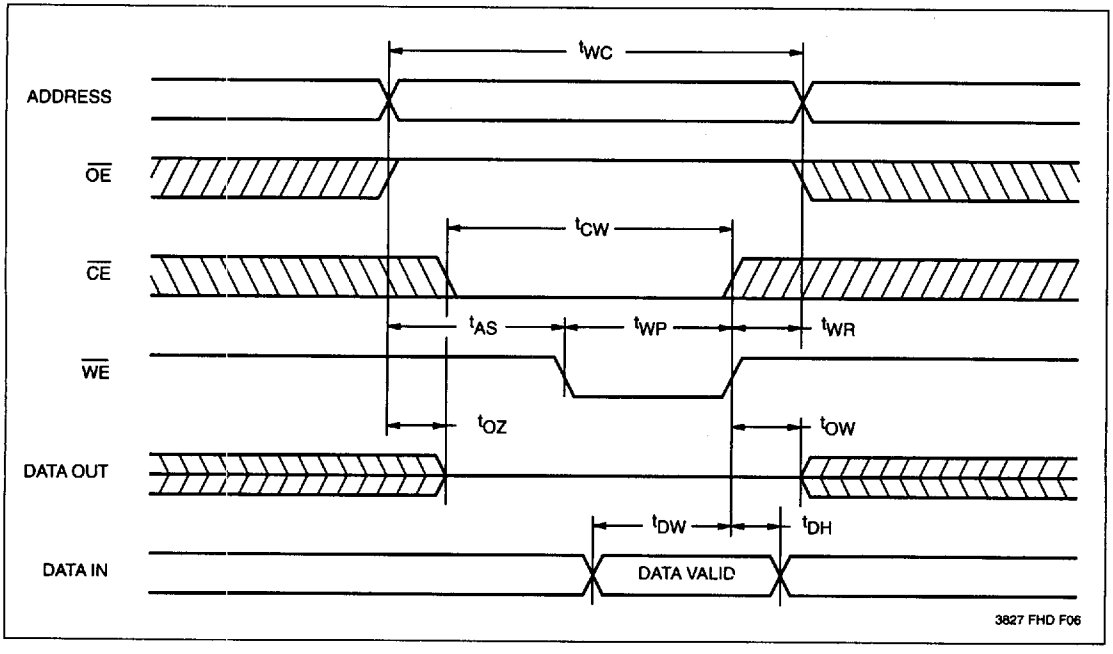
$\overline{WE}$ Controlled Write Cycle

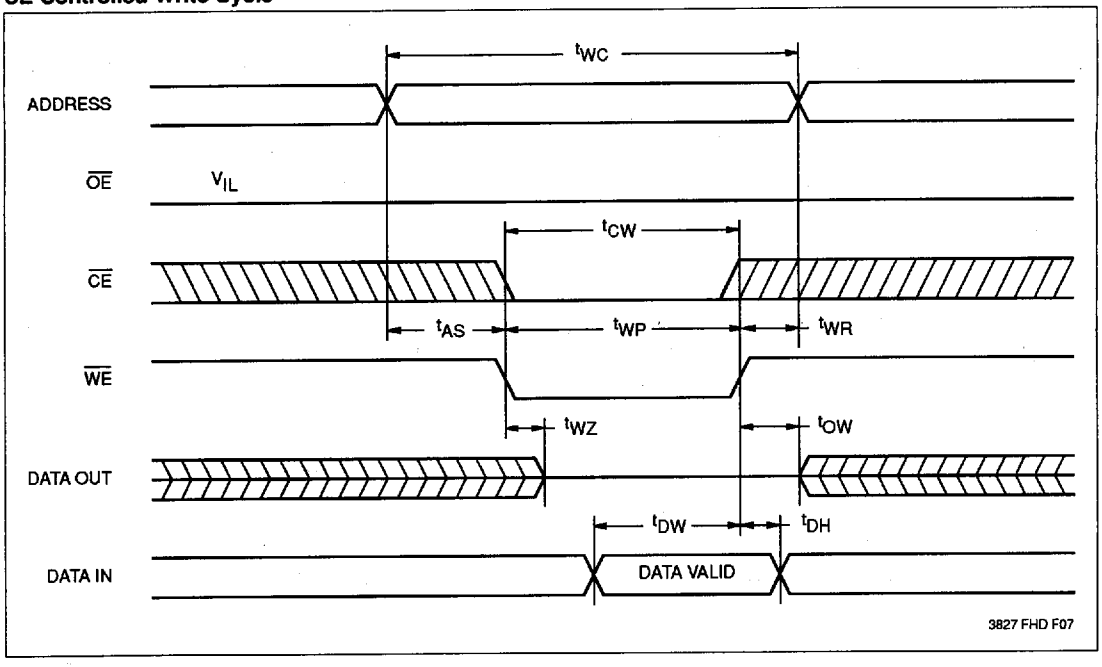


3827 FHD F06

Note: (4) t_{WZ}, t_{OW} and t_{CZ} are periodically sampled and not 100% tested.

X20C05

$\overline{CE}$ Controlled Write Cycle



X20C05

Array Recall Cycle Limits

Symbol	Parameter	X20C05-35		X20C05-45		X20C05-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RCC}	Array Recall Cycle Time		5		5		5	µs
t_{RCP}(7)	Recall Pulse Width to InitiateRecall	30		40		50		ns
t_{RWE}	$\overline{WE}$ Setup Time to $\overline{NE}$	0		0		0		ns

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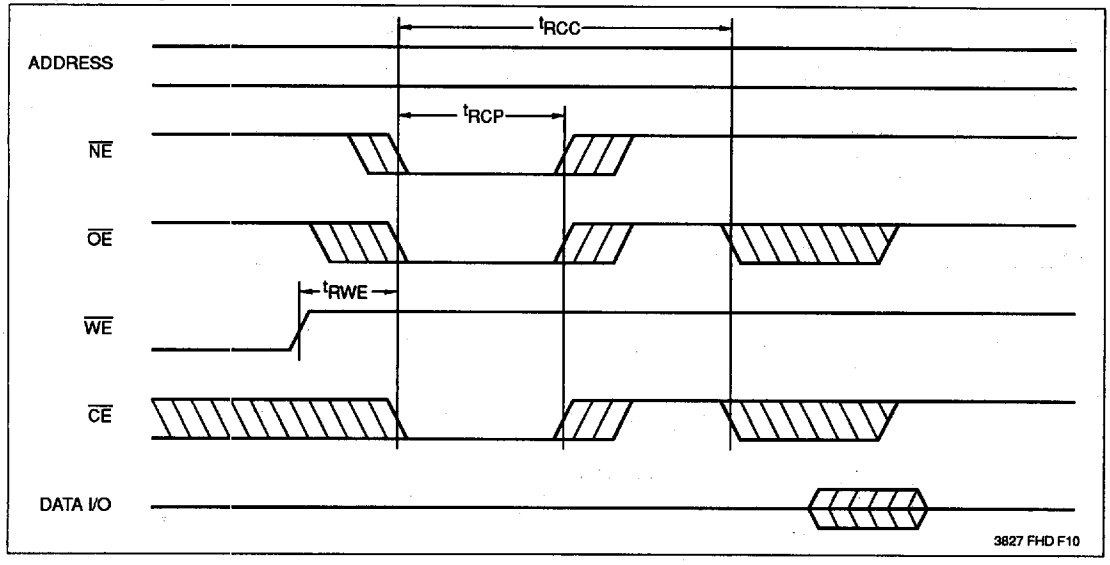
Array Recall Cycle



3827 FHD F10

Note: (7) The Recall Pulse Width (t_{RCP}) is a minimum time that $\overline{NE}$, $\overline{OE}$ and $\overline{CE}$ must be LOW simultaneously. To insure data integrity, $\overline{NE}$ and $\overline{CE}$ must remain HIGH after initiation of and through the duration (t_{RCC}) of the Recall operation. During t_{RCC}, $\overline{OE}$ and $\overline{WE}$ may go LOW providing the host access to other devices in the system.

X20C05

Software Command Timing Limits

Symbol	Parameter	X20C05-35		X20C05-45		X20C05-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{STO}	Store Cycle Time		5		5		5	ms
t_{SP}(5)	Store Pulse Width	30		40		50		ns
t_{SPH}	Store Pulse Hold Time	35		45		55		ns
t_{WC}	Write Cycle Time	35		45		55		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{AH}	Address Hold time	0		0		0		ns
t_{DS}	Data Setup Time	15		20		25		ns
t_{DH}	Data Hold Time	0		3		3		ns
t_{SOE}(6)	$\overline{OE}$ Disable to Store Function	20		20		20		ns
t_{OEST}(6)	Output Enable from End of Store	10		10		10		ns
t_{NHZ}(6)	Nonvolatile Enable to Output in High Z		15		20		25	ns

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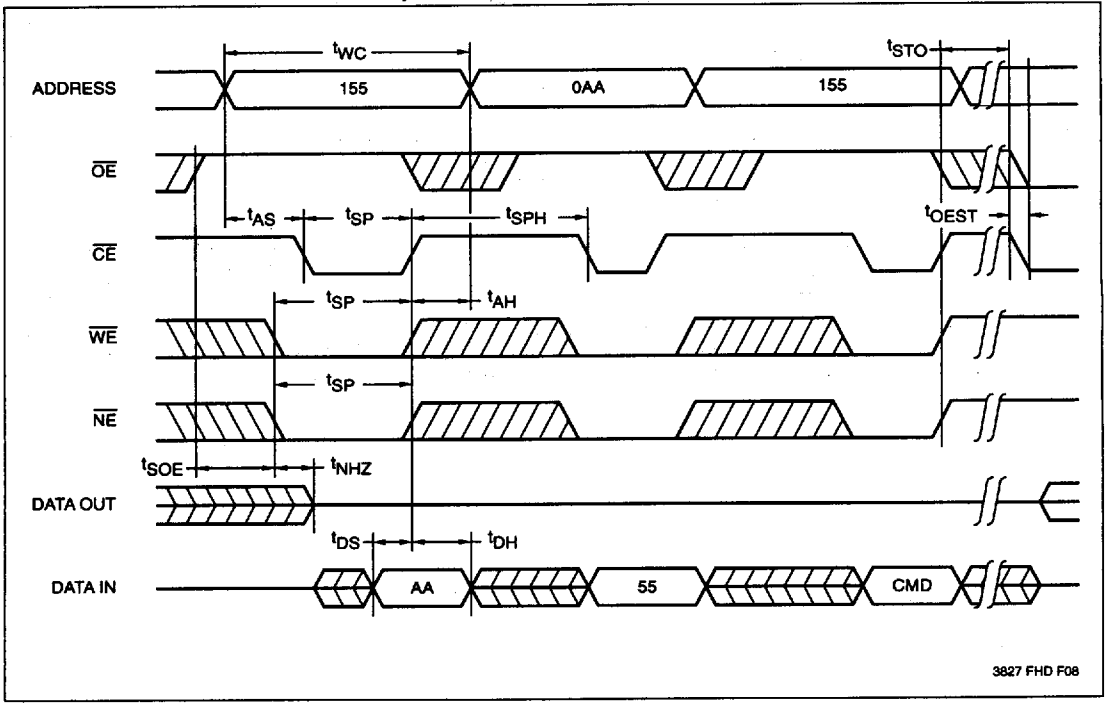
$\overline{CE}$ Controlled Software Command Sequence



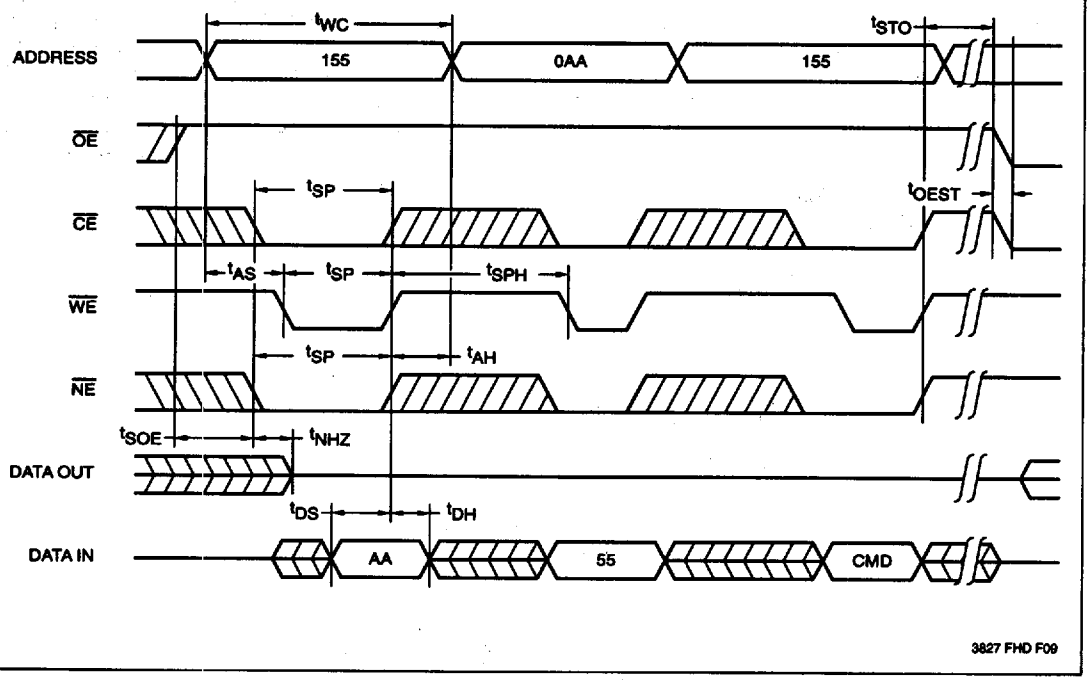
3827 FHD F08

Notes: (5) The Store Pulse Width (t_{SP}) is a minimum time that $\overline{NE}$, $\overline{WE}$ and $\overline{CE}$ must be LOW simultaneously. To insure data integrity, $\overline{NE}$ and $\overline{CE}$ must remain HIGH after initiation of and throughout the duration (t_{STO}) of the Store operation. During t_{STO}, $\overline{OE}$ and $\overline{WE}$ may go LOW providing the host system access to other devices in the system.

(6) t_{SOE}, t_{OEST} and t_{NHZ} are periodically sampled and not 100% tested.

X20C05

$\overline{WE}$ Controlled Software Command Sequence



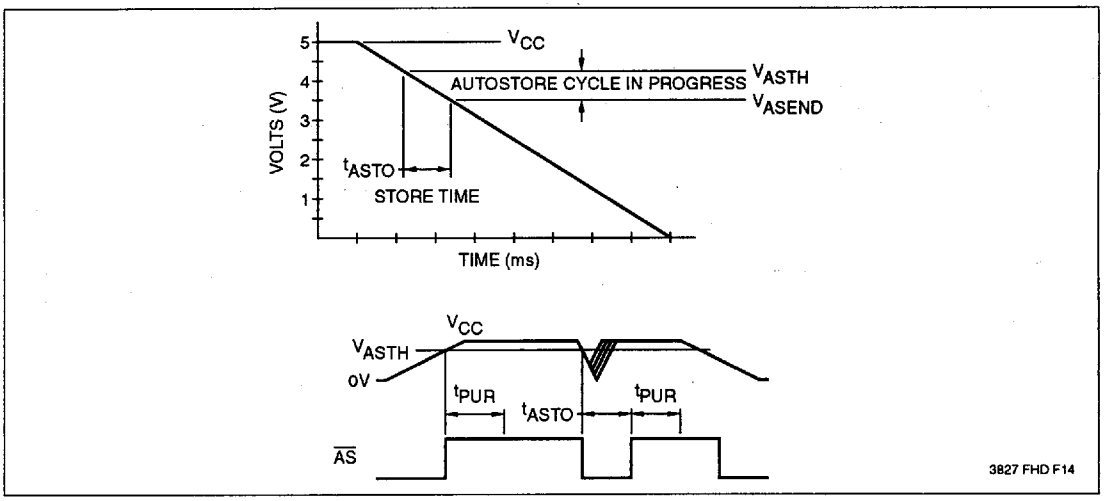
X20C05

AUTOSTORE Feature

The AUTOSTORE feature automatically saves the contents of the X20C05's Static RAM to the on-board bit-for-bit shadow E²PROM at power down. This circuitry insures that no data is lost during accidental power downs or general system crashes, and is ideal for microprocessor caching systems, embedded software systems, and general system back-up memory.

The AUTOSTORE instruction (EAS) to the SDP register sets the AUTOSTORE enable latch, allowing the X20C05 to automatically perform a store operation whenever V_{CC} falls below the AUTOSTORE threshold (V_{ASTH}). V_{CC} must remain above the AUTOSTORE Cycle End Voltage (V_{ASEND}) for the duration of the store cycle (t_{ASTO}). The detailed timing for this feature is illustrated in the AUTOSTORE timing diagrm, below. Once the AUTOSTORE cycle is initiated, all other device functions are inhibited.

AUTOSTORE CYCLE Timing Diagrams



AUTOSTORE CYCLE LIMITS

Symbol	Parameter	X20C05		Units
		Min.	Max.	
t_{ASTO}	AUTOSTORE Cycle Time		2.5	ms
V_{ASTH}	AUTOSTORE Threshold Voltage	4.0	4.3	V
V_{ASEND}	AUTOSTORE Cycle End Voltage	3.5		V

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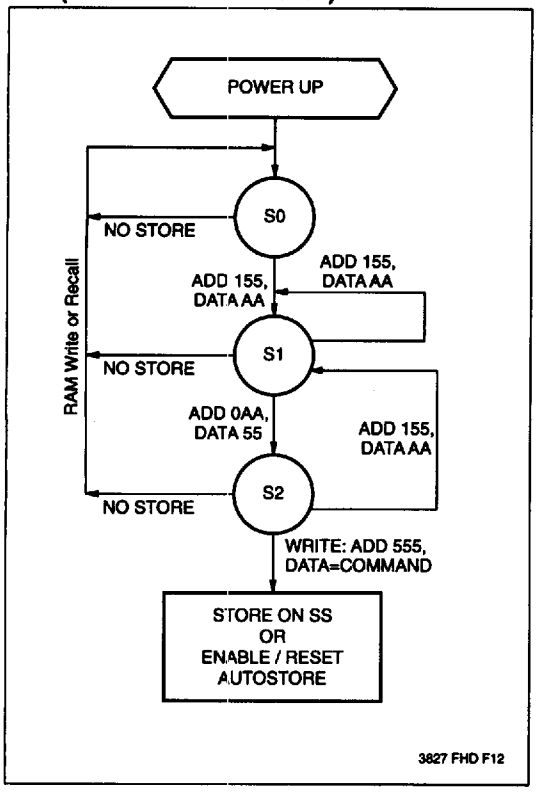
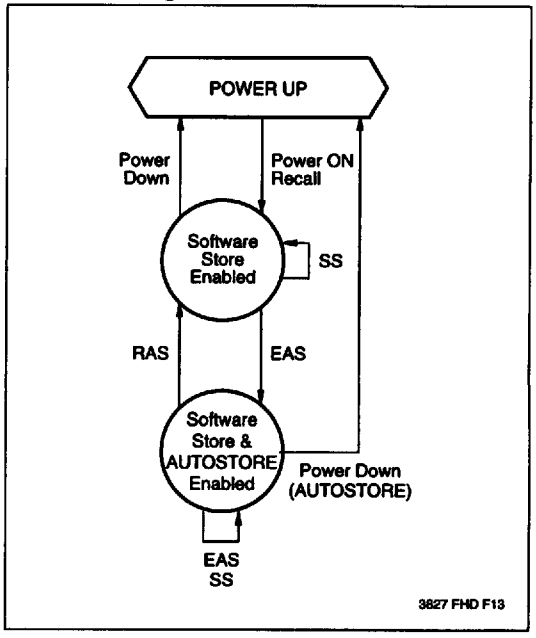
X20C05

SDP (Software Data Protection)



Store State Diagram



SOFTWARE DATA PROTECTION COMMANDS

Command		Data [Hex]
EAS	Enable AUTOSTORE	CC
RAS	Reset AUTOSTORE	CD
SS	Software Store	33

3827 PGM T14