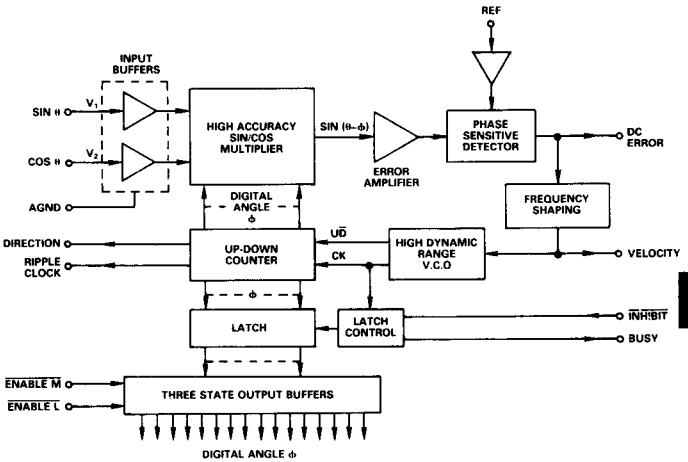
Hybrid, Tracking Resolver-to-Digital Converters

1S20/1S40/1S60/1S61

FEATURES
Low Cost
32-Pin Hybrid
High Tracking Rate 170rps at 12 Bits
Velocity Output
DC Error Output
Logic Outputs for Extension Pitch Counter

APPLICATIONS
Numerical Control of Machine Tools
Robotics

1S20/1S40/1S60/1S61 FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The 1S20/40/60/61 are a series of low cost hybrid converters with a high tracking rate and all essential features for numerically controlled machine applications. These converters are housed in a 32-pin triple DIP ceramic package measuring 1.1″ × 1.7″ × 0.205″ (28 × 43.2 × 5.2mm).

The 1S20/40/60/61 convert resolver format input signals into a parallel natural binary digital word. Typically, these signals would be obtained from a brushless resolver and the resolver/converter combination gives a parallel absolute angular output word similar to that provided by an absolute encoder. The ratiometric conversion principle of the 1S20/40/60/61 series ensures high noise immunity and tolerance of lead length when the converter is at a distance from the resolver.

The output word is in three-state digital logic form with a high and low byte enable input so that the converter can communicate with an 8- or 16-bit digital highway. In this series there are 12-, 14- and two 16-bit resolution (±4 arc mins and ±10 arc mins accuracy) models available.

Repeatability is 1LSB for all models under constant temperature conditions.

The 1S20/40/60/61 are available with three frequency options covering the range 400Hz to 10kHz.

Models Available

Four models are available in this range and three frequency options for each model.

1S20 is a 12-bit up to 170 revolutions per second
1S40 is a 14-bit up to 42.5 revolutions per second
1S60 is a 16-bit up to 10.5 revolutions per second
1S61 is a 16-bit up to 10.5 revolutions per second

APPLICATIONS/USER BENEFITS

The 1S20/40/60/61 has been specifically designed for the numerically controlled machine and robot industry. Using the type 2 servo loop tracking principle ideally suits these converters to the electrically noisy environment found in these industrial applications.

By using hybrid construction techniques, small size, low power and high reliability are further benefits offered by these converters. This small size with the three-state digital outputs makes these converters ideal for multichannel operation.

The layout of the connections simplifies the parallel connection to a digital highway.

The provision of the digital outputs of DIRECTION and RIPPLE CLOCK allow simple extension counters for multi-pitch operation to be implemented.

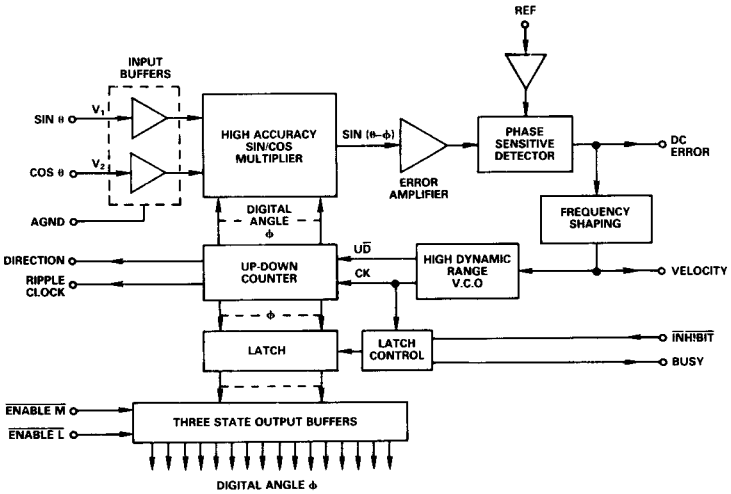
Analog outputs of velocity and dc error for control loop stabilization and bite (built in test) provide two more features required in these applications.

SPECIFICATIONS (typical @ +25°C, unless otherwise specified)

Models	1S20	1S40	1S60	1S61	Units
RESOLUTION	12	14	16	16	Bits
ACCURACY[1]	±8.5	±5.3	±4.0	±10	arc-mins
REPEATABILITY[2]	1	*	*	*	LSB
SIGNAL AND REFERENCE FREQUENCY[3]	400-10k	*	*	*	Hz
DIGITAL OUTPUT	Parallel natural binary				
Max Load	20	*	*	*	LSTTL
TRACKING RATE (min)					
400Hz – 2.6kHz	50	12.5	3.0	3.0	rps
2.6kHz – 5kHz	90	22.5	5.5	5.5	rps
5kHz – 10kHz	170	42.5	10.5	10.5	rps
SETTLING TIME					
400Hz – 2.6kHz	150	180	350	350	ms
2.6kHz – 5kHz	40	50	130	130	ms
5kHz – 10kHz	20	25	60	60	ms
ACCELERATION CONSTANT (K_a)					
400Hz – 2.6kHz	9,500	*	*	*	sec^{-2}
2.6kHz – 5kHz	144,000	*	*	*	sec^{-2}
5kHz – 10kHz	713,000	*	*	*	sec^{-2}
SIGNAL VOLTAGE	2.0	*	*	*	V rms
SIGNAL INPUT IMPEDANCE	>10	*	*	*	MΩ
REFERENCE VOLTAGE	2.0	*	*	*	V rms
REFERENCE INPUT IMPEDANCE	125	*	*	*	kΩ
ALLOWABLE PHASE SHIFT[4]					
(Signal to Reference)	±10	*	*	*	Degrees
BUSY OUTPUT[5]	Logic "Hi" when Busy				
Max Load	20	*	*	*	LSTTL
BUSY WIDTH	430	*	*	*	ns
ENABLE INPUTS	Logic "Lo" to ENABLE				
Load	1	*	*	*	LSTTL
ENABLE AND DISABLE TIMES	120(typ)	*	*	*	ns
	220(max)	*	*	*	ns
INHIBIT INPUT	Logic "Lo" to INHIBIT	*	*	*	
Load	1	*	*	*	LSTTL
DIRECTION OUTPUT (DIR)[5]	Logic "Hi" when counting up Logic "Lo" when counting down				
Max Load	20	*	*	*	LSTTL
RIPPLE CLOCK[5]	Negative pulse indicating when internal counters change from all "1's" to all "0's" or vice versa.				
Max Load	20	*	*	*	LSTTL
VELOCITY OUTPUT[6] (at specified min tracking rate).					
Polarity	positive for increasing angle	*	*	*	–
Output Voltage[7]	±10	*	*	*	V dc
Accuracy	±10	*	*	*	% FSD
Zero Offset	±8	*	*	*	mV
DC ERROR OUTPUT VOLTAGE[6]	40	10	2.5	2.5	mV/LSB
POWER SUPPLIES					
$+V_S$	+11.5 to +16	*	*	*	V
$-V_S$	−11.5 to −16	*	*	*	V
+5V	+4.75 to +5.25	*	*	*	V
POWER SUPPLY CONSUMPTION[7]					
$+V_S$	20, 30 (max)	*	*	*	mA
$-V_S$	20, 30 (max)	*	*	*	mA
+5V	105, 125 (max)	*	*	*	mA
POWER DISSIPATION[7]	1.1, 1.5 (max)	*	*	*	W
TEMPERATURE RANGE					
Operating	0 to +70	*	*	*	°C
Storage	−55 to +125	*	*	*	°C
PACKAGE OPTION[8]	DH-32E	*	*	*	
WEIGHT	1(28)	*	*	*	oz. (grms)

NOTES
[1]Specified over the operating temperature range and for:
a). ±10% signal and reference amplitude variation.
b). 10% signal and reference harmonic distortion.
c). ±10% on frequency range of option.
[2]Specified at constant temperature. Over the operating temperature range, worst case repeatability could be up to 1.5 arc mins for all models.
[3]See frequency range options.
[4]For no additional error with a static input, see "Dynamic Accuracy vs. Resolver Phase Shift"
[5]See timing diagram.
[6]These outputs should be connected via buffers or comparator inputs (max load 100pF).
[7]$\pm V_S = \pm 15$ volts.
[8]See Section 14 for package outline information.
*Specifications same as 1S20.
Specifications subject to change without notice.

FUNCTIONAL DIAGRAM



BIT WEIGHT TABLE

Bit Number	Weight in Degrees
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12	0.0879
13	0.0440
14	0.0220
15	0.0110
16	0.0055

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THEORY OF OPERATION

The sine and cosine signals are applied to the signal input.

$V_1 = K E_O \text{ Sin } \omega t \text{ Sin } \theta$
$V_2 = K E_O \text{ Sin } \omega t \text{ Cos } \theta$

Where θ is the angle of the resolver shaft or the distance through a particular pitch of the Inductosyn™.

To understand the conversion process, then assume that the current word state of the up-down counter is ϕ.

V_1 is multiplied by Cos ϕ and V_2 is multiplied by Sin ϕ to give:

$K E_O \text{ Sin } \omega t \text{ Sin } \theta \text{ Cos } \phi$
and $K E_O \text{ Sin } \omega t \text{ Cos } \theta \text{ Sin } \phi$

These signals are subtracted by the error amplifier to give:

$K' E_O \text{ Sin } \omega t \text{ (Sin } \theta \text{ Cos } \phi - \text{Cos } \theta \text{ Sin } \phi)$
or $K' E_O \text{ Sin } \omega t \text{ Sin } (\theta - \phi)$

A phase sensitive detector, integrator and Voltage Controlled Oscillator (VCO) form a closed loop system which seeks to null Sin $(\theta - \phi)$.

When this is accomplished, the word state of the up-down counter (ϕ), equals, within the rated accuracy of the converter, the resolver shaft angle θ.

OPERATION OF THE CONVERTER

The 1S20/40/60/61 are tracking converters, this means that the output automatically follows the input for speeds up to the maximum tracking rate for the frequency option specified. No convert command is necessary as the conversion is initiated by each LSB increment of the input. Each LSB increment of the converter initiates a BUSY pulse.

As the digital output of the converter passes through the major carry; i.e., all "1's" to all "0's" or the converse, a RIPPLE CLOCK (RC) logic output is initiated indicating that a revolution or a pitch of the input has been completed.

The direction of input rotation is indicated by the DIRECTION (DIR) logic output. This direction data is *always* valid in advance of a RIPPLE CLOCK pulse.

The $\overline{\text{INHIBIT}}$ logic input only inhibits the data transfer from the up-down counter to the output latches and therefore does not interrupt the operation of the tracking loop. Releasing the $\overline{\text{INHIBIT}}$ automatically generates a BUSY pulse to refresh the output data.

Two $\overline{\text{ENABLE}}$ inputs are provided, $\overline{\text{ENABLE M}}$ for the Most Significant 8 bits and $\overline{\text{ENABLE L}}$ for the Least Significant remainder. The operation of these enables has no effect on the conversion process.

The tracking conversion technique produces an internal signal at the input to the VCO that is proportional to the rate of the input angle. This is a bipolar dc analog signal that is made available at the VELOCITY (VEL) pin. As this is an internal control signal it is not closely characterized.

The signal at the output of the phase sensitive detector is the input to the internal nulling loop and hence is proportional to the error between the input angle and the output digital angle. As the converter is a type 2 servo loop, this DC ERROR signal will increase if the output angle fails to track the input for any reason, it is therefore an indication that the input has exceeded the maximum tracking rate of the converter or due to some internal malfunction, the converter is unable to reach a null. By the use of two external comparators this voltage can be used as a "built in test".

NOTE: The DC ERROR voltage has no internal filtering.

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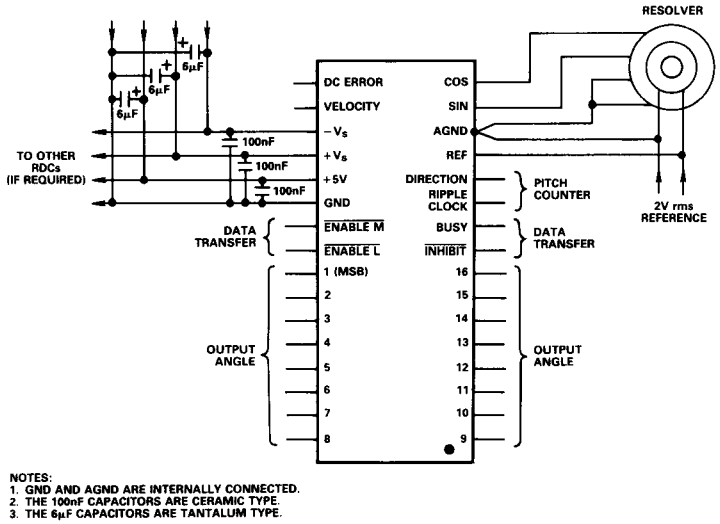


Figure 1. Electrical Connections

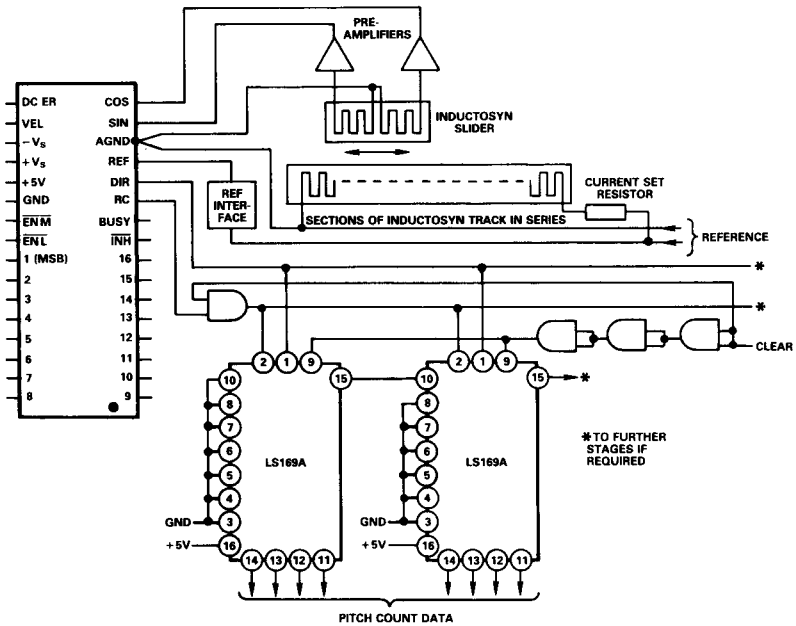


Figure 2. Connections for Use with Industosyn/"LS" External Counters

CONNECTING THE CONVERTER

The electrical connection of the converter is straight-forward. The power supply voltages connected to $+V_S$ and $-V_S$ pins can be ±12V to ±15V but must not be reversed. The +5V supply connects to the +5V pin and should not be allowed to become negative with respect to the GND pin.

It is suggested that decoupling capacitors of 100nF are connected in parallel between the power lines ($+V_S$, $-V_S$ and +5V) and GND adjacent to the converter.

When more than one converter is used on a card, then separate decoupling capacitors should be used for each converter (refer to Figure 1).

The converter has some H/F decoupling provided internally, as well as input protection on the signal and reference inputs.

The resolver connections are made to the sine and cosine inputs, reference and analog ground as shown in the electrical connection diagram (Figure 1).

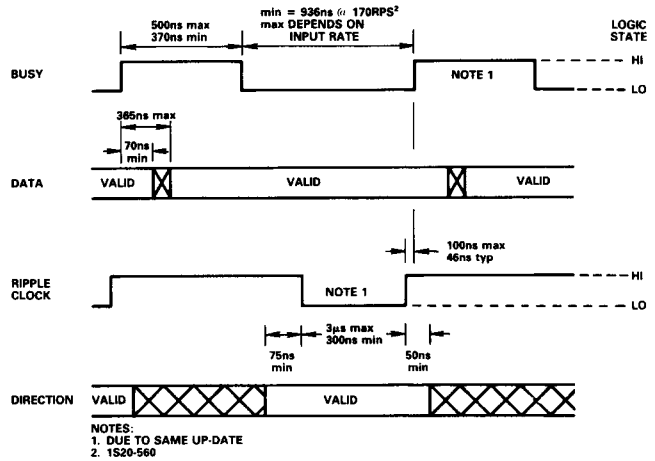


Figure 3. Timing Diagram

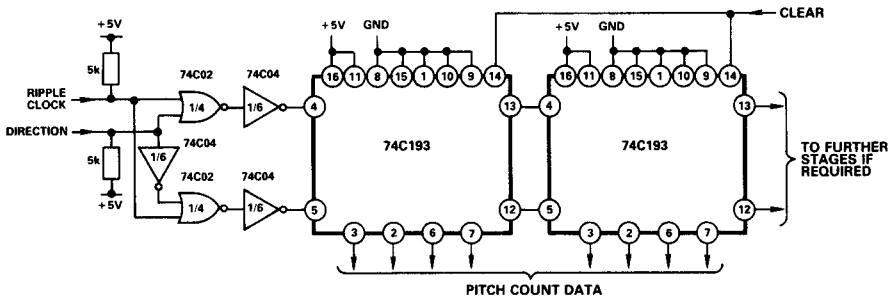


Figure 4. CMOS External Counter

DATA TRANSFER

The readiness of the converter for data transfer is given by the state of the BUSY output. The signal appearing on the BUSY output pin is a series of pulses of TTL levels when the angular input of the converter is changing. A BUSY pulse is initiated each time the input moves by an LSB and the internal counter is incremented or decremented. With the $\overline{\text{INHIBIT}}$ input pin in the "Hi" TTL state, data will be transferred automatically to the output latches.

The $\overline{\text{ENABLE}}$ input pin determines the state of the output data. A TTL logic "Hi" maintains the output data pins in a high impedance condition, the application of a logic "Lo" presents the data in the latches to the output pins.

From the above it can be seen that there are two methods available for transferring data.

One method is to transfer data when the BUSY is in a "Lo" state or clock the data out on the trailing edge of the BUSY pulse. Both the $\overline{\text{INHIBIT}}$ and the $\overline{\text{ENABLES}}$ must be in their correct state of "Hi" and "Lo's" respectively.

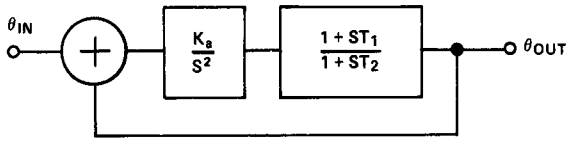
The alternative method is to use the $\overline{\text{INHIBIT}}$ input. Data will always be valid one microsecond after the application of a logic "Lo" to the $\overline{\text{INHIBIT}}$. This is regardless of the time when the $\overline{\text{INHIBIT}}$ is applied.

In order to count input revolutions or pitches, an external extension counter is required. A circuit performing this function is shown in Figure 2.

The DIRECTION (DIR) and RIPPLE CLOCK (RC) logic outputs should always be used in the manner shown in the application circuit. We recommend the circuit in Figure 2 to be used as the circuit in Figure 4 uses CMOS and great care must be taken to keep the stray capacitances low because of the high tracking rate of the converter.

DYNAMIC PERFORMANCE

The transfer function of the converter is given below.



Open loop gain:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_a}{S^2} \cdot \frac{1 + ST_1}{1 + ST_2}$$

Closed loop gain:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1 + ST_1}{1 + ST_1 + \frac{S^2}{K_a} + \frac{S^3 T_2}{K_a}}$$

1S20/1S40/1S60/1S61 (typical values)

Constant \ Option	510	550	560
K_a	9,500	144,000	713,000
T_1	17.4ms	4.1ms	1.85ms
T_2	2.6ms	0.6ms	0.25ms
Gain Plot	Figure 5	Figure 7	Figure 9
Phase Plot	Figure 6	Figure 8	Figure 10

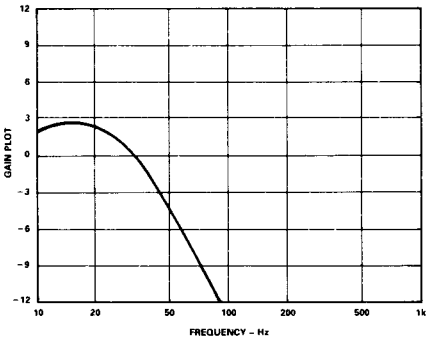


Figure 5

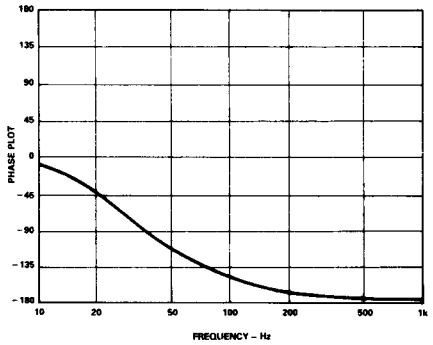


Figure 6

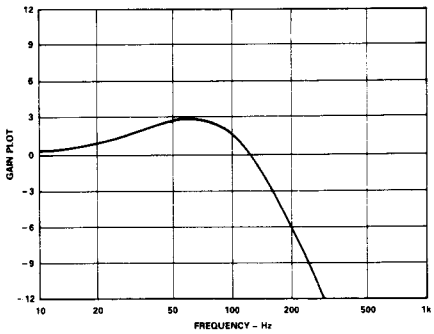


Figure 7

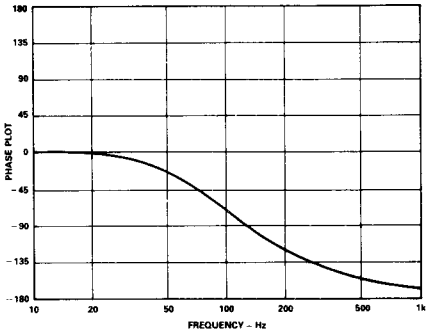


Figure 8

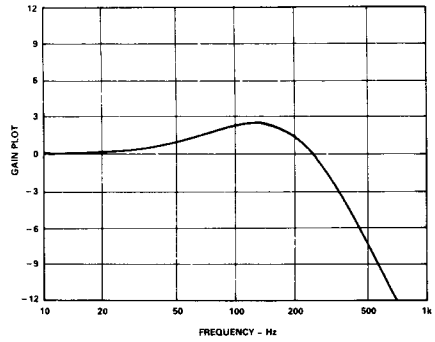


Figure 9

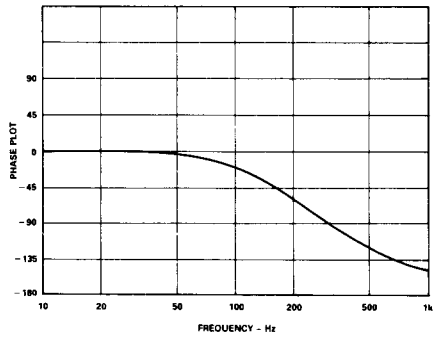


Figure 10

ACCELERATION ERROR

A tracking converter like the 1S20 employing a type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration. This additional error can be defined using the acceleration constant K_a of the converter.

$$K_a = \frac{\text{Input acceleration}}{\text{Error in output angle}}$$

The numerator and denominator have the same units. K_a does not define maximum acceleration only the error due to acceleration, maximum acceleration is in the region of 10 times the K_a figure (deg/sec^2).

An example using the K_a of the 1S60/560

Acceleration of 33 revolutions sec^{-2} with K_a = 713,000

Additional error = 1 arc-min

DYNAMIC ACCURACY VS. RESOLVER PHASE SHIFT

Most resolvers, particularly those of the brushless type, exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by:

$$\frac{\text{Shaft Speed (RPS)} \times \text{Phase Shift (DEGS)}}{\text{Reference Frequency}}$$

For example, for a phase shift of 20°, a shaft rotation of 22rps and a reference frequency of 5kHz, the converter will exhibit an additional error of:

$$\frac{20 \times 22}{5000} = 0.088°$$

This effect can be eliminated by putting a phase shift in the reference to the converter equivalent to the phase shift in the resolver.

PROCESSING FOR HIGH RELIABILITY

STANDARD PROCESSING

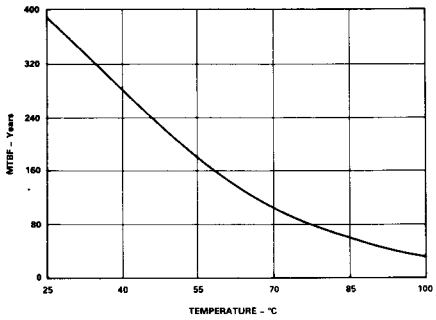
As part of the standard manufacturing procedure, all converters receive the following processing:

Process	Condition
1. Pre-Cap Visual Inspection	In-House Criteria
2. Burn-In	70°C
3. Constant Acceleration	5000G
4. Gross Leak Test	In-House Criteria
5. Final Electrical Test	Performed at 25°C

MEAN TIME BETWEEN FAILURES (MTBF)

The reliability of these products is very high due to the extensive use of custom chip circuitry. For details of MTBF figures under particular conditions please consult the factory.

The graph below shows the typical variation of MTBF with temperature for the 1S20, under ground benign environment.



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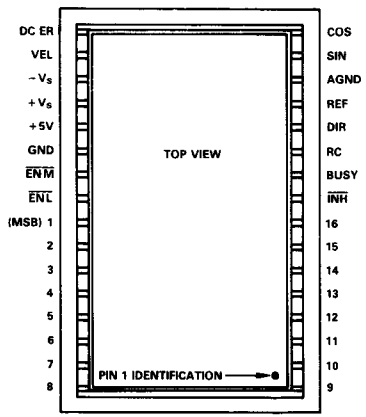
ABSOLUTE MAXIMUM INPUTS (with respect to GND)

$+V_S$[1]	0V to +17V dc
$-V_S$[1]	0V to −17V dc
+5V[2]	0V to +7.0V dc
Reference	±17V dc
Sine	±17V dc
Cosine	±17V dc
Any Logical Input	−0.4V to +5.5V dc

CAUTION:

1. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.
2. The +5 volt power supply must *never* go below GND potential.

PIN CONFIGURATION



OTHER PRODUCTS

IRDC1732–	Inductosyn™/Resolver to Digital Converter (Hybrid)
IPA1751–	Inductosyn™ Pre-Amplifier
OSC1754–	Power Oscillator
OSC1758–	Power Oscillator (Hybrid)
IPA1764–	Inductosyn™ Pre-Amplifier (Hybrid)
MCI1794–	3 Channel Inductosyn™/Resolver to Digital Converter (Multibus Compatible Card)

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ORDERING INFORMATION