

Preliminary W24256



32K × 8 CMOS STATIC RAM

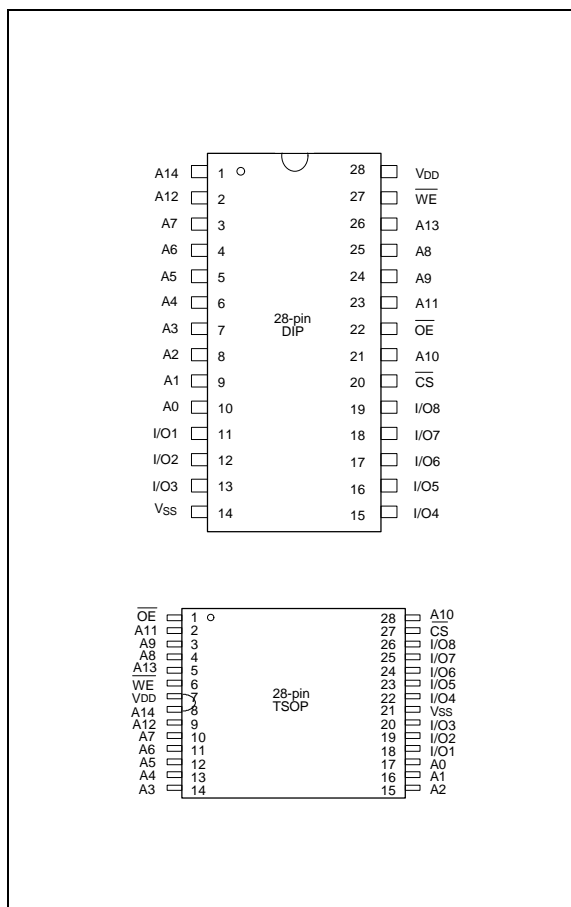
GENERAL DESCRIPTION

The W24256 is a normal speed, very low power CMOS static RAM organized as 32768 × 8 bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

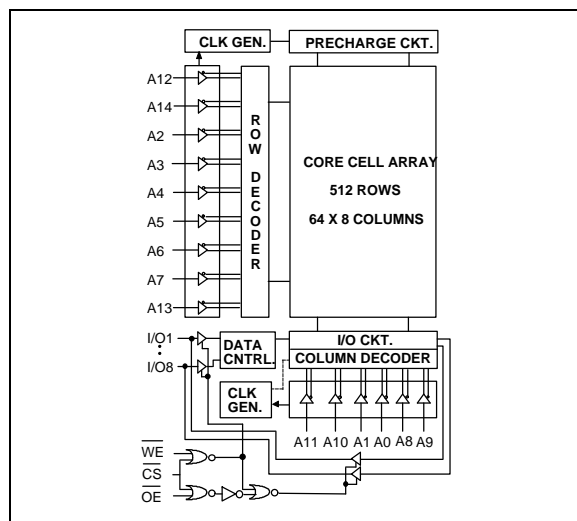
FEATURES

- Low power consumption:
 - Access time: 70 nS (max.)
 - Active :300 mW
 - Standby :250 μW
- Single 5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 2V (min.)
- Packaged in 28-pin 600 mil DIP, 330 mil SOP and standard type one TSOP (8 mm × 13.4 mm)

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A14	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
CS	Chip Select Input
WE	Write Enable Input
OE	Output Enable Input
V _{DD}	Power Supply
V _{SS}	Ground

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TRUTH TABLE

\overline{CS}	\overline{OE}	\overline{WE}	MODE	I/O1 - I/O8	V _{DD} CURRENT
H	X	X	Not Selected	High Z	ISB, ISB1
L	H	H	Output Disable	High Z	IDD
L	L	H	Read	Data Out	IDD
L	X	L	Write	Data In	IDD

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to V _{SS} Potential	-0.5 to +7.0	V
Input/Output to V _{SS} Potential	-0.5 to V _{DD} +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to 70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD} = 5V ±10%; V_{SS} = 0V; T_A = 0° C to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.*	MAX.	UNIT	
Input Low Voltage	V _{IL}	-	-0.5	-	+0.8	V	
Input High Voltage	V _{IH}	-	+2.2	-	V _{DD} +1	V	
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{DD}	-5	-	+5	μA	
Output Leakage Current	I _{LO}	V _{I/O} = V _{SS} to V _{DD} , \overline{CS} = V _{IH} (min.) or \overline{OE} = V _{IH} (min.) or \overline{WE} = V _{IL} (max.)	-5	-	+5	μA	
Output Low Voltage	V _{OL}	I _{OL} = +2.1 mA	-	-	0.4	V	
Output High Voltage	V _{OH}	I _{OH} = -1.0 mA	2.4	-	-	V	
Operating Power Supply Current	I _{DD}	\overline{CS} = V _{IL} (max.), I/O = 0 mA, Cycle = min, Duty = 100 %	-	-	60	mA	
Standby Power Supply Current	ISB	\overline{CS} = V _{IH} (min.), Cycle = min. Duty = 100%	-	-	3	mA	
	ISB1	$\overline{CS} \geq V_{DD} - 0.2V$	L	-	-	100	μA
			LL	-	-	50	μA

Note: Typical parameter is measured under ambient temperature T_A = 25° C and V_{DD} = 5V.

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CAPACITANCE

(V_{DD} = 5V, T_A = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C _{IN}	V _{IN} = 0V	6	pF
Input/Output Capacitance	C _{I/O}	V _{OUT} = 0V	8	pF

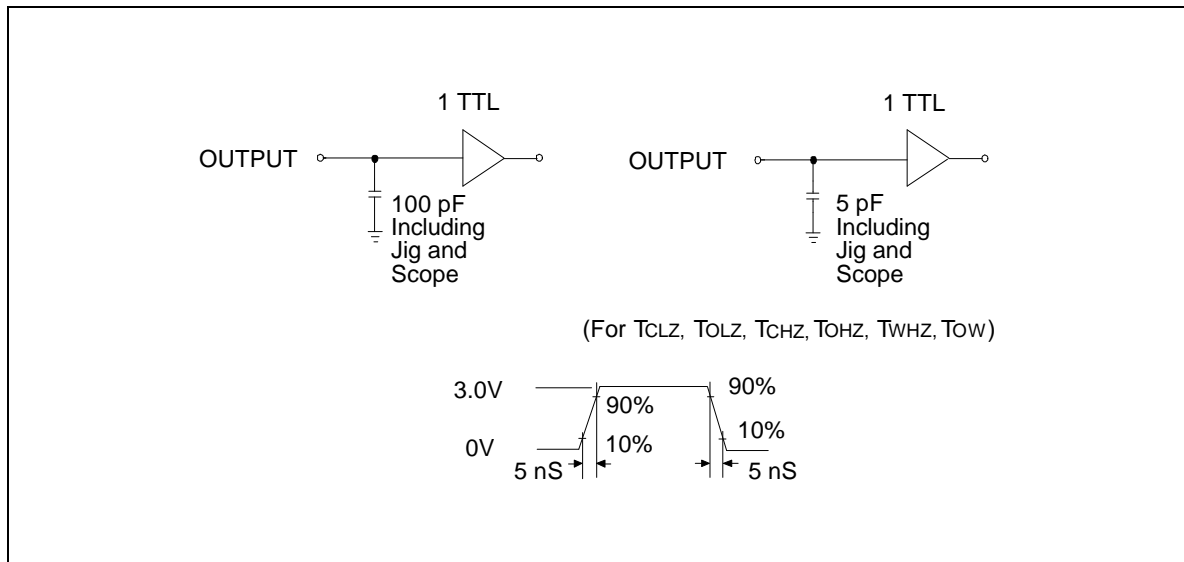
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	See the drawing below

AC TEST LOADS AND WAVEFORM



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AC Characteristics, continued

(V_{DD} = 5V ±10%; V_{SS} = 0V; T_A = 0° C to 70° C)

Read Cycle

PARAMETER	SYM.	W24256-70L/LL		UNIT
		MIN.	MAX.	
Read Cycle Time	TRC	70	-	nS
Address Access Time	TAA	-	70	nS
Chip Select Access Time	TACS	-	70	nS
Output Enable to Output Valid	TAOE	-	30	nS
Chip Selection to Output in Low Z	TCLZ*	5	-	nS
Output Enable to Output in Low Z	TOLZ*	5	-	nS
Chip Deselection to Output in High Z	TCHZ*	-	20	nS
Output Disable to Output in High Z	TOHZ*	-	20	nS
Output Hold from Address Change	TOH	3	-	nS

* These parameters are sampled but not 100% tested

Write Cycle

PARAMETER	SYM.	W24256-70L/LL		UNIT
		MIN.	MAX.	
Write Cycle Time	TWC	70	-	nS
Chip Selection to End of Write	TCW	70	-	nS
Address Valid to End of Write	TAW	70	-	nS
Address Setup Time	TAS	0	-	nS
Write Pulse Width	TWP	50	-	nS
Write Recovery Time	$\overline{CS}, \overline{WE}$ TWR	0	-	nS
Data Valid to End of Write	TDW	30	-	nS
Data Hold from End of Write	TDH	0	-	nS
Write to Output in High Z	TWHZ*	-	25	nS
Output Disable to Output in High Z	TOHZ*	-	30	nS
Output Active from End of Write	TOW	5	-	nS

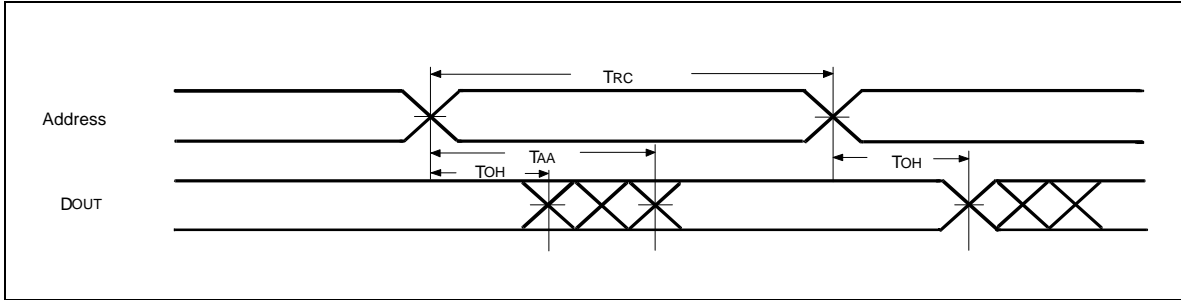
* These parameters are sampled but not 100% tested



TIMING WAVEFORMS

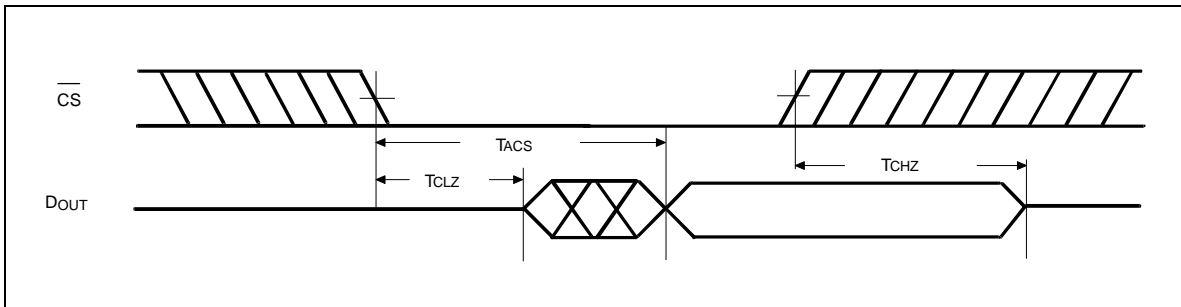
Read Cycle 1

(Address Controlled)



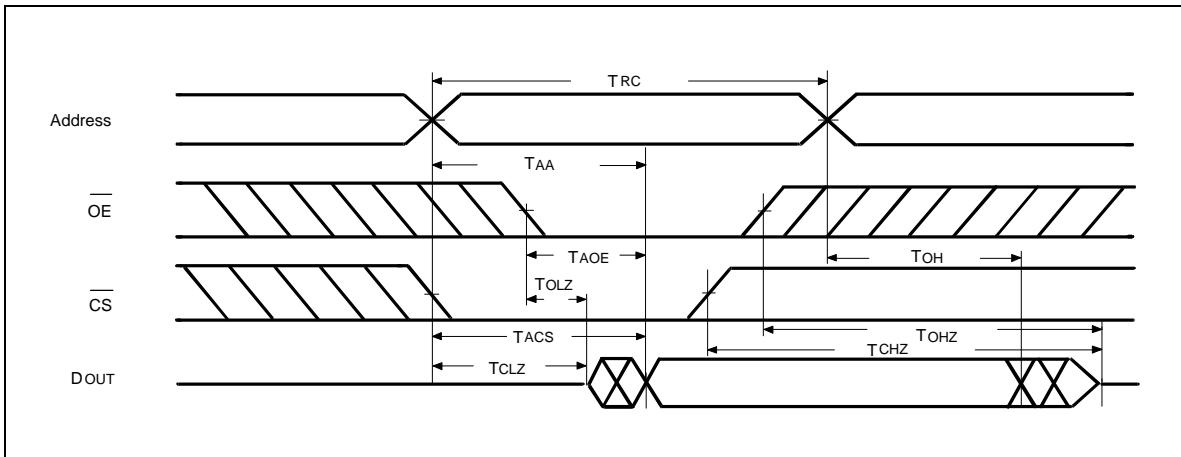
Read Cycle 2

(Chip Select Controlled)



Read Cycle 3

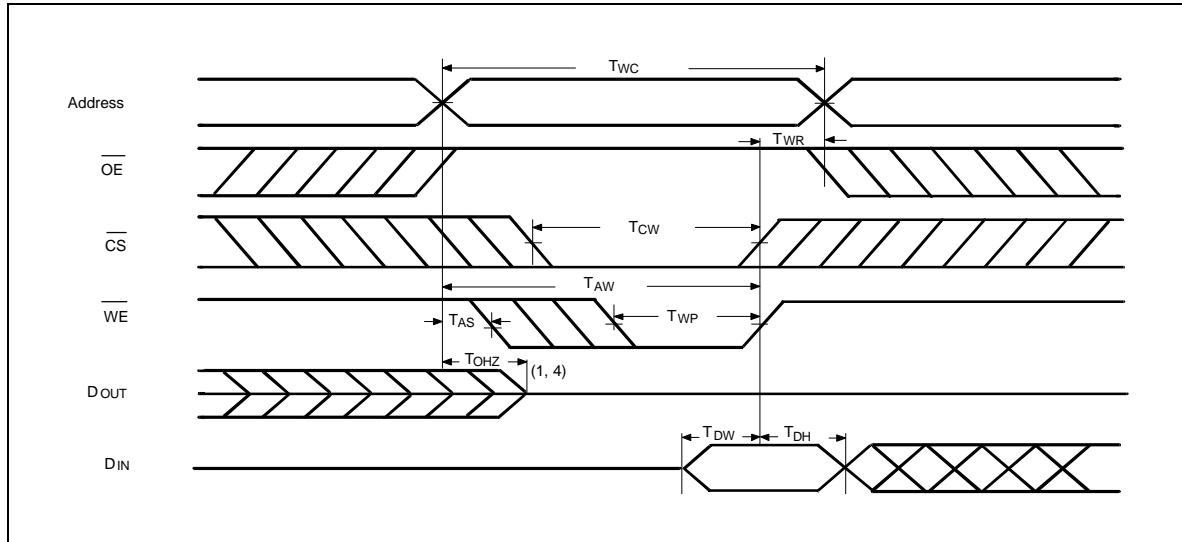
(Output Enable Controlled)





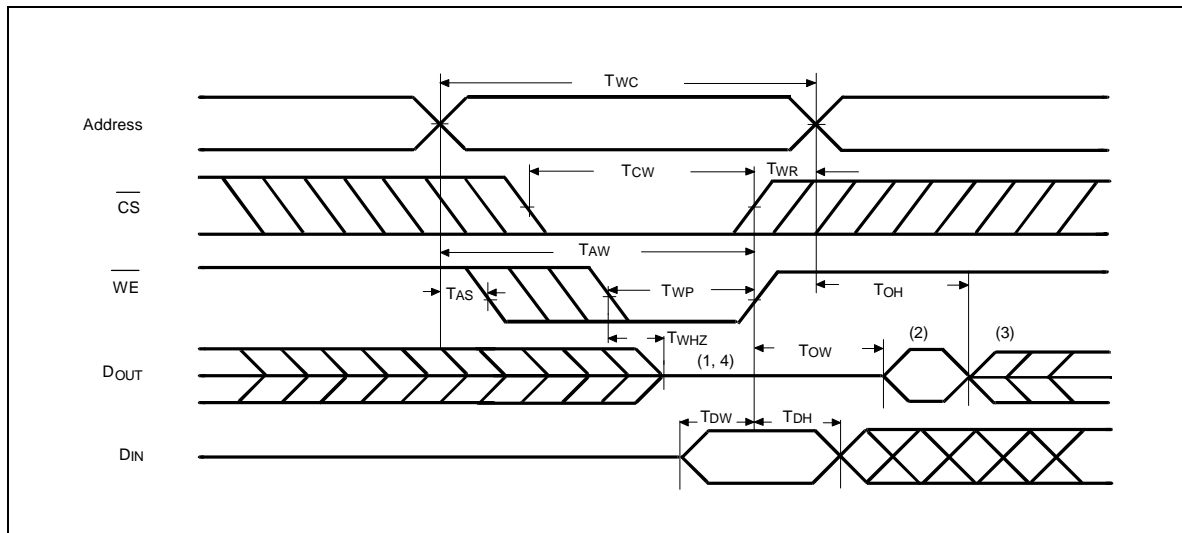
Timing Waveforms, continued

Write Cycle 1



Write Cycle 2

($\overline{OE} = V_{IL}$ Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with $C_L = 5$ pF. This parameter is guaranteed but not 100% tested.



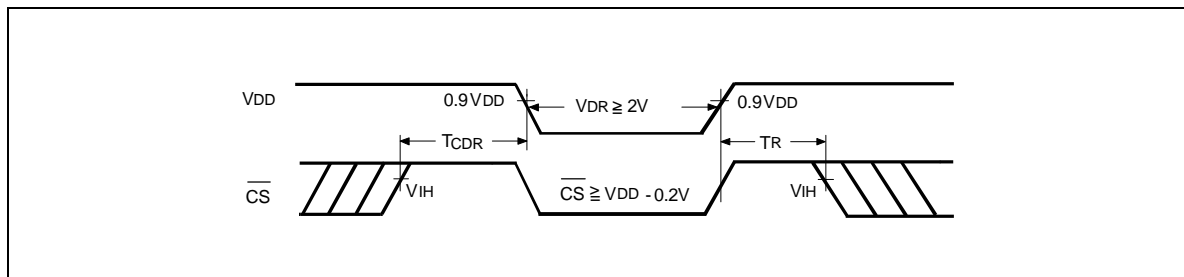
DATA RETENTION CHARACTERISTICS

(T_A = 0° C to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VDD for Data Retention	VDR	$\overline{CS} \geq V_{DD} - 0.2V$	2.0	-	5.5	V
Data Retention Current	I _{DDDR}	$\overline{CS} \geq V_{DD} - 0.2V, V_{DD} = 3V$	-	-	20	μA
Chip Deselect to Data Retention Time	T _{CDR}	See data retention waveform	0	-	-	nS
Operation Recovery Time	TR		TRC*	-	-	nS

* Read Cycle Time

DATA RETENTION WAVEFORM



ORDERING INFORMATION

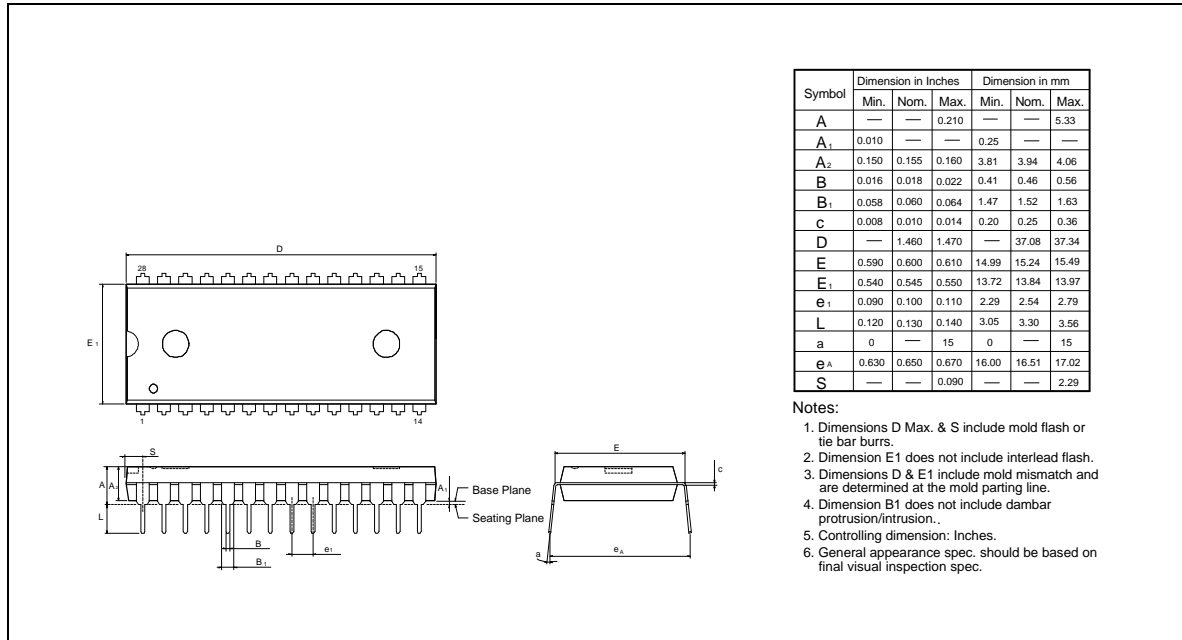
PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W24256-70L	70	60	100	600 mil DIP
W24256-70LL	70	60	50	600 mil DIP
W24256S-70L	70	60	100	330 mil SOP
W24256S-70LL	70	60	50	330 mil SOP
W24256Q-70L	70	60	100	Standard type one TSOP
W24256Q-70LL	70	60	50	Standard type one TSOP

Notes:

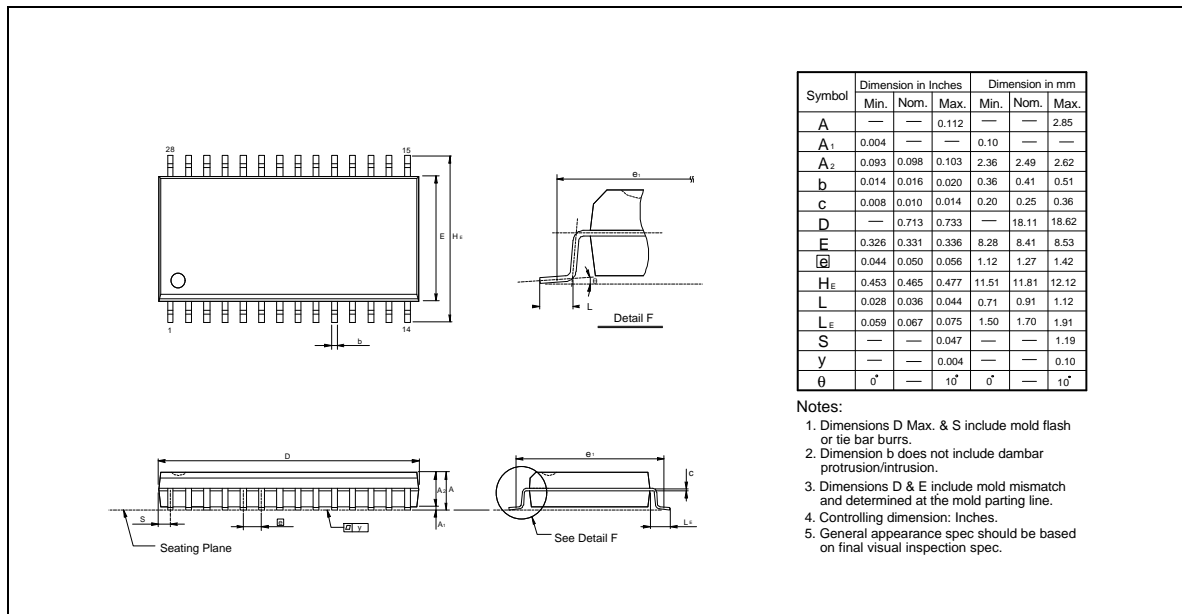
- Winbond reserves the right to make changes to its products without prior notice.
- Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

28-pin P-DIP

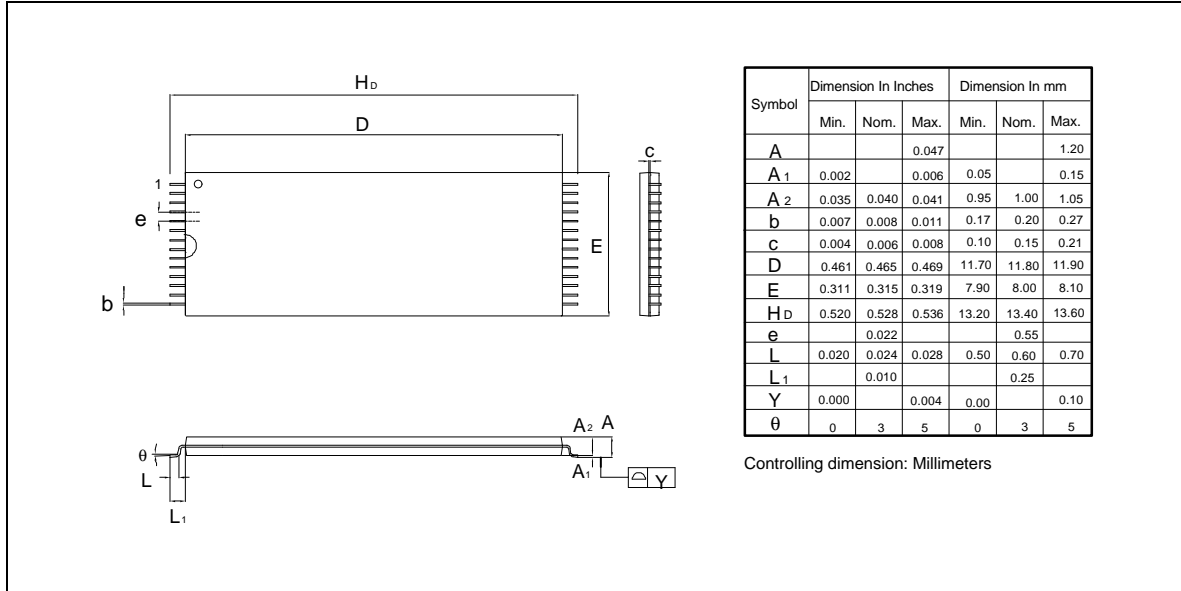


28-pin SOP Wide Body



Package Dimensions, continued

28-pin Standard Type One TSOP



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VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Oct. 1999	-	Initial issued



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Note: All data and specifications are subject to change without notice.