

E0C6281

4-bit Single Chip Microcomputer



- Core CPU Architecture
- SVD Circuit/Comparator
- Melody Circuit

DESCRIPTION

The E0C6281 is an advanced single-chip CMOS 4-bit microcomputer consisting of the E0C6200 CMOS 4-bit core CPU. It also contains the ROM, RAM, LCD driver, time base counter and melody generation circuit. The E0C6281 provides an excellent solution for low-power consumption systems with clock functions.

FEATURES

- CMOS LSI 4-bit parallel processing
- Clock 32.768kHz (Typ.)
- Instruction set 100 instructions
- Instruction cycle time 153μsec, 214μsec or 366μsec (depending on instruction)
- ROM capacity 1,024 × 12 bits
- RAM capacity 96 × 4 bits
- Input port 5 bits
(pull-down resistors are available by mask option)
- Output port 4 bits (general purpose port)
2 bits (for melody output): MO, \overline{MO} (also used as the external CR connecting terminal for envelope)
1 bit (for lamp output)
1 bit (for clock output: frequency can be selected from 256Hz through 32kHz by mask option)
- I/O port 4 bits
- LCD driver 26 segments × 3 commons, 1/3 duty or 4 commons, 1/4 duty
- Built-in stopwatch timer
- Built-in supply voltage detection (SVD) circuit
- Built-in comparator 1 ch.
- Built-in melody generation circuit Equivalent to SVM7500 (80-word melody ROM is built in)
- Interrupts External : Input interrupt 2 lines
Internal : Timer interrupt 1 line
 Stopwatch interrupt 1 line
 Melody completion interrupt 1 line
- Supply voltage 1.5V/3.0V (Minimum operating voltage: 0.9V/1.8V)
- Current consumption E0C6281/62L81 HALT mode : 1.0μA (Typ.)
 OPERATING mode : 2.5μA (Typ.)
 E0C62A81/62B81 HALT mode : 5.5μA (Typ.)
 OPERATING mode : 7.2μA (Typ.)
- Package QFP6-64pin-S1 (plastic)
Die form

LINE UP

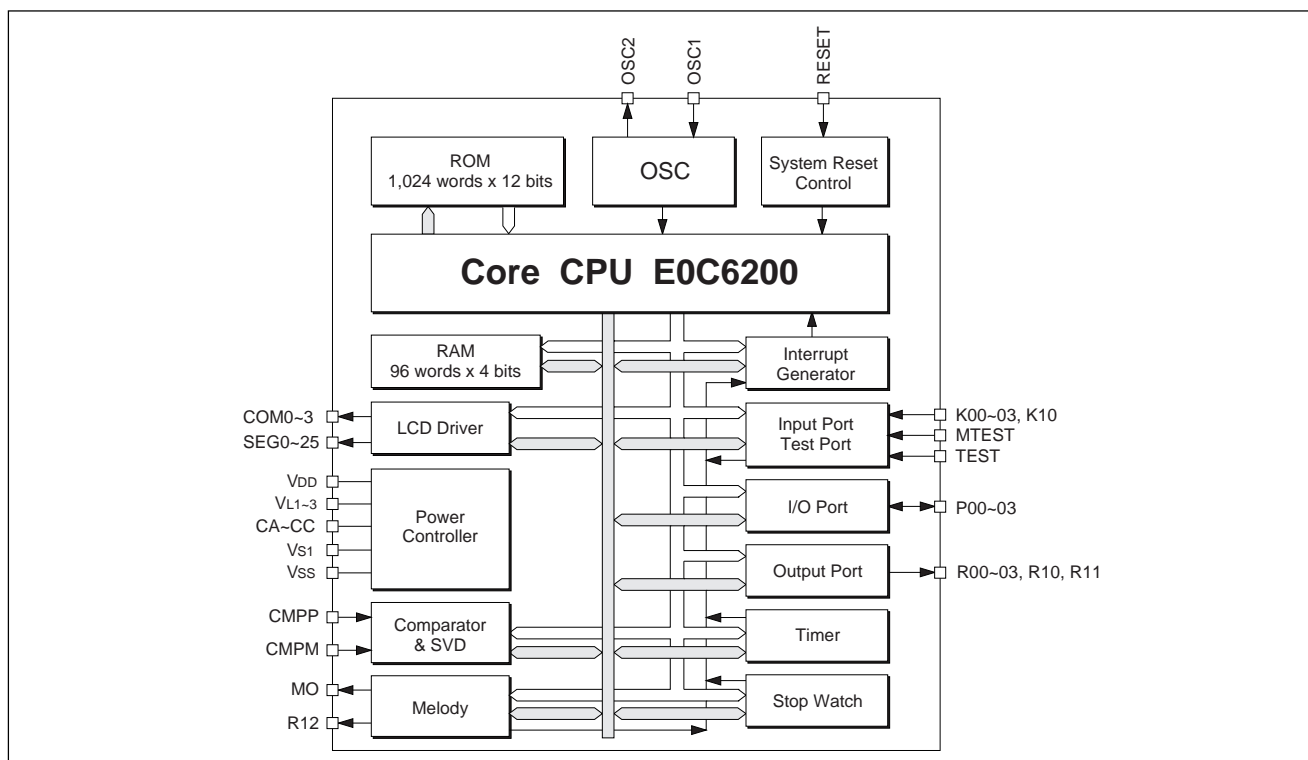
Model	Supply voltage	Clock
E0C6281	3.0V (1.8V to 3.5V)	32kHz (Crystal oscillation)
E0C62L81	1.5V (0.9V to 3.5V)	32kHz (Crystal oscillation)
E0C62A81	3.0V (1.8V to 3.5V)	32kHz (CR oscillation)
E0C62B81	1.5V (0.9V to 3.5V)	32kHz (CR oscillation)

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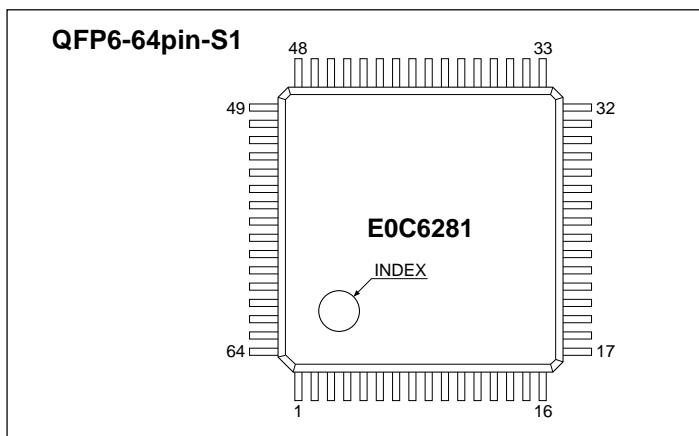
< Detail of Melody Function >

- Melody memory capacity 80 words
- Interval memory capacity 16 words (including one pause note)
- Interval generated C3 to C6#, or C4 to C7# (mask option)
- Useful note 8 (from sixteenth note to a half note)
- Tempo Basic: Select 2 tempos out of 16 tempos (30 to 480) (mask option)
(The tempo selected is changed by the software control.)
The tempo having 8 times, 16 times or 32 times the basic tempo is available by software.
- Envelope External CR is required. (not available for the piezoelectric direct drive type)
- Piezoelectric direct drive Envelope not available
- Melody control function (1) 1 music: Melody start address is controlled by the software.
(2) Repeating: The address is controlled by the software when repeated.
(3) Forcible music change: The new music address is designated with the software while a music is now played.

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	COM1	17	SEG12	33	P01	49	R00
2	COM2	18	TEST	34	P02	50	R01
3	COM3	19	SEG13	35	P03	51	R02
4	SEG25	20	SEG14	36	CMPM	52	R03
5	SEG0	21	SEG15	37	CMPP	53	Vs1
6	SEG1	22	SEG16	38	MTEST	54	VDD
7	SEG2	23	SEG17	39	RESET	55	Vss
8	SEG3	24	SEG18	40	K00	56	OSC2
9	SEG4	25	SEG19	41	K01	57	OSC1
10	SEG5	26	SEG20	42	K02	58	VL3
11	SEG6	27	SEG21	43	K03	59	VL2
12	SEG7	28	SEG22	44	K10	60	VL1
13	SEG8	29	SEG23	45	R10	61	CC
14	SEG9	30	SEG24	46	R11	62	CB
15	SEG10	31	N.C.	47	R12	63	CA
16	SEG11	32	P00	48	MO	64	COM0

N.C. = No Connection

■ PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V _{DD}	54	I	Power source (+) terminal
V _{SS}	55	I	Power source (-) terminal
V _{S1}	53	O	Oscillation and internal logic system regulated voltage output terminal
V _{L1}	60	O	LCD system regulated voltage output terminal (approx. -1.05 V)
V _{L2}	59	O	LCD system booster output terminal (V _{L1} x 2)
V _{L3}	58	O	LCD system booster output terminal (V _{L1} x 3)
CA-CC	61-63	-	Booster capacitor connecting terminal
OSC1	57	I	Crystal or CR oscillation input terminal
OSC2	56	O	Crystal or CR oscillation output terminal
K00-K03, K10	40-44	I	Input terminal
P00-P03	32-35	I/O	I/O terminal
R00-R03	49-52	O	Output terminal
R10	45	O	Output terminal (FOUT output available by mask option)
R11	46	O	Output terminal
R12	47	O	Output terminal (Melody inverted output and envelope function available by mask option)
MO	48	O	Melody signal output terminal
CMPP	37	I	Analog comparator non-inverted input terminal
CMPM	36	I	Analog comparator inverted input terminal
SEG0-25	4-17, 19-30	O	LCD segment output terminal (Convertible to DC output by mask option)
COM0-3	64, 1-3	O	LCD common output terminal
RESET	39	I	Initial reset input terminal
TEST	18	I	Test input terminal
MTEST	38	I	Melody test input terminal

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V _{SS}	-5.0 to 0.5	V
Input voltage (1)	V _I	V _{SS} - 0.3 to 0.5	V
Input voltage (2)	V _{Iosc}	V _{SS} - 0.3 to 0.5	V
Permissible total output current *1	∑I _{vss}	10	mA
Operating temperature	T _{opr}	-20 to 70	°C
Storage temperature	T _{stg}	-65 to 150	°C
Soldering temperature / Time	T _{sol}	260°C, 10sec (lead section)	-
Permissible dissipation *2	P _D	250	mW

*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is drawn in).

*2: In case of plastic package (QFP6-64pin).

● Recommended Operating Conditions

E0C6281/62A81

(T_a=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V _{SS}	V _{DD} =0V	-3.5	-3.0	-1.8	V
Oscillation frequency	f _{osc}		-	32.768	-	kHz

E0C62L81/62B81

(T_a=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V _{SS}	V _{DD} =0V	-3.5	-1.5	-1.1	V
		V _{DD} =0V, With software control *1	-3.5	-1.5	-0.9 *2	V
		V _{DD} =0V, When the analog comparator is used	-3.5	-1.5	-1.3	V
Oscillation frequency	f _{osc}		-	32.768	-	kHz

*1: When switching to heavy load protection mode. The SVD circuit and analog voltage comparator are turned OFF.

*2: The possibility of LCD panel display differs depending on the characteristics of the LCD panel.

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● DC Characteristics

E0C6281/62A81

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{osc}=32.768kHz, T_a=25°C, V_{S1}/V_{L1}-V_{L3} are internal voltage, C₁-C₆=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	V _{IH1}	K00-K03, K10, P00-P03 MTEST	0.2•V _{SS}		0	V
High level input voltage (2)	V _{IH2}	RESET, TEST	0.10•V _{SS}		0	V
Low level input voltage (1)	V _{IL1}	K00-K03, K10, P00-P03 MTEST	V _{SS}		0.8•V _{SS}	V
Low level input voltage (2)	V _{IL2}	RESET, TEST	V _{SS}		0.90•V _{SS}	V
High level input current (1)	I _{IH1}	V _{IH1} =0V No pull down resistor	0		0.5	μA
High level input current (2)	I _{IH2}	V _{IH2} =0V With pull down resistor	5		16	μA
High level input current (3)	I _{IH3}	V _{IH3} =0V With pull down resistor	30		100	μA
Low level input current	I _{IL}	V _{IL} =V _{SS}	-0.5		0	μA
High level output current (1)	I _{OH1}	V _{OH1} =0.1•V _{SS} R11			-1.0	mA
High level output current (2)	I _{OH2}	V _{OH2} =0.1•V _{SS} R00-R03, R10, P00-P03			-1.0	mA
High level output current (3)	I _{OH3}	V _{OH3} =0.1•V _{SS} MO, R12			-2.0	mA
Low level output current (1)	I _{OL1}	V _{OL1} =0.9•V _{SS} R11	3.0			mA
Low level output current (2)	I _{OL2}	V _{OL2} =0.9•V _{SS} R00-R03, R10, P00-P03	3.0			mA
Low level output current (3)	I _{OL3}	V _{OL3} =0.9•V _{SS} MO, R12	4.5			mA
Common output current	I _{OH4}	V _{OH4} =-0.05V COM0-COM3			-3	μA
	I _{OL4}	V _{OL4} =V _{L3} +0.05V	3			μA
Segment output current (during LCD output)	I _{OH5}	V _{OH5} =-0.05V SEG0-SEG25			-3	μA
	I _{OL5}	V _{OL5} =V _{L3} +0.05V	3			μA
Segment output current (during DC output)	I _{OH6}	V _{OH6} =0.1•V _{SS} SEG0-SEG25			-300	μA
	I _{OL6}	V _{OL6} =0.9•V _{SS}	300			μA

E0C62L81/62B81

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{osc}=32.768kHz, T_a=25°C, V_{S1}/V_{L1}-V_{L3} are internal voltage, C₁-C₆=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	V _{IH1}	K00-K03, K10, P00-P03 MTEST	0.2•V _{SS}		0	V
High level input voltage (2)	V _{IH2}	RESET, TEST	0.10•V _{SS}		0	V
Low level input voltage (1)	V _{IL1}	K00-K03, K10, P00-P03 MTEST	V _{SS}		0.8•V _{SS}	V
Low level input voltage (2)	V _{IL2}	RESET, TEST	V _{SS}		0.90•V _{SS}	V
High level input current (1)	I _{IH1}	V _{IH1} =0V No pull down resistor	0		0.5	μA
High level input current (2)	I _{IH2}	V _{IH2} =0V With pull down resistor	2.0		10	μA
High level input current (3)	I _{IH3}	V _{IH3} =0V With pull down resistor	9.0		60	μA
Low level input current	I _{IL}	V _{IL} =V _{SS}	-0.5		0	μA
High level output current (1)	I _{OH1}	V _{OH1} =0.1•V _{SS} R11			-450	μA
High level output current (2)	I _{OH2}	V _{OH2} =0.1•V _{SS} R00-R03, R10, P00-P03			-200	μA
High level output current (3)	I _{OH3}	V _{OH3} =0.1•V _{SS} MO, R12			-0.8	mA
High level output current (4)	I _{OH4}	V _{OH4} =0.1•V _{SS} When envelope is used (R12=Normal H level)			-0.4	mA
Low level output current (1)	I _{OL1}	V _{OL1} =0.9•V _{SS} R11	1,300			μA
Low level output current (2)	I _{OL2}	V _{OL2} =0.9•V _{SS} R00-R03, R10, P00-P03	700			μA
Low level output current (3)	I _{OL3}	V _{OL3} =0.9•V _{SS} MO, R12	1.5			mA
Low level output current (4)	I _{OL4}	V _{OL4} =0.9•V _{SS} When envelope is used (R12=Normal L level)	750			μA
Common output current	I _{OH5}	V _{OH5} =-0.05V COM0-COM3			-3	μA
	I _{OL5}	V _{OL5} =V _{L3} +0.05V	3			μA
Segment output current (during LCD output)	I _{OH6}	V _{OH6} =-0.05V SEG0-SEG25			-3	μA
	I _{OL6}	V _{OL6} =V _{L3} +0.05V	3			μA
Segment output current (during DC output)	I _{OH7}	V _{OH7} =0.1•V _{SS} SEG0-SEG25			-100	μA
	I _{OL7}	V _{OL7} =0.9•V _{SS}	130			μA

● Analog Circuit Characteristics and Current Consumption

E0C6281 (Normal Operating Mode)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, $f_{OSC}=32.768kHz$, $T_a=25^{\circ}C$, $C_G=25pF$, $V_{S1}/V_{L1}-V_{L3}$ are internal voltage, $C1-C6=0.1\mu F$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect $1M\Omega$ load resistor between V_{DD} and V_{L1} (without panel load)	-1.15	-1.05	-0.95	V
	V_{L2}	Connect $1M\Omega$ load resistor between V_{DD} and V_{L2} (without panel load)	$2 \cdot V_{L1}$ -0.1		$2 \cdot V_{L1}$ $\times 0.9$	V
	V_{L3}	Connect $1M\Omega$ load resistor between V_{DD} and V_{L3} (without panel load)	$3 \cdot V_{L1}$ -0.1		$3 \cdot V_{L1}$ $\times 0.9$	V
SVD voltage	V_{SVD}		-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}				100	μS
Analog comparator input voltage	V_{IP}	Noninverted input (CMPP)	$V_{SS}+0.3$		$V_{DD}-0.9$	V
	V_{IM}	Inverted input (CMPM)				
Analog comparator offset voltage	V_{OF}				10	mV
Analog comparator response time	t_{CMP}	$V_{IP}=-1.5V$, $V_{IM}=V_{IP}\pm 15mV$			3	mS
Current consumption	IOP	During HALT		1.0	2.5	μA
		During operation *1	Without panel load	2.5	5.0	μA

*1: The SVD circuit and analog voltage comparator are turned OFF.

E0C6281 (Heavy Load Protection Mode)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, $f_{OSC}=32.768kHz$, $T_a=25^{\circ}C$, $C_G=25pF$, $V_{S1}/V_{L1}-V_{L3}$ are internal voltage, $C1-C6=0.1\mu F$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect $1M\Omega$ load resistor between V_{DD} and V_{L1} (without panel load)	-1.15	-1.05	-0.95	V
	V_{L2}	Connect $1M\Omega$ load resistor between V_{DD} and V_{L2} (without panel load)	$2 \cdot V_{L1}$ -0.1		$2 \cdot V_{L1}$ $\times 0.85$	V
	V_{L3}	Connect $1M\Omega$ load resistor between V_{DD} and V_{L3} (without panel load)	$3 \cdot V_{L1}$ -0.1		$3 \cdot V_{L1}$ $\times 0.85$	V
SVD voltage	V_{SVD}		-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}				100	μS
Analog comparator input voltage	V_{IP}	Noninverted input (CMPP)	$V_{SS}+0.3$		$V_{DD}-0.9$	V
	V_{IM}	Inverted input (CMPM)				
Analog comparator offset voltage	V_{OF}				10	mV
Analog comparator response time	t_{CMP}	$V_{IP}=-1.5V$, $V_{IM}=V_{IP}\pm 15mV$			3	mS
Current consumption	IOP	During HALT		2.0	5.5	μA
		During operation *1	Without panel load	5.5	10.0	μA

*1: The SVD circuit and analog voltage comparator are turned OFF.

E0C62L81 (Normal Operating Mode)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-1.5V$, $f_{OSC}=32.768kHz$, $T_a=25^{\circ}C$, $C_G=25pF$, $V_{S1}/V_{L1}-V_{L3}$ are internal voltage, $C1-C6=0.1\mu F$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect $1M\Omega$ load resistor between V_{DD} and V_{L1} (without panel load)	-1.15	-1.05	-0.95	V
	V_{L2}	Connect $1M\Omega$ load resistor between V_{DD} and V_{L2} (without panel load)	$2 \cdot V_{L1}$ -0.1		$2 \cdot V_{L1}$ $\times 0.9$	V
	V_{L3}	Connect $1M\Omega$ load resistor between V_{DD} and V_{L3} (without panel load)	$3 \cdot V_{L1}$ -0.1		$3 \cdot V_{L1}$ $\times 0.9$	V
SVD voltage	V_{SVD}		-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}				100	μS
Analog comparator input voltage	V_{IP}	Noninverted input (CMPP)	$V_{SS}+0.3$		$V_{DD}-0.9$	V
	V_{IM}	Inverted input (CMPM)				
Analog comparator offset voltage	V_{OF}				20	mV
Analog comparator response time	t_{CMP}	$V_{IP}=-1.1V$, $V_{IM}=V_{IP}\pm 30mV$			3	mS
Current consumption	IOP	During HALT		1.0	2.5	μA
		During operation *1	Without panel load	2.5	5.0	μA

*1: The SVD circuit and analog voltage comparator are turned OFF.

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E0C62L81 (Heavy Load Protection Mode)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-1.5V$, $f_{osc}=32.768kHz$, $T_a=25^\circ C$, $C_G=25pF$, $V_{S1}/V_{L1}-V_{L3}$ are internal voltage, $C1-C6=0.1\mu F$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	VL1	Connect 1M Ω load resistor between VDD and VL1 (without panel load)	-1.15	-1.05	-0.95	V
	VL2	Connect 1M Ω load resistor between VDD and VL2 (without panel load)	2•VL1 -0.1		2•VL1 ×0.85	V
	VL3	Connect 1M Ω load resistor between VDD and VL3 (without panel load)	3•VL1 -0.1		3•VL1 ×0.85	V
SVD voltage	VSVD		-1.30	-1.20	-1.10	V
SVD circuit response time	tSVD				100	μS
Analog comparator input voltage	VIP	Noninverted input (CMPP)	VSS+0.3		VDD-0.9	V
	VIM	Inverted input (CMPM)				
Analog comparator offset voltage	VOF				20	mV
Analog comparator response time	tCMP	VIP=-1.1V, VIM=VIP±30mV			3	mS
Current consumption	IOP	During HALT	Without panel load		2.0	5.5
		During operation *1				

*1: The SVD circuit and analog voltage comparator are turned OFF.

E0C62A81 (Normal Operating Mode)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, $f_{osc}=32.768kHz$, $T_a=25^\circ C$, $C_G=25pF$, $V_{S1}/V_{L1}-V_{L3}$ are internal voltage, $C1-C6=0.1\mu F$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	VL1	Connect 1M Ω load resistor between VDD and VL1 (without panel load)	-1.15	-1.05	-0.95	V
	VL2	Connect 1M Ω load resistor between VDD and VL2 (without panel load)	2•VL1 -0.1		2•VL1 ×0.9	V
	VL3	Connect 1M Ω load resistor between VDD and VL3 (without panel load)	3•VL1 -0.1		3•VL1 ×0.9	V
SVD voltage	VSVD		-2.55	-2.40	-2.25	V
SVD circuit response time	tSVD				100	μS
Analog comparator input voltage	VIP	Noninverted input (CMPP)	VSS+0.3		VDD-0.9	V
	VIM	Inverted input (CMPM)				
Analog comparator offset voltage	VOF				10	mV
Analog comparator response time	tCMP	VIP=-1.5V, VIM=VIP±15mV			3	mS
Current consumption	IOP	During HALT	Without panel load		5.5	10.0
		During operation *1				

*1: The SVD circuit and analog voltage comparator are turned OFF.

E0C62A81 (Heavy Load Protection Mode)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, $f_{osc}=32.768kHz$, $T_a=25^\circ C$, $C_G=25pF$, $V_{S1}/V_{L1}-V_{L3}$ are internal voltage, $C1-C6=0.1\mu F$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	VL1	Connect 1M Ω load resistor between VDD and VL1 (without panel load)	-1.15	-1.05	-0.95	V
	VL2	Connect 1M Ω load resistor between VDD and VL2 (without panel load)	2•VL1 -0.1		2•VL1 ×0.85	V
	VL3	Connect 1M Ω load resistor between VDD and VL3 (without panel load)	3•VL1 -0.1		3•VL1 ×0.85	V
SVD voltage	VSVD		-2.55	-2.40	-2.25	V
SVD circuit response time	tSVD				100	μS
Analog comparator input voltage	VIP	Noninverted input (CMPP)	VSS+0.3		VDD-0.9	V
	VIM	Inverted input (CMPM)				
Analog comparator offset voltage	VOF				10	mV
Analog comparator response time	tCMP	VIP=-1.5V, VIM=VIP±15mV			3	mS
Current consumption	IOP	During HALT	Without panel load		11.0	20.0
		During operation *1				

*1: The SVD circuit and analog voltage comparator are turned OFF.

E0C62B81 (Normal Operating Mode)(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-1.5V$, $f_{osc}=32.768kHz$, $T_a=25^{\circ}C$, $C_G=25pF$, $V_{S1}/V_{L1}-V_{L3}$ are internal voltage, $C1-C6=0.1\mu F$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1M Ω load resistor between V_{DD} and V_{L1} (without panel load)	-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1M Ω load resistor between V_{DD} and V_{L2} (without panel load)	$2 \cdot V_{L1}$ -0.1		$2 \cdot V_{L1}$ $\times 0.9$	V
	V_{L3}	Connect 1M Ω load resistor between V_{DD} and V_{L3} (without panel load)	$3 \cdot V_{L1}$ -0.1		$3 \cdot V_{L1}$ $\times 0.9$	V
SVD voltage	V_{SVD}		-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}				100	μS
Analog comparator input voltage	V_{IP}	Noninverted input (CMPP)	$V_{SS}+0.3$		$V_{DD}-0.9$	V
	V_{IM}	Inverted input (CMPM)				
Analog comparator offset voltage	V_{OF}				20	mV
Analog comparator response time	t_{CMP}	$V_{IP}=-1.1V$, $V_{IM}=V_{IP} \pm 30mV$			3	mS
Current consumption	I_{OP}	During HALT	Without panel load			μA
		During operation *1				
						μA
				7.2	12.0	μA

*1: The SVD circuit and analog voltage comparator are turned OFF.

E0C62B81 (Heavy Load Protection Mode)(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-1.5V$, $f_{osc}=32.768kHz$, $T_a=25^{\circ}C$, $C_G=25pF$, $V_{S1}/V_{L1}-V_{L3}$ are internal voltage, $C1-C6=0.1\mu F$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1M Ω load resistor between V_{DD} and V_{L1} (without panel load)	-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1M Ω load resistor between V_{DD} and V_{L2} (without panel load)	$2 \cdot V_{L1}$ -0.1		$2 \cdot V_{L1}$ $\times 0.85$	V
	V_{L3}	Connect 1M Ω load resistor between V_{DD} and V_{L3} (without panel load)	$3 \cdot V_{L1}$ -0.1		$3 \cdot V_{L1}$ $\times 0.85$	V
SVD voltage	V_{SVD}		-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}				100	μS
Analog comparator input voltage	V_{IP}	Noninverted input (CMPP)	$V_{SS}+0.3$		$V_{DD}-0.9$	V
	V_{IM}	Inverted input (CMPM)				
Analog comparator offset voltage	V_{OF}				20	mV
Analog comparator response time	t_{CMP}	$V_{IP}=-1.1V$, $V_{IM}=V_{IP} \pm 30mV$			3	mS
Current consumption	I_{OP}	During HALT	Without panel load			μA
		During operation *1				
						μA
				15.0	25.0	μA

*1: The SVD circuit and analog voltage comparator are turned OFF.

E0C6281

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

E0C6281 (Crystal)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, Crystal: C-002R ($C_I=35k\Omega$), $C_G=25pF$, C_D =built-in, $T_a=25^\circ C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	$t_{sta} \leq 3sec$ (Vss)	-1.8			V
Oscillation stop voltage	Vstp	$t_{stp} \leq 10sec$ (Vss)	-1.8			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS}=-1.8$ to $-3.5V$			5	ppm
Frequency/IC deviation	$\partial f/\partial IC$		-10		10	ppm
Frequency adjustment range	$\partial f/\partial C_G$	$C_G=5$ to $25pF$	40			ppm
Harmonic oscillation start voltage	Vhho	(Vss)			-3.5	V
Permitted leak resistance	Rleak	Between OSC1 and V_{DD} , V_{SS}	200			M Ω

E0C62L81 (Crystal)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-1.5V$, Crystal: C-002R ($C_I=35k\Omega$), $C_G=25pF$, C_D =built-in, $T_a=25^\circ C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	$t_{sta} \leq 3sec$ (Vss)	-1.1			V
Oscillation stop voltage	Vstp	$t_{stp} \leq 10sec$ (Vss)	-1.1(-0.9)*1			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS}=-1.1$ to $-3.5V$ (-0.9) *1			5	ppm
Frequency/IC deviation	$\partial f/\partial IC$		-10		10	ppm
Frequency adjustment range	$\partial f/\partial C_G$	$C_G=5$ to $25pF$	40			ppm
Harmonic oscillation start voltage	Vhho	(Vss)			-3.5	V
Permitted leak resistance	Rleak	Between OSC1 and V_{DD} , V_{SS}	200			M Ω

*1: Items enclosed in parentheses () are those used when operating at heavy load protection mode.

E0C62A81 (CR)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, $R_{CR}=850k\Omega$, $T_a=25^\circ C$)

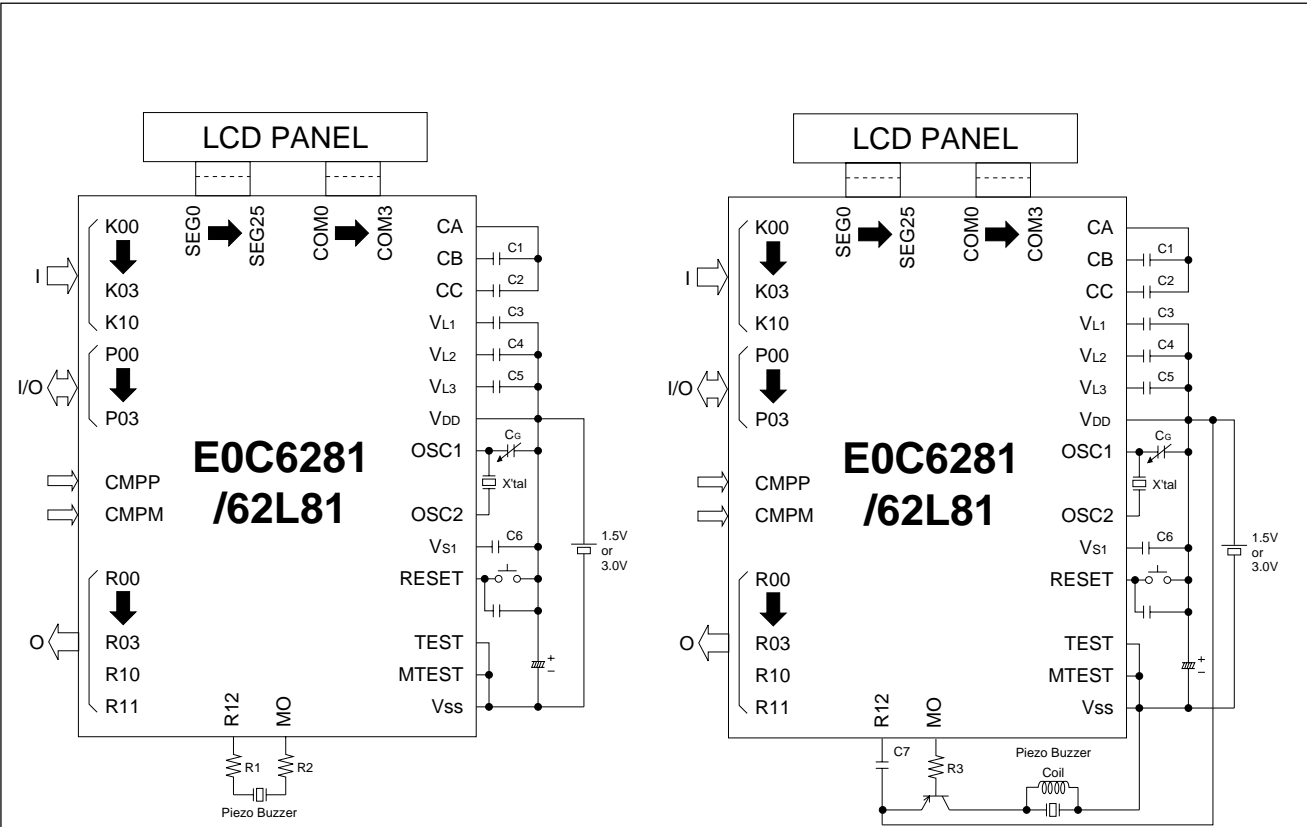
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fosc		-20	32.768kHz	20	%
Oscillation start voltage	Vsta	(Vss)	-1.8			V
Oscillation start time	tsta	$V_{SS}=-1.8$ to $-3.5V$		3		mS
Oscillation stop voltage	Vstp	(Vss)	-1.8			V

E0C62B81 (CR)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-1.5V$, $R_{CR}=850k\Omega$, $T_a=25^\circ C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fosc		-20	32.768kHz	20	%
Oscillation start voltage	Vsta	(Vss)	-0.9			V
Oscillation start time	tsta	$V_{SS}=-0.9$ to $-3.5V$		3		mS
Oscillation stop voltage	Vstp	(Vss)	-0.9			V

■ BASIC EXTERNAL CONNECTION DIAGRAM



X'tal	Crystal oscillator	32.768kHz, C _i (Max.)=35kΩ
Cg	Trimmer capacitor	5–25pF
C1–C6	Capacitor	0.1μF
Cp	Capacitor	3.3μF
R1, R2	Protection resistor	100Ω

X'tal	Crystal oscillator	32.768kHz, C _i (Max.)=35kΩ
Cg	Trimmer capacitor	5–25pF
C1–C6	Capacitor	0.1μF
C7	Capacitor	1μF–10μF
Cp	Capacitor	3.3μF
R3	Resistor	1kΩ or more

Note: The above tables are simply an example, and are not guaranteed to work.

