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N04L163WC1C

**Advance Information** 

# 4Mb Ultra-Low Power Asynchronous CMOS SRAM 256K × 16 bit

#### Overview

The N04L163WC1C is an integrated memory device containing a 4 Mbit Static Random Access Memory organized as 262,144 words by 16 bits. The device is designed and fabricated using NanoAmp's advanced CMOS technology to provide both high-speed performance and ultra-low power. The device operates with a single chip enable  $(\overline{CE})$  control and output enable  $(\overline{OE})$  to allow for easy memory expansion. Byte controls (UB and LB) allow the upper and lower bytes to be accessed independently. The N04L163WC1C is optimal for various applications where low-power is critical such as battery backup and hand-held devices. The device can operate over a very wide temperature range of -40°C to +85°C and is available in JEDEC standard packages compatible with other standard 256Kb x 16 SRAMs.

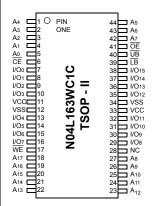
#### **Features**

- Single Wide Power Supply Range 2.2 to 3.6 Volts
- Very low standby current 2.0µA at 3.0V (Typical)
- Very low operating current
   1.5mA at 3.0V and 1µs (Typical)
- Simple memory control
   Single Chip Enable (CE)
   Byte control for independent byte operation
   Output Enable (OE) for memory expansion
- Low voltage data retention Vcc = 1.5V
- Very fast output enable access time 25ns OE access time
- Automatic power down to standby mode
- TTL compatible three-state output driver
- Compact space saving BGA package available
- Ultra Low Power Sort Available

### **Product Family**

Part Number	Package Type	Operating Temperature	Power Supply (Vcc)	Speed Options	Standby Current (I <sub>SB</sub> ), Typical	Operating Current (Icc), Typical
N04L163WC1CZ1	VFBGA Pb-Free	4000 1 0500	2.2V - 3.6V	55ns	2 4	1.5 mA @
N04L163WC1CT1	44-TSOP II Pb-Free	-40°C to +85°C	2.20 - 3.00	55118	2 μΑ	1MHz

## **Pin Configurations**

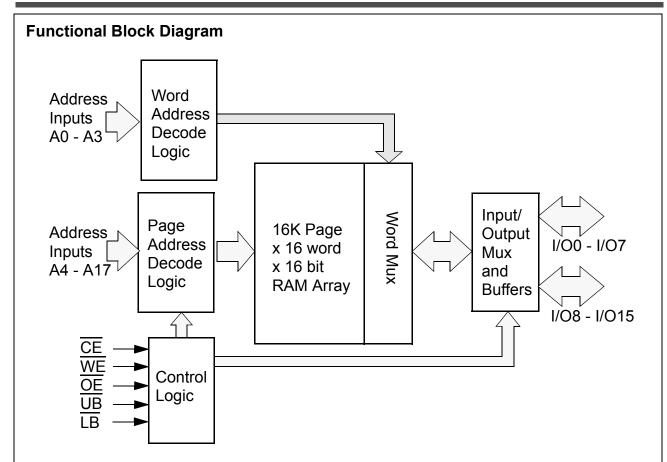


	1	2	3	4	5	6	
Α	lВ	OE.	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	NC	
В	I/O <sub>8</sub>	UB	A <sub>3</sub>	A <sub>4</sub>	CE	I/O <sub>0</sub>	
С	I/O <sub>9</sub>	I/O <sub>10</sub>	A <sub>5</sub>	A <sub>6</sub>	I/O <sub>1</sub>	I/O <sub>2</sub>	
D	$v_{ss}$	I/O <sub>11</sub>	A <sub>17</sub>	A <sub>7</sub>	I/O <sub>3</sub>	$v_{cc}$	
Е	v <sub>cc</sub>	I/O <sub>12</sub>	DNU	A <sub>16</sub>	I/O <sub>4</sub>	V <sub>SS</sub>	
F	I/O <sub>14</sub>	I/O <sub>13</sub>	A <sub>14</sub>	A <sub>15</sub>	I/O <sub>5</sub>	I/O <sub>6</sub>	
G	I/O <sub>15</sub>	NC	A <sub>12</sub>	A <sub>13</sub>	WE	I/O <sub>7</sub>	
Н	NC	A <sub>8</sub>	A <sub>9</sub>	A <sub>10</sub>	A <sub>11</sub>	NC	
	48 Pin VERGA (top)						

48 Pin VFBGA (top) 6 x 8 mm

## **Pin Descriptions**

Pin Name	Pin Function	
A <sub>0</sub> -A <sub>17</sub>	Address Inputs	
WE	Write Enable Input	
CE	Chip Enable Input	
ŌĒ	Output Enable Input	
LB	Lower Byte Enable Input	
UB	Upper Byte Enable Input	
I/O <sub>0</sub> -I/O <sub>15</sub>	Data Inputs/Outputs	
V <sub>CC</sub>	Power	
V <sub>SS</sub> Ground		
NC	Not Connected	
DNU Do Not Use		



### **Functional Description**

CE	WE	OE	UB	LB	I/O <sub>0</sub> - I/O <sub>15</sub> <sup>1</sup> MODE		POWER
Н	Х	Х	Х	Х	High Z	Standby <sup>2</sup>	Standby
Х	Х	Χ	Н	Н	High Z	Standby <sup>2</sup>	Standby
L	L	X <sup>3</sup>	L <sup>1</sup>	L <sup>1</sup>	Data In	Write <sup>3</sup>	Active
L	Н	L	$L^1$	L <sup>1</sup>	Data Out	Read	Active
L	Н	Н	L <sup>1</sup>	L <sup>1</sup>	High Z	Active	Active

- 1. When  $\overline{\text{UB}}$  and  $\overline{\text{LB}}$  are in select mode (low), I/O $_0$  I/O $_{15}$  are affected as shown. When  $\overline{\text{LB}}$  only is in the select mode only I/O $_0$  I/O $_7$  are affected as shown. When  $\overline{\text{UB}}$  is in the select mode only I/O $_8$  I/O $_{15}$  are affected as shown.
- 2. When the device is in standby mode, control inputs (WE, OE, UB, and LB), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.
- 3. When  $\overline{\text{WE}}$  is invoked, the  $\overline{\text{OE}}$  input is internally disabled and has no effect on the circuit.

# Capacitance<sup>1</sup>

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V, f = 1 MHz, T <sub>A</sub> = 25°C		10	pF
I/O Capacitance	C <sub>I/O</sub>	V <sub>IN</sub> = 0V, f = 1 MHz, T <sub>A</sub> = 25°C		10	pF

1. These parameters are verified in device characterization and are not 100% tested

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# Absolute Maximum Ratings<sup>1</sup>

Item	Symbol	Rating	Unit
Voltage on any pin relative to V <sub>SS</sub>	V <sub>IN,OUT</sub>	-0.3 to V <sub>CC</sub> +0.3	V
Voltage on $V_{CC}$ Supply Relative to $V_{SS}$	V <sub>CC</sub>	-0.3 to 4.5	V
Power Dissipation	$P_{D}$	500	mW
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Operating Temperature	T <sub>A</sub>	-40 to +85	°C
Soldering Temperature and Time	T <sub>SOLDER</sub>	260°C, 10sec	°C

<sup>1.</sup> Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### **Operating Characteristics (Over Specified Temperature Range)**

Item	Symbol	Test Conditions		Min.	Typ <sup>1</sup>	Max	Unit
Supply Voltage	V <sub>CC</sub>			2.2	3.0	3.6	V
Data Retention Voltage	$V_{DR}$	Chip Disabled		1.5			V
Input High Voltage	\/	Vcc = 2.2V to 2.7V		1.8		V <sub>CC</sub> +0.3	V
Input High Voltage	$V_{IH}$	Vcc = 2.7V to 3.6V		2.2		V <sub>CC</sub> +0.3	V
Input Low Voltage	V <sub>IL</sub>	Vcc = 2.2V to 2.7V		-0.3		0.6	V
mput Low Voltage	¥ IL	Vcc = 2.7V to 3.6V		-0.3		8.0	٧
Output High Voltage	V <sub>OH</sub>	$I_{OH} = -0.1 \text{mA}, Vcc = 2.20$	V	2.0			V
Output riight voitage	VOH	I <sub>OH</sub> = -1.0mA, Vcc = 2.70	2.4			V	
Output Law Valtage	V <sub>OL</sub>	$I_{OL} = 0.1 \text{mA}, Vcc = 2.20 \text{V}$				0.4	V
Output Low Voltage		I <sub>OL</sub> = 2.1mA, Vcc = 2.70\			0.4	v	
Input Leakage Current	ILI	$V_{IN}$ = 0 to $V_{CC}$	V <sub>IN</sub> = 0 to V <sub>CC</sub>			1	μА
Output Leakage Current	I <sub>LO</sub>	$\overline{OE}$ = V <sub>IH</sub> or Chip Disable V <sub>OUT</sub> = 0 to V <sub>CC</sub>	$\overline{OE} = V_{IH}$ or Chip Disabled $V_{OUT} = 0$ to $V_{CC}$			1	μА
Read/Write Operating Supply Current		V <sub>CC</sub> =3.6 V, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> Chip Enabled, I <sub>OUT</sub> = 0 -L			1.5	3.0	mA
@ 1 μs Cycle Time <sup>2</sup>	I <sub>CC1</sub>				1.5	3.0	IIIA
Read/Write Operating Supply Current	I <sub>CC2</sub>	$V_{CC}$ =3.6 V, $V_{IN}$ = $V_{IH}$ or $V_{IL}$			8	15.0	mA
@ fmax	ICC2	Chip Enabled, I <sub>OUT</sub> = 0	-L		8	10.0	ША
		$V_{IN} = V_{CC}$ or $0V$			2.0	12	
Maximum Standby Current	I <sub>SB1</sub>	Chip Disabled t <sub>A</sub> = 85°C, VCC = 3.6 V			2.0	8	μА
Maximum Data Retention Current	I <sub>DR</sub>	Vcc = 1.5V, CE ≥ Vcc - 0.2V,				9	μА
Waximum Bata Notontion Ourient	יטא.	$VIN \ge Vcc - 0.2V \text{ or } VIN \le 0.2V$	-L			6	μι

<sup>1.</sup> Typical values are measured at Vcc=Vcc Typ.,  $\rm T_A=25^{\circ}C$  and are not 100% tested.

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<sup>2.</sup> This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.

## **Timing Test Conditions**

Item	
Input Pulse Level	0.1V <sub>CC</sub> to 0.9 V <sub>CC</sub>
Input Rise and Fall Time	1V/ns
Input and Output Timing Reference Levels	0.5 V <sub>CC</sub>
Output Load	CL = 50pF
Operating Temperature	-40 to +85 °C

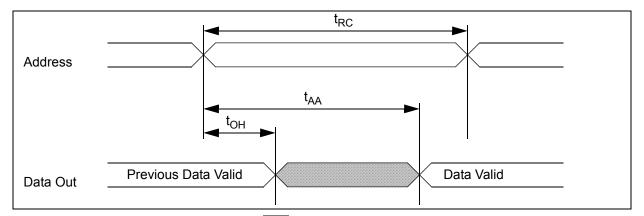
#### **Timing**

Mann	Oh al	-	Units	
Item	Symbol	Min.	Max.	
Read Cycle Time	t <sub>RC</sub>	55		ns
Address Access Time	t <sub>AA</sub>		55	ns
Chip Enable to Valid Output	t <sub>CO</sub>		55	ns
Output Enable to Valid Output	t <sub>OE</sub>		25	ns
Byte Select to Valid Output	t <sub>LB</sub> , t <sub>UB</sub>		55	ns
Chip Enable to Low-Z output	t <sub>LZ</sub>	10		ns
Output Enable to Low-Z Output	t <sub>OLZ</sub>	5		ns
Byte Select to Low-Z Output	t <sub>LBZ</sub> , t <sub>UBZ</sub>	10		ns
Chip Disable to High-Z Output	t <sub>HZ</sub>	0	20	ns
Output Disable to High-Z Output	t <sub>OHZ</sub>	0	20	ns
Byte Select Disable to High-Z Output	t <sub>LBHZ</sub> , t <sub>UBHZ</sub>	0	20	ns
Output Hold from Address Change	t <sub>OH</sub>	10		ns
Write Cycle Time	t <sub>WC</sub>	55		ns
Chip Enable to End of Write	t <sub>CW</sub>	40		ns
Address Valid to End of Write	t <sub>AW</sub>	40		ns
Byte Select to End of Write	t <sub>LBW</sub> , t <sub>UBW</sub>	40		ns
Write Pulse Width	t <sub>WP</sub>	40		ns
Address Setup Time	t <sub>AS</sub>	0		ns
Write Recovery Time	t <sub>WR</sub>	0		ns
Write to High-Z Output	t <sub>WHZ</sub>		20	ns
Data to Write Time Overlap	t <sub>DW</sub>	25		ns
Data Hold from Write Time	t <sub>DH</sub>	0		ns
End Write to Low-Z Output	t <sub>OW</sub>	10		ns

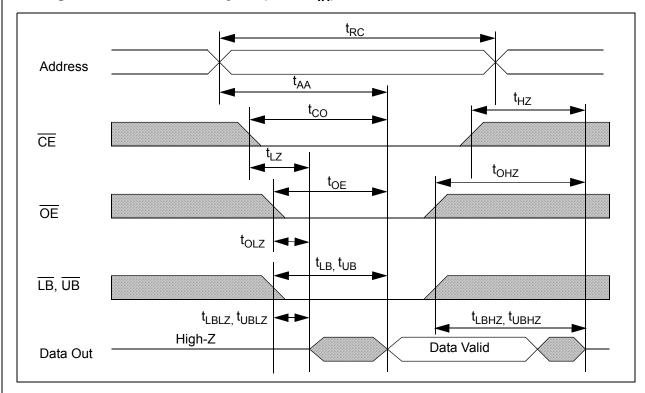
#### Note:

- 1. Full device AC operation assumes a 100us ramp time from 0 to Vcc(min) and 200us wait time after Vcc stablization.
- 2. Full device operation requires linear Vcc ramp from  $V_{DR}$  to  $Vcc(min) \ge 100us$  or stable at  $Vcc(min) \ge 100us$ .

# Timing of Read Cycle ( $\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$ )



# Timing Waveform of Read Cycle ( $\overline{WE} = V_{IH}$ )

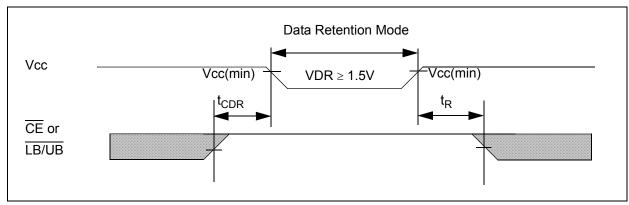


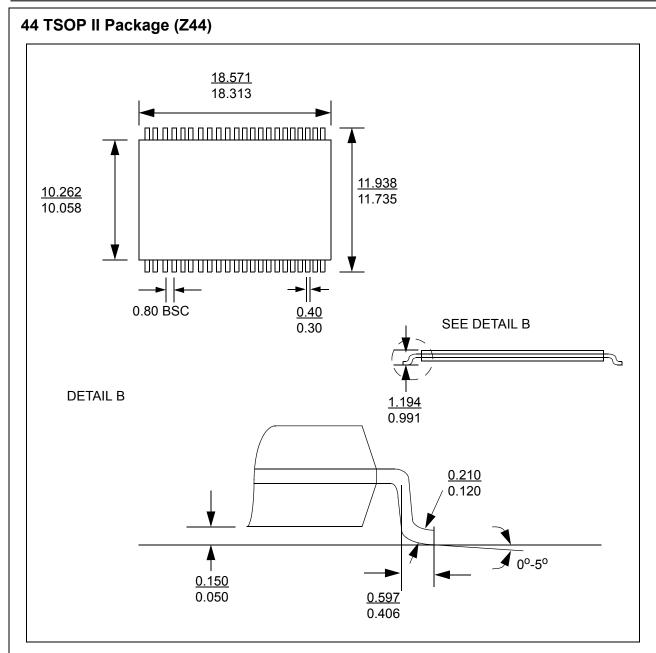
# Timing Waveform of Write Cycle (WE control) $t_{WC}$ Address $t_{WR}$ $t_{AW}$ $t_{CW}$ CE $t_{LBW},\,t_{UBW}$ LB, UB $t_{WP}$ $t_{AS}$ $\overline{\mathsf{WE}}$ $t_{DW}$ $t_{DH}$ High-Z Data Valid Data In t<sub>WHZ</sub> $t_{OW}$ High-Z Data Out Timing Waveform of Write Cycle (CE Control) t<sub>WC</sub> Address $t_{AW}$ CE $t_{CW}$ $t_{AS}$ $t_{LBW},\,t_{UBW}$ LB, UB $t_{WP}$ WE $t_{DW}$ $t_{DH}$ Data Valid Data In $t_{\text{WHZ}} \\$ High-Z Data Out

#### **Data Retention Characteristics**

Parameter	Description	Condition		Min	Тур	Max	Unit
$V_{DR}$	Vcc for Data Retention			1.5			V
I <sub>CCDR</sub>	Data Retention Current	Vcc = 1.5V, CE ≥ Vcc - 0.2V,				9	μA
OODIX		$VIN \ge Vcc - 0.2V \text{ or } VIN \le 0.2V$	<b>-</b> L			6	Jan. 1
t <sub>CDR</sub>	Chip Deselect to Data Retention Time			0			ns
t <sub>R</sub>	Operation Recovery Time			t <sub>RC</sub>			ns

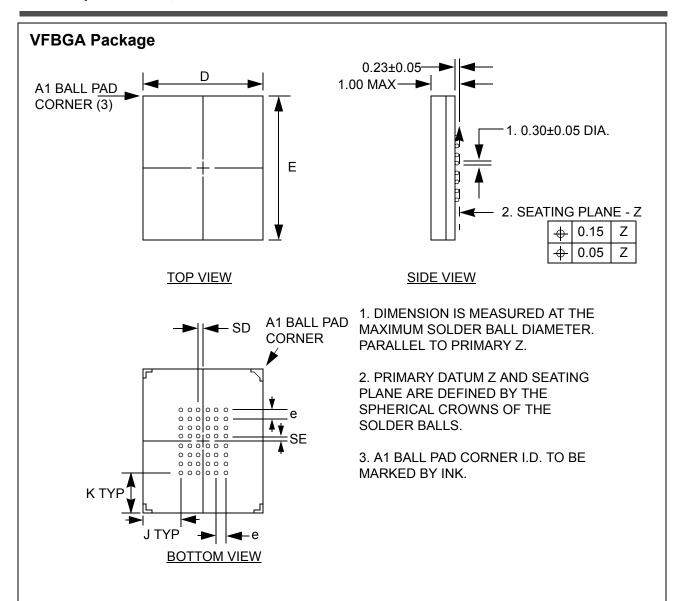
#### **Data Retention Waveform**





#### Note:

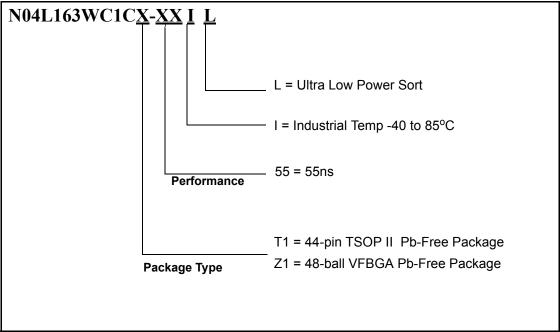
1. All dimensions in inches (Millimeters)



#### **Dimensions (mm)**

D	Е		BALL MATRIX			
	E	SD	SE	J	K	TYPE
6±0.10	8±0.10	0.375	0.375	1.125	1.375	FULL

## **Ordering Information**



#### **Revision History**

Revision #	Date Change Description			
Α	Oct 6. 2004	Initial Preliminary Release		
В	Nov 8. 2004 General Update			
С	C Jan 14. 2005 General Update			

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