

*4M x 4Bit CMOS Dynamic RAM with Fast Page Mode*

**DESCRIPTION**

This is a family of 4,194,304 x 4 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Power supply voltage (+5.0V or +3.3V), refresh cycle (2K Ref. or 4K Ref.), access time (-50 or -60), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh,  $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 4Mx4 Fast Page Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory for high level computer, microcomputer and personal computer.

**FEATURES**

• Part Identification

- K4F170411C-B(F) (5V, 4K Ref.)
- K4F160411C-B(F) (5V, 2K Ref.)
- K4F170412C-B(F) (3.3V, 4K Ref.)
- K4F160412C-B(F) (3.3V, 2K Ref.)

• Active Power Dissipation

Unit : mW

Speed	3.3V		5V	
	4K	2K	4K	2K
-50	324	396	495	605
-60	288	360	440	550

• Refresh Cycles

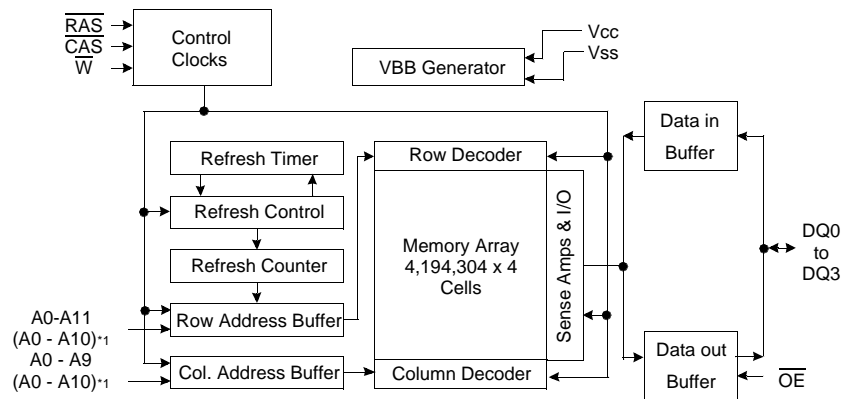
Part NO.	V <sub>CC</sub>	Refresh cycle	Refresh period	
			Nor-	L-ver
K4F170411C	5V	4K	64ms	128ms
K4F170412C	3.3V			
K4F160411C	5V	2K	32ms	
K4F160412C	3.3V			

• Performance Range

Speed	t <sub>RAC</sub>	t <sub>CAC</sub>	t <sub>RC</sub>	t <sub>PC</sub>	Remark
-50	50ns	13ns	90ns	35ns	5V/3.3V
-60	60ns	15ns	110ns	40ns	5V/3.3V

- Fast Page Mode operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- Fast parallel test mode capability
- TTL(5V)/LVTTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply (5V product)
- Single +3.3V±0.3V power supply (3.3V product)

**FUNCTIONAL BLOCK DIAGRAM**

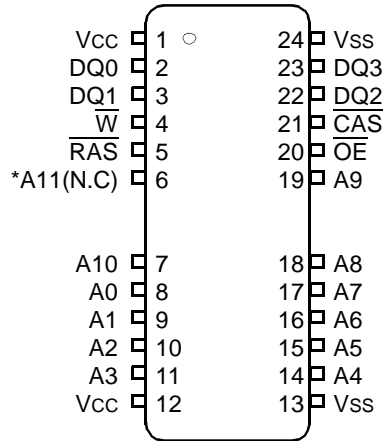


Note) \*1: 2K Refresh

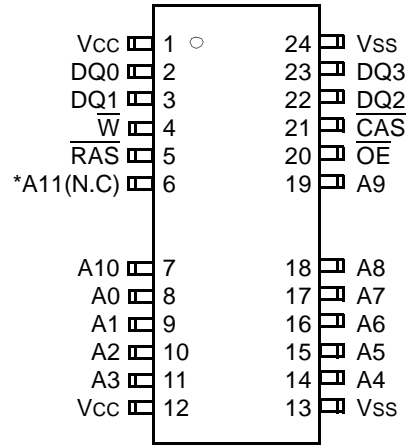
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PIN CONFIGURATION (Top Views)

• K4F17(6)0411(2)C-B



• K4F17(6)0411(2)C-F



\*A11 is N.C for K4F160411(2)C (5V/3.3V, 2K Ref. product)

B : 300mil 26(24) SOJ

F : 300mil 26(24) TSOP II

Pin Name	Pin Function
A0 - A11	Address Inputs (4K Product)
A0 - A10	Address Inputs (2K Product)
DQ0 - 3	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power(+5V)
	Power(+3.3V)
N.C	No Connection (2K Ref. product)

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to Vss	VIN,VOUT	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on Vcc supply relative to Vss	Vcc	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	PD	1	1	W
Short Circuit Output Current	IosAddress	50	50	mA

\* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS** (Voltage referenced to Vss, TA= 0 to 70°C)

Parameter	Symbol	3.3V			5V			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	Vcc	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	Vss	0	0	0	0	0	0	V
Input High Voltage	VIH	2.0	-	Vcc+0.3*1	2.4	-	Vcc+1.0*1	V
Input Low Voltage	VIL	-0.3*2	-	0.8	-1.0*2	-	0.8	V

\*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc

\*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at Vss

**DC AND OPERATING CHARACTERISTICS** (Recommended operating conditions unless otherwise noted.)

Max	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{IN} + 0.3V$ , all other input pins not under test=0 Volt)	II(L)	-5	5	uA
	Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$ )	IO(L)	-5	5	uA
	Output High Voltage Level( $I_{OH} = -2mA$ )	VOH	2.4	-	V
	Output Low Voltage Level( $I_{OL} = 2mA$ )	VOL	-	0.4	V
5V	Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{IN} + 0.5V$ , all other input pins not under test=0 Volt)	II(L)	-5	5	uA
	Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$ )	IO(L)	-5	5	uA
	Output High Voltage Level( $I_{OH} = -5mA$ )	VOH	2.4	-	V
	Output Low Voltage Level( $I_{OL} = 4.2mA$ )	VOL	-	0.4	V

**DC AND OPERATING CHARACTERISTICS (Continued)**

Symbol	Power	Speed	Max				Units
			K4F170412C	K4F160412C	K4F170411C	K4F160411C	
Icc1	Don't care	-50	90	110	90	110	mA
		-60	80	100	80	100	mA
Icc2	Normal L	Don't care	1	1	2	2	mA
			1	1	1	1	mA
Icc3	Don't care	-50	90	110	90	110	mA
		-60	80	100	80	100	mA
Icc4	Don't care	-50	80	90	80	90	mA
		-60	70	80	70	80	mA
Icc5	Normal L	Don't care	0.5	0.5	1	1	mA
			200	200	250	250	uA
Icc6	Don't care	-50	90	110	90	110	mA
		-60	80	100	80	100	mA
Icc7	L	Don't care	250	250	300	300	uA
Iccs	L	Don't care	200	200	250	250	uA

Icc1\* : Operating Current ( $\overline{RAS}$  and  $\overline{CAS}$ , Address cycling @trc=min.)

Icc2 : Standby Current ( $RAS=CAS=W=V_{IH}$ )

Icc3\* :  $\overline{RAS}$ -only Refresh Current ( $\overline{CAS}=V_{IH}$ ,  $\overline{RAS}$ , Address cycling @trc=min.)

Icc4\* : Fast Page Mode Current ( $\overline{RAS}=V_{IL}$ ,  $\overline{CAS}$ , Address cycling @tPC=min.)

Icc5 : Standby Current ( $RAS=CAS=W=V_{CC}-0.2V$ )

Icc6\* :  $\overline{CAS}$ -Before- $\overline{RAS}$  Refresh Current ( $\overline{RAS}$  and  $\overline{CAS}$  cycling @trc=min.)

Icc7 : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage( $V_{IH}$ )= $V_{CC}-0.2V$ , Input low voltage( $V_{IL}$ )= $0.2V$ ,  $\overline{CAS}=0.2V$ ,

DQ=Don't care, Trc=31.25us(4K/L-ver), 62.5us(2K/L-ver), TRAS=TRASmin~300ns

Iccs : Self Refresh Current

$RAS=CAS=0.2V$ ,  $\overline{W}=\overline{OE}=A0 \sim A11=V_{CC}-0.2V$  or  $0.2V$ ,

DQ0 ~ DQ3= $V_{CC}-0.2V$ ,  $0.2V$  or Open

**\*Note** : Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1, Icc3 and Icc6 address can be changed maximum once while  $\overline{RAS}=V_{IL}$ . In Icc4, address can be changed maximum once within one fast page mode cycle time, tPC.

# K4F170411C, K4F160411C K4F170412C, K4F160412C

## CMOS DRAM

### CAPACITANCE (TA=25°C, VCC=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A11]	CIN1	-	5	pF
Input capacitance [ $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{W}}$ , $\overline{\text{OE}}$ ]	CIN2	-	7	pF
Output capacitance [DQ0 - DQ3]	CDQ	-	7	pF

### AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, See note 1,2)

Test condition (5V device) : VCC=5.0V±10%, VIH/VIL=2.4/0.8V, VOH/VOL=2.4/0.4V

Test condition (3.3V device) : VCC=3.3V±0.3V, VIH/VIL=2.0/0.8V, VOH/VOL=2.0/0.8V

Parameter	Symbol	-50		-60		Units	Notes
		Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		ns	
Read-modify-write cycle time	tRWC	133		155		ns	
Access time from $\overline{\text{RAS}}$	tRAC		50		60	ns	3,4,10
Access time from $\overline{\text{CAS}}$	tCAC		13		15	ns	3,4,5
Access time from column address	tAA		25		30	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	ns	6
Transition time (rise and fall)	tT	3	50	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	30		40		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	13		15		ns	
$\overline{\text{CAS}}$ hold time	tCSH	50		60		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	13	10K	15	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	20	37	20	45	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	15	25	15	30	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	10		10		ns	
Column address set-up time	tASC	0		0		ns	
Column address hold time	tCAH	10		10		ns	
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		ns	8
Write command hold time	tWCH	10		10		ns	
Write command pulse width	tWP	10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	13		15		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	13		15		ns	

**AC CHARACTERISTICS** (Continued)

Parameter	Symbol	-50		-60		Units	Note
		Min	Max	Min	Max		
Data set-up time	tDS	0		0		ns	9
Data hold time	tDH	10		10		ns	9
Refresh period (2K, Normal)	tREF		32		32	ms	
Refresh period (4K, Normal)	tREF		64		64	ms	
Refresh period (L-ver)	tREF		128		128	ms	
Write command set-up time	tWCS	0		0		ns	7
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	36		40		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	73		85		ns	7
Column address to $\overline{\text{W}}$ delay time	tAWD	48		55		ns	7
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tCPWD	53		60		ns	
$\overline{\text{CAS}}$ set-up time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	5		5		ns	
$\overline{\text{CAS}}$ hold time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		5		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		30		35	ns	3
Fast Page cycle time	tPC	35		40		ns	
Fast Page read-modify-write cycle time	tPRWC	76		85		ns	
$\overline{\text{CAS}}$ precharge time (Fast Page cycle)	tCP	10		10		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page cycle)	tRASP	50	200K	60	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	30		35		ns	
$\overline{\text{OE}}$ access time	tOEA		13		15	ns	
$\overline{\text{OE}}$ to data delay	tOED	13		15		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	0	13	0	15	ns	6
$\overline{\text{OE}}$ command hold time	tOEH	13		15		ns	
Write command set-up time (Test mode in)	tWTS	10		10		ns	11
Write command hold time (Test mode in)	tWTH	10		10		ns	11
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time( $\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ refresh)	tWRP	10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time( $\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ refresh)	tWRH	10		10		ns	
$\overline{\text{RAS}}$ pulse width ( $\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	tRASS	100		100		us	13,14,15
$\overline{\text{RAS}}$ precharge time ( $\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	tRPS	90		110		ns	13,14,15
$\overline{\text{CAS}}$ hold time ( $\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	tCHS	-50		-50		ns	13,14,15

**TEST MODE CYCLE**

( Note 11 )

Parameter	Symbol	-50		-60		Units	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t <sub>RC</sub>	95		115		ns	
Read-modify-write cycle time	t <sub>RWC</sub>	138		160		ns	
Access time from $\overline{\text{RAS}}$	t <sub>RAC</sub>		55		65	ns	3,4,10,12
Access time from $\overline{\text{CAS}}$	t <sub>CAC</sub>		18		20	ns	3,4,5,12
Access time from column address	t <sub>AA</sub>		30		35	ns	3,10,12
$\overline{\text{RAS}}$ pulse width	t <sub>RAS</sub>	55	10K	65	10K	ns	
$\overline{\text{CAS}}$ pulse width	t <sub>CAS</sub>	18	10K	20	10K	ns	
$\overline{\text{RAS}}$ hold time	t <sub>RSH</sub>	18		20		ns	
$\overline{\text{CAS}}$ hold time	t <sub>CSH</sub>	55		65		ns	
Column address to $\overline{\text{RAS}}$ lead time	t <sub>RAL</sub>	30		35		ns	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	t <sub>CWD</sub>	41		45		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t <sub>RWD</sub>	78		90		ns	7
Column address to $\overline{\text{W}}$ delay time	t <sub>AWD</sub>	53		60		ns	7
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	t <sub>CPWD</sub>	58		65		ns	
Fast Page cycle time	t <sub>PC</sub>	40		45		ns	
Fast Page read-modify-write cycle time	t <sub>PRWC</sub>	81		90		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page cycle)	t <sub>RASP</sub>	55	200K	65	200K	ns	
Access time from $\overline{\text{CAS}}$ precharge	t <sub>CPA</sub>		35		40	ns	3
$\overline{\text{OE}}$ access time	t <sub>OE A</sub>		18		20	ns	
$\overline{\text{OE}}$ to data delay	t <sub>OE D</sub>	18		20		ns	
$\overline{\text{OE}}$ command hold time	t <sub>OE H</sub>	18		20		ns	

**NOTES**

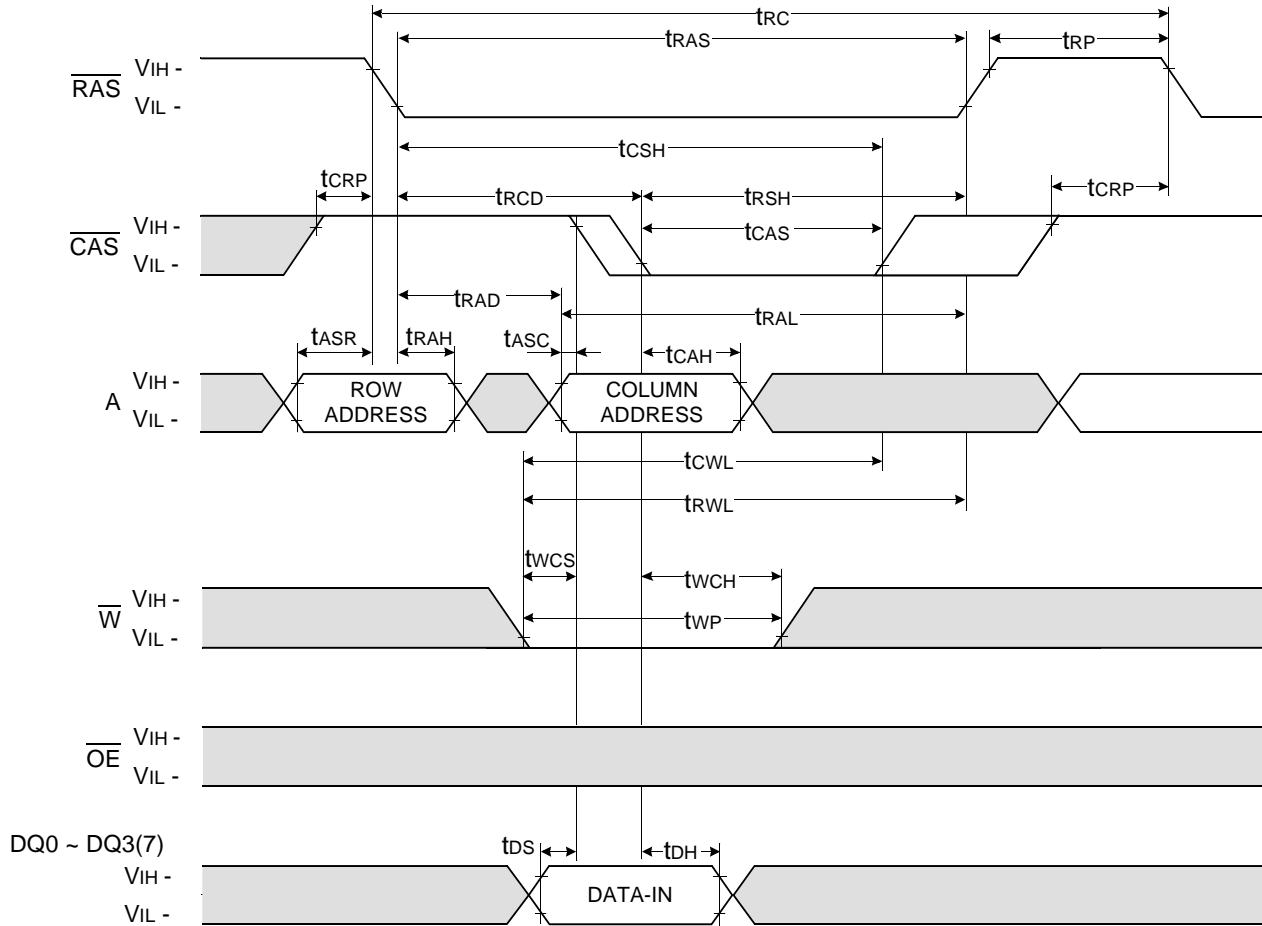
1. An initial pause of 200us is required after power-up followed by any 8  $\overline{\text{RAS}}$ -only refresh or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles before proper device operation is achieved.
2.  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1 TTL(3.3V) loads and 100pF.
4. Operation within the  $t_{\text{RCD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met.  $t_{\text{RCD}}(\text{max})$  is specified as a reference point only. If  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{CAC}}$ .
5. Assumes that  $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$ .
6.  $t_{\text{OFF}}(\text{min})$  and  $t_{\text{OEZ}}(\text{max})$  define the time at which the output achieves the open circuit condition and are not referenced  $V_{oh}$  or  $V_{ol}$ .
7.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{CWD}}$  and  $t_{\text{AWD}}$  are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ , the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If  $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ ,  $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$  and  $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ , then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a read cycle.
9. These parameters are referenced to  $\overline{\text{CAS}}$  falling edge in early write cycles and to  $\overline{\text{W}}$  falling edge in read-modify-write cycles.
10. Operation within the  $t_{\text{RAD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met.  $t_{\text{RAD}}(\text{max})$  is specified as a reference point only. If  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}(\text{max})$  limit, then access time is controlled by  $t_{\text{AA}}$ .
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of  $t_{\text{RAC}}$ ,  $t_{\text{AA}}$ ,  $t_{\text{CAC}}$  is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. If  $t_{\text{RASS}} \geq 100\text{us}$ , then  $\overline{\text{RAS}}$  precharge time must use  $t_{\text{RPS}}$  instead of  $t_{\text{RP}}$ .
14. For  $\overline{\text{RAS}}$ -only refresh and burst  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh mode, 4096(4K)/2048(2K) cycles of burst refresh must be executed within 64ms/32ms before and after self refresh, in order to meet refresh specification.
15. For distributed  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  with 15.6us interval  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.





WRITE CYCLE ( EARLY WRITE )

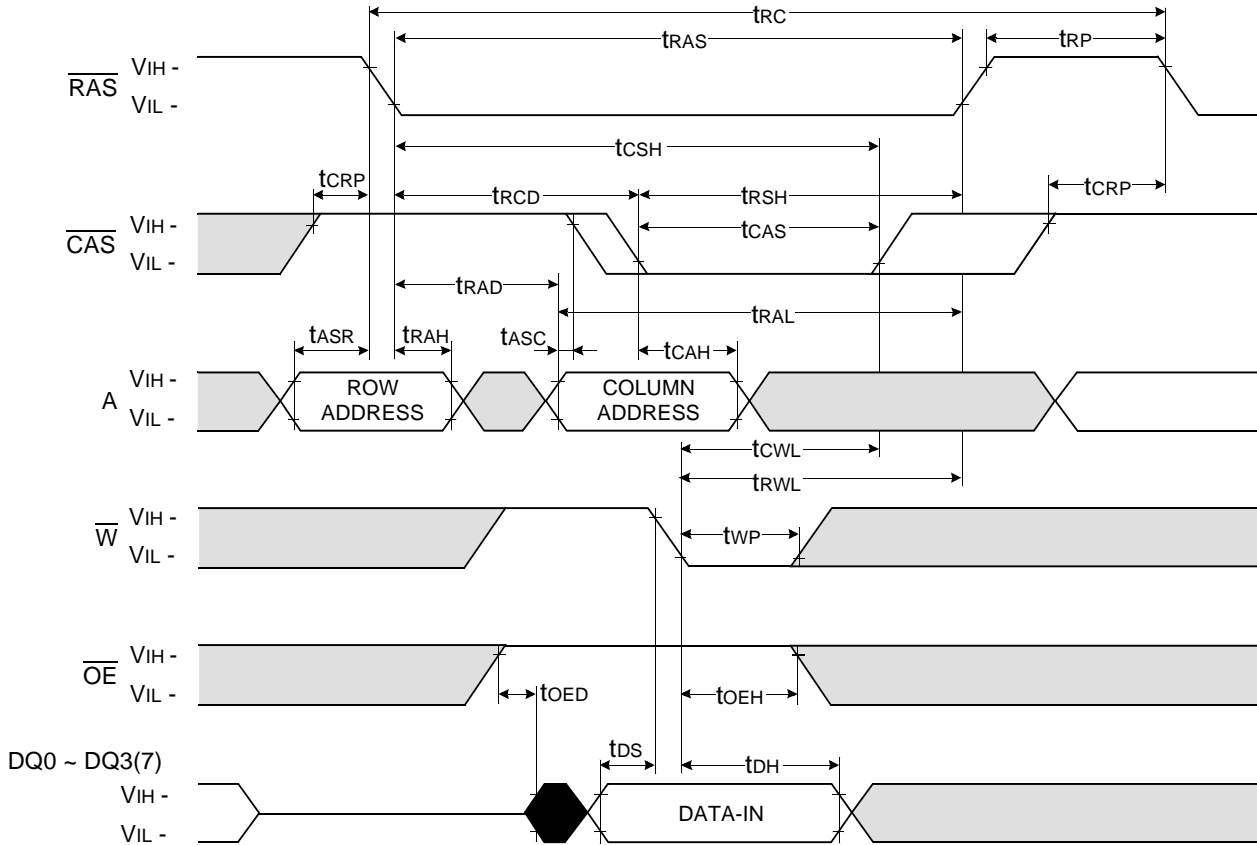
NOTE : DOUT = OPEN



□ Don't care  
 ■ Undefined

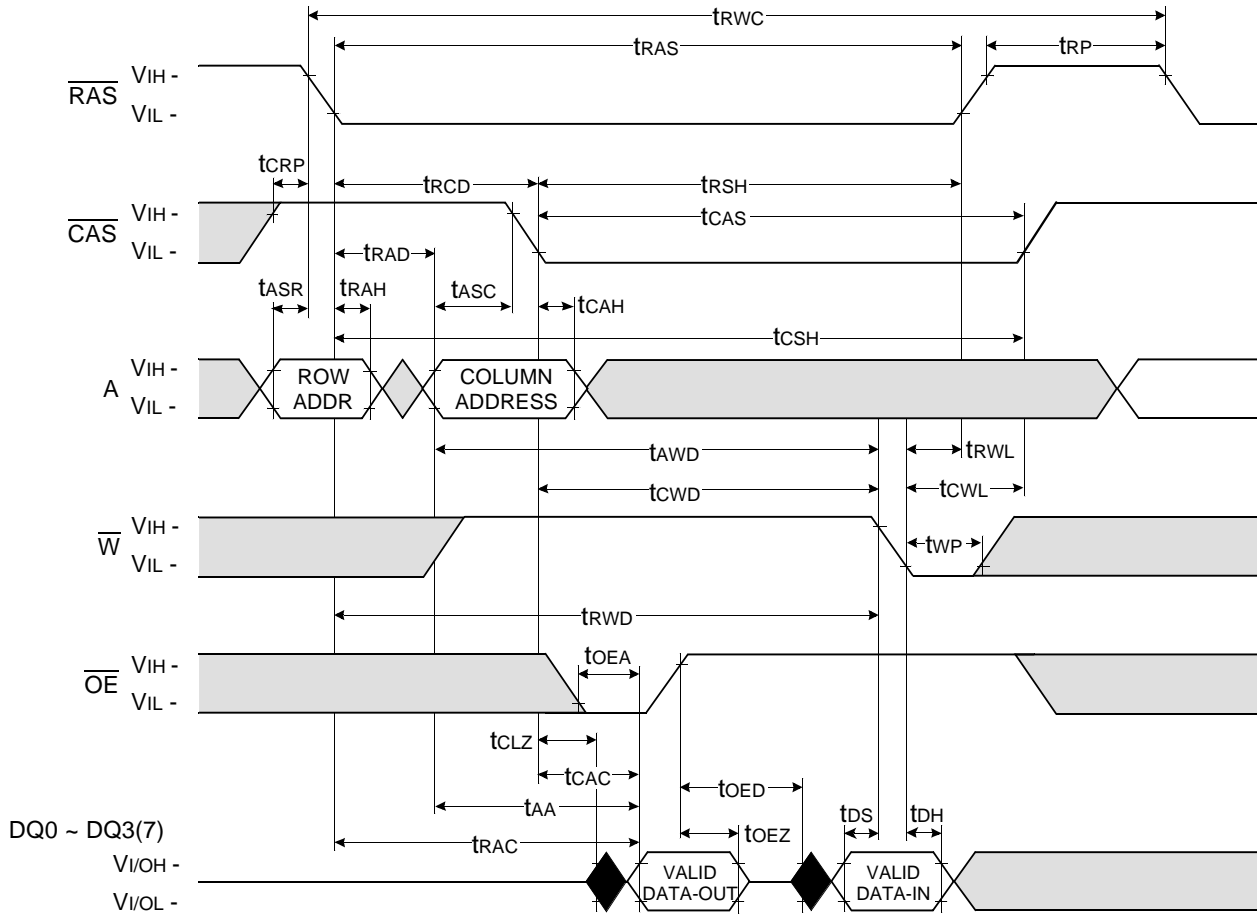
WRITE CYCLE (  $\overline{\text{OE}}$  CONTROLLED WRITE )

NOTE : DOUT = OPEN



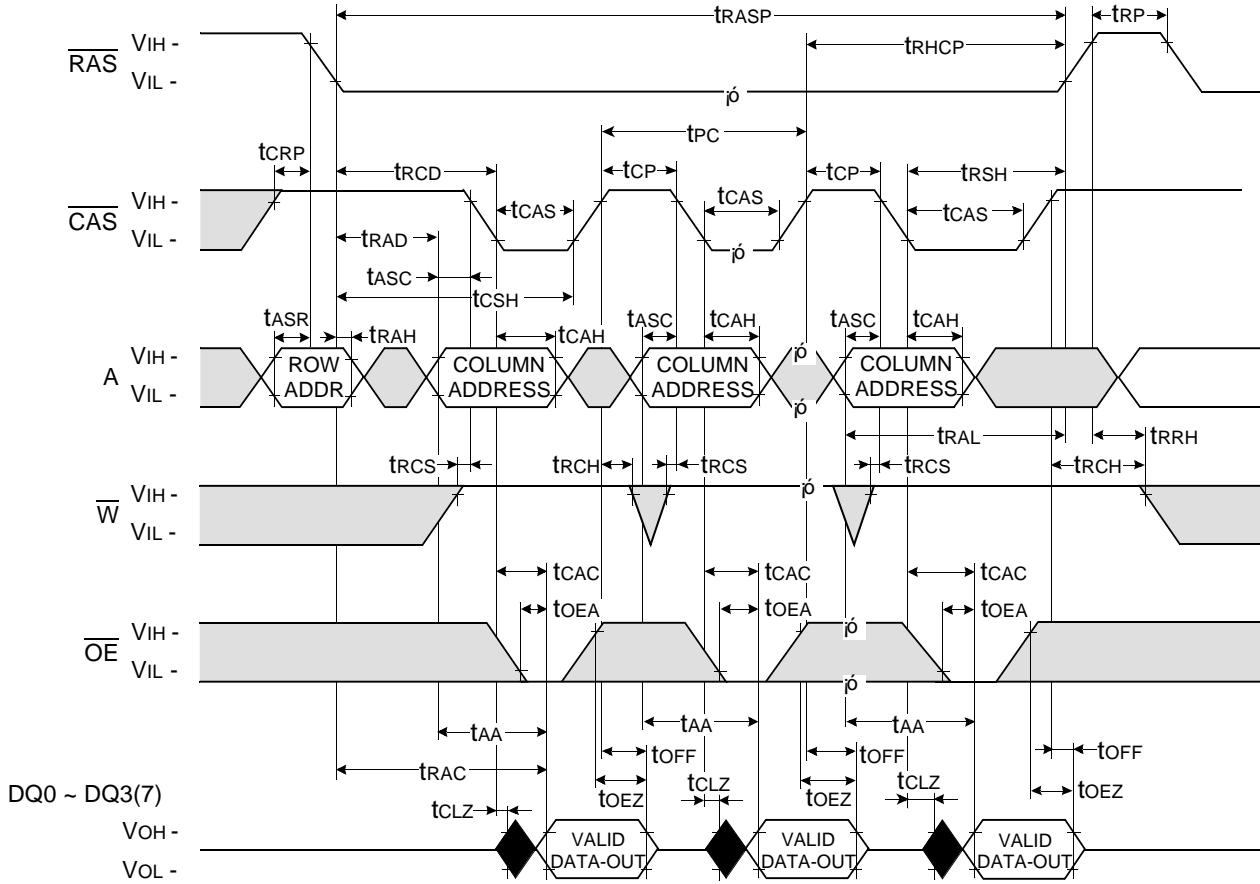
Don't care  
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READ - MODIFY - WRITE CYCLE



□ Don't care  
 ■ Undefined

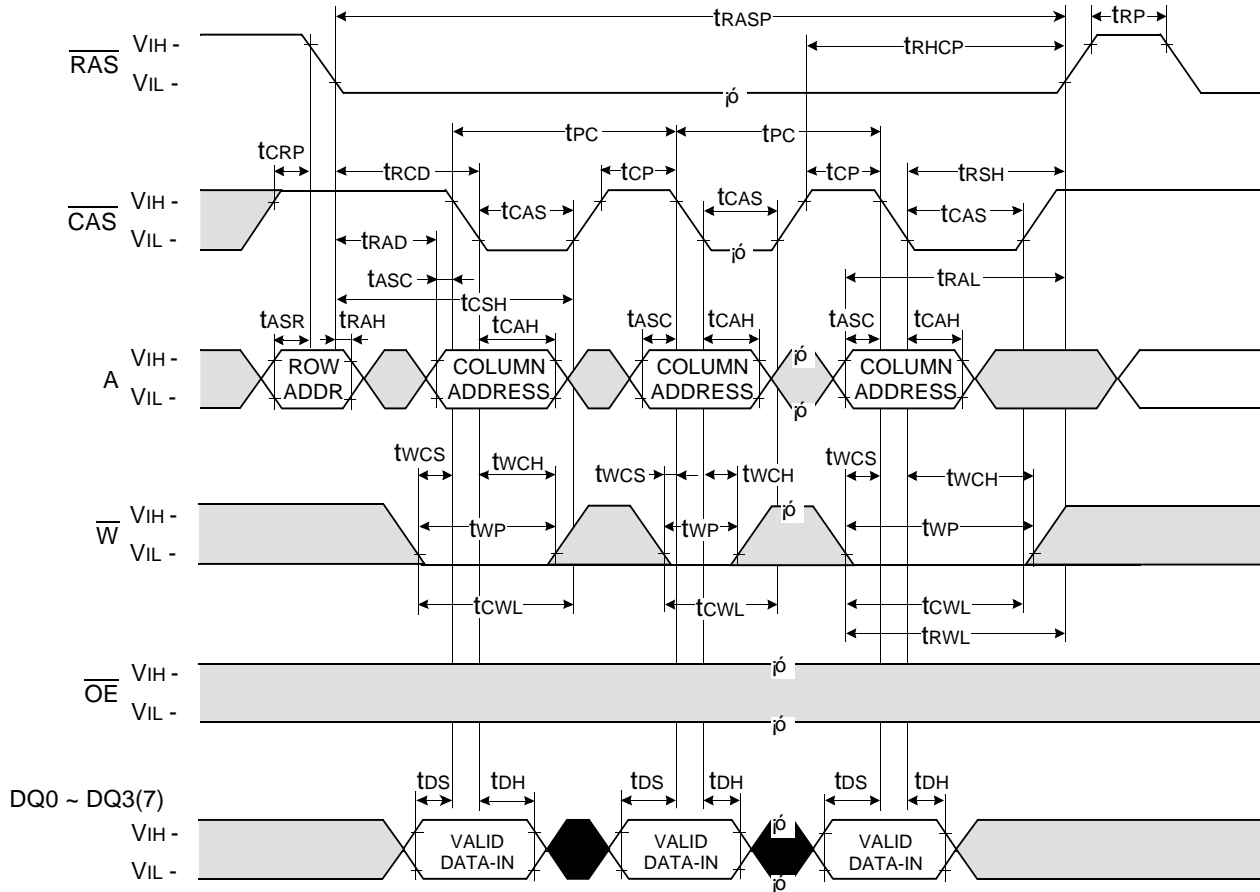
FAST PAGE READ CYCLE



□ Don't care  
 ■ Undefined

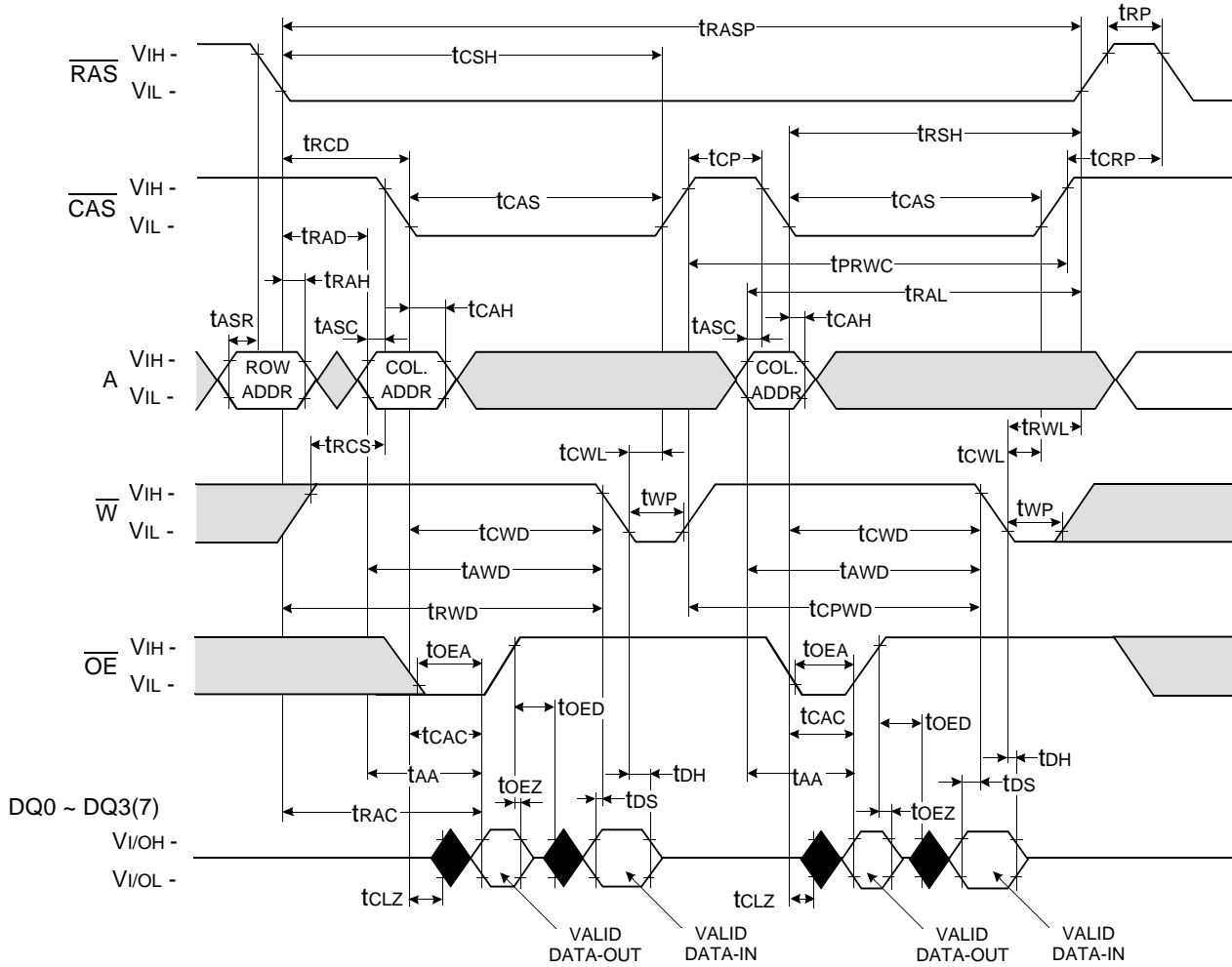
**FAST PAGE WRITE CYCLE ( EARLY WRITE )**

NOTE : DOUT = OPEN



□ Don't care  
 ■ Undefined

FAST PAGE READ - MODIFY - WRITE CYCLE

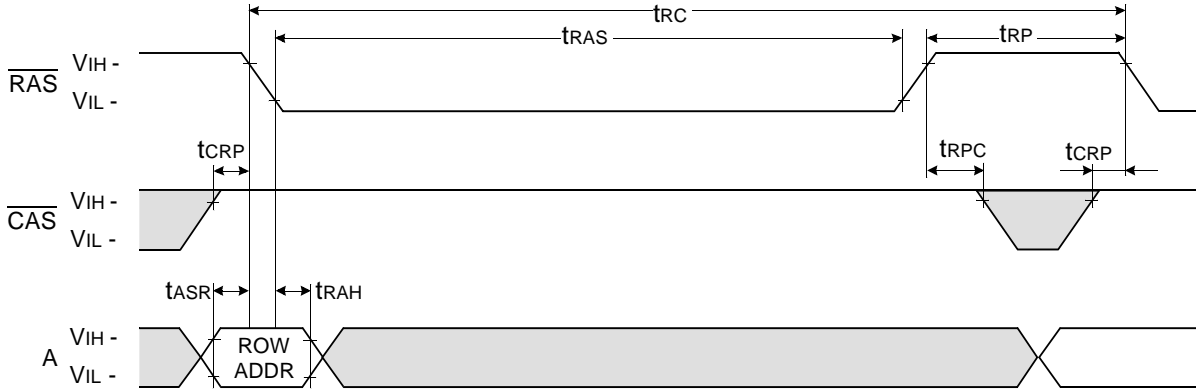


Don't care  
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**$\overline{\text{RAS}}$  - ONLY REFRESH CYCLE**

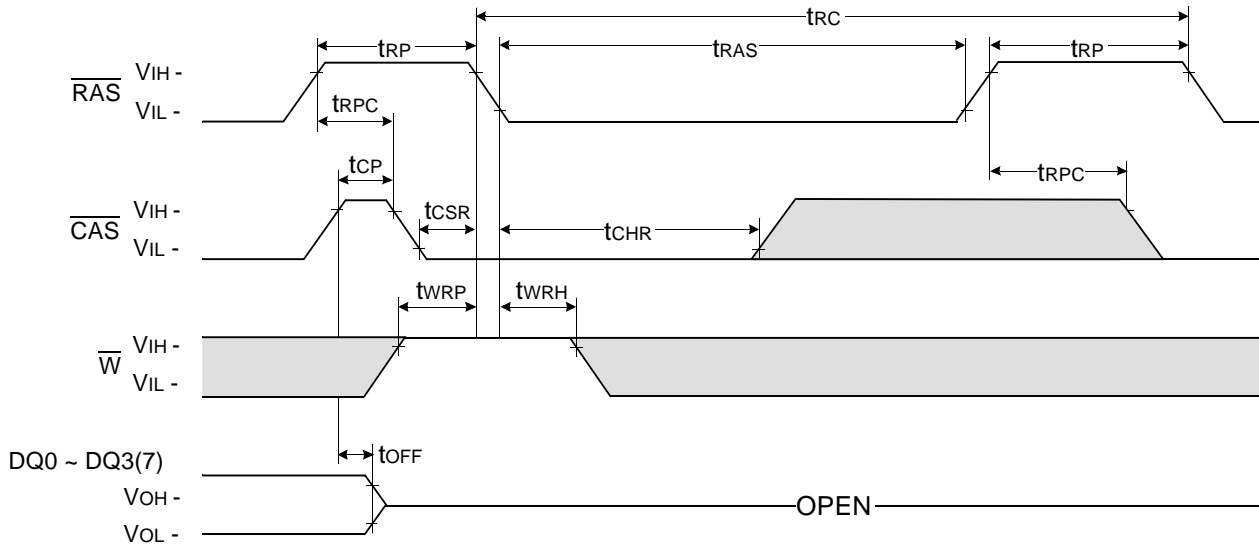
NOTE :  $\overline{\text{W}}$ ,  $\overline{\text{OE}}$ , DIN = Don't care

DOUT = OPEN



**$\overline{\text{CAS}}$  - BEFORE -  $\overline{\text{RAS}}$  REFRESH CYCLE**

NOTE :  $\overline{\text{OE}}$ , A = Don't care



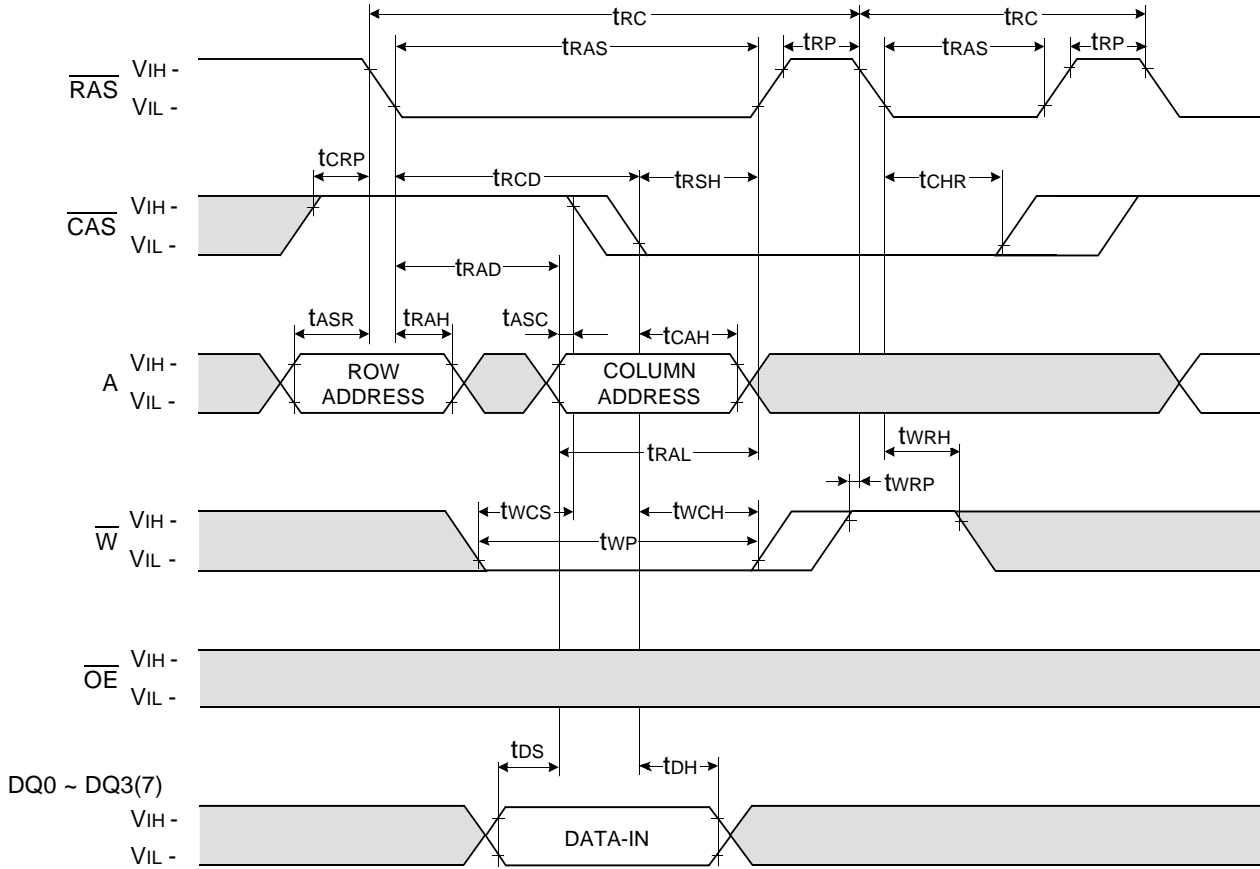
□ Don't care  
 ■ Undefined





HIDDEN REFRESH CYCLE ( WRITE )

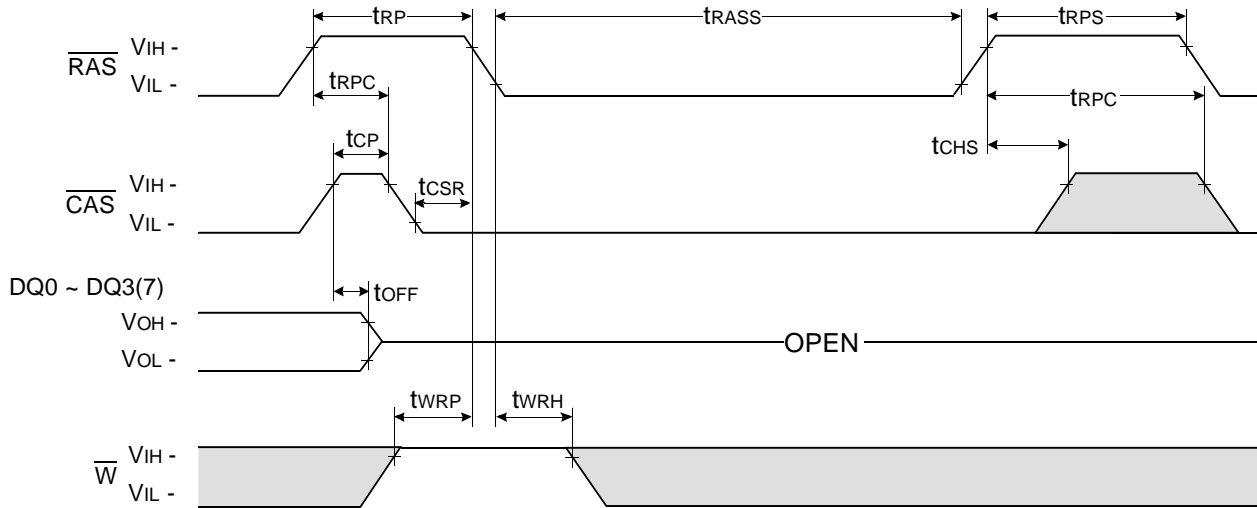
NOTE : DOUT = OPEN



□ Don't care  
 ■ Undefined

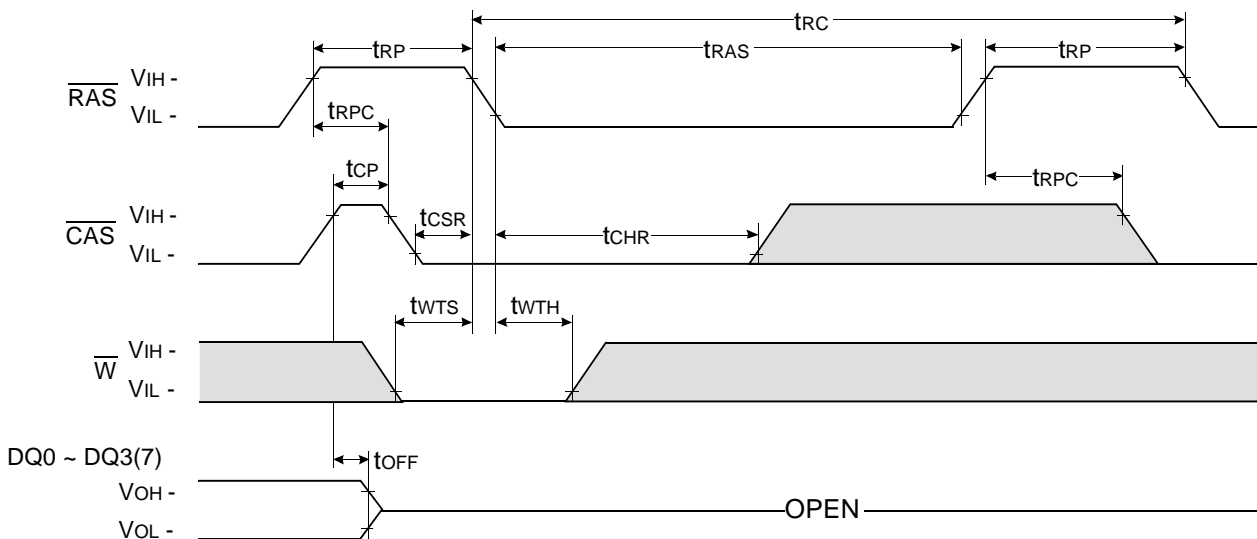
**$\overline{\text{CAS}}$  - BEFORE -  $\overline{\text{RAS}}$  SELF REFRESH CYCLE**

NOTE :  $\overline{\text{OE}}$ , A = Don't care



**TEST MODE IN CYCLE**

NOTE :  $\overline{\text{OE}}$ , A = Don't care



Don't care  
 Undefined

PACKAGE DIMENSION

