Product Specification

AHA3431 StarLite™

40 MBytes/sec Simultaneous Compressor/Decompressor IC, 3.3V

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1.0 INTRODUCTION

AHA3431 is a lossless compression coprocessor IC for hardcopy systems on many standard platforms. The device is targeted for high throughput and high resolution hardcopy systems. The AHA3431 is functionally backward compatible to the AHA3411.

Enhancements to this product over the AHA3411 include improved I/O timings, higher operating frequency and data rate, and lower power.

Blank band generation in real time and prearming registers between records enable advanced banding techniques. Bands may be in raw uncompressed, compressed or blank format in the frame buffer. The device processes all three formats and outputs the raster data to the printer engine. Appropriate registers are prearmed when switching from one type to the next. Separate byte ordering between the Compressor and the Decompressor with bit order control into the compressor allow full reversal of the image data for duplex printing support. A system may use multiple record counters and End-of-Transfer interrupts to easily handle pages partitioned into smaller records or bands.

This document contains functional description, system configurations, register descriptions, electrical characteristics and ordering information. It is intended for system designers considering a compression coprocessor in their embedded applications. Software simulation and an analysis of the algorithm for printer and copier images of various complexity are also available for evaluation. A comprehensive Designer's Guide complements this document to assist with the system design. Section 11.0 contains a list of related technical publications.

1.1 CONVENTIONS, NOTATIONS AND DEFINITIONS

– Active low signals have an "N" appended to the end of the signal name. For example, CSN and RDYN.
– A "bar" over a signal name indicates an inverse of the signal. For example, $\overline{SD}$ indicates an inverse of SD. This terminology is used only in logic equations.
– "Signal assertion" means the output signal is logically true.
– Hex values are represented with a prefix of "0x", such as Register "0x00". Binary values do not contain a prefix, for example, DSC=000.
– A range of signal names or register bits is denoted by a set of colons between the numbers. Most significant bit is always shown first, followed by least significant bit. For example, VOD[7:0] indicates signal names VOD7 through VOD0.
– A logical "AND" function of two signals is expressed with an "&" between variables.
– Mega Bytes per second is referred to as MBytes/sec or MB/sec.
– In referencing microprocessors, an x, xx or xxx is used as suffix to indicate more than one processor. For example, Motorola 68xxx processor family includes various 68000 processors from Motorola.
– Reserved bits in registers are referred as "*res*".
– REQN or ACKN refer to either CI, DI, CO or DO Request or Acknowledge signals, as applicable.

1.2 FEATURES

PERFORMANCE:

- 40 MBytes/sec maximum sustained compression and decompression rate
- 160 MBytes/sec burst data rate over a 32-bit data bus
- 40 MBytes/sec synchronous 8-bit video in and video out ports
- Maximum clock speeds up to 40 MHz
- Simultaneous compression and decompression at full bandwidth
- Average 15 to 1 compression ratio for 1200 dpi bitmap image data
- Advanced banding support: blank bands, prearming

FLEXIBILITY:

- Big Endian or Little Endian; 32 or 16-bit bus width and data bit/byte reordering for duplex printing support
- Programmable Record Length, Record Count and Scan Length Registers may be prearmed
- Scan line length up to 2K bytes
- Interfaces directly with various MIPS, Motorola 68xxx and Cold FIRE, and Intel i960 embedded processors
- Pass-through mode passes raw data through compression and decompression engines
- Counter checks errors in decompression

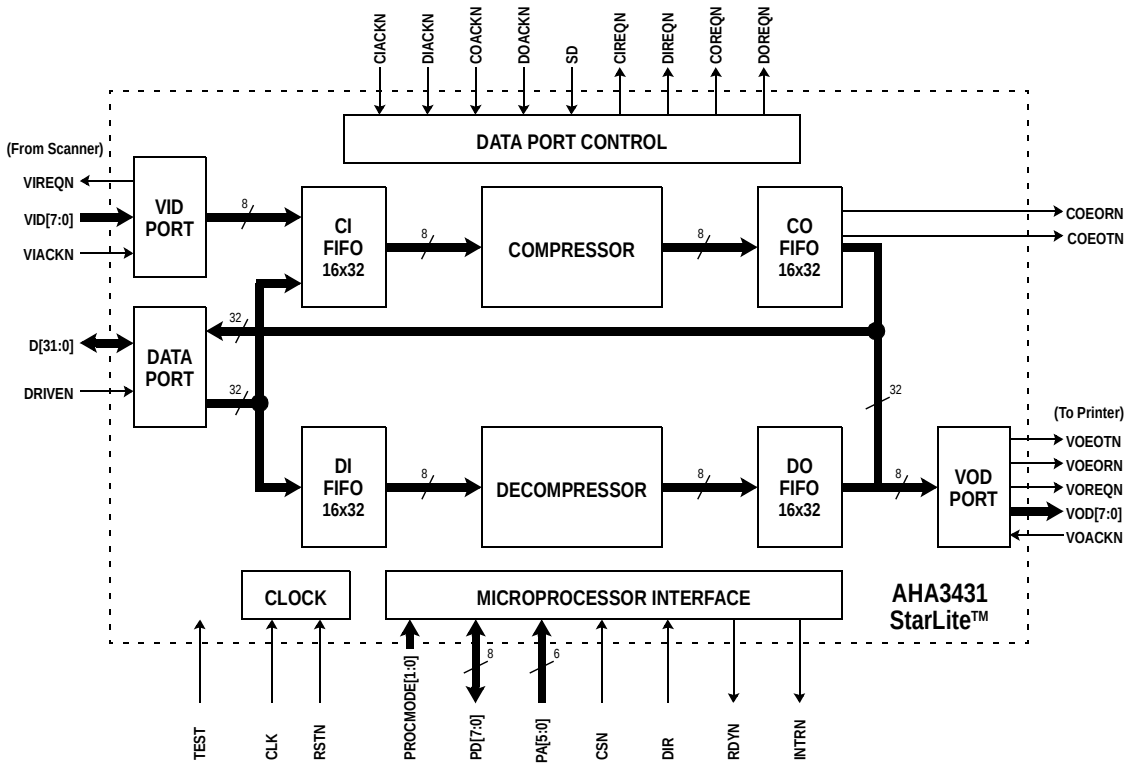
SYSTEM INTERFACE:

- Single chip compression/decompression solution – no external SRAM required
- Four 16 × 32-bit FIFOs with programmable threshold counters facilitate burst mode transfers

OTHERS:

- Low power modes
- Software emulation program available
- 128 pin quad flat package
- 3.3V operation
- Test pin tristates outputs
- Firmware, Register, Pinout and Functional compatible with 5V, AHA3411

Figure 1: Functional Block Diagram



1.3 FUNCTIONAL OVERVIEW

The coprocessor device has three external high speed synchronous data ports capable of transferring once every clock cycle. These are a 32-bit bidirectional data port, an 8-bit Video Input Data (VID) port and a Video Output Data (VOD) port. The 32-bit port is capable of transferring up to 4 bytes per clock. The VID and VOD are capable of up to one byte per clock.

The device accepts uncompressed data through the 8-bit VID port or the 32-bit data port into its Compression In FIFO (CI FIFO). The 32-bit data port may be configured for 16-bit transfers. Compressed data is available through the 32-bit data port via the Compressed Output FIFO (CO FIFO). The sustained data rate through the compression engine is one byte per clock.

Decompression data may be simultaneously processed by the device. Decompression data is accepted through the 32-bit data port, buffered in the Decompression Input FIFO (DI FIFO) and decompressed. The output data is made available on the 32-bit data port via the Decompression Output FIFO (DO FIFO) or the 8-bit Video Output port. The decompression engine is capable of processing an uncompressed byte every clock.

The four FIFOs are organized as 16×32 each. For data transfers through the three ports, the "effective" FIFO sizes differ according to their data bus widths. The table below shows the size of the data port and the "effective" FIFO size for the various configurations supported by the device.

Table 1: Data Bus and FIFO Sizes Supported by AHA3431

OPERATION	*DATA BUS WIDTH*	*PORT*	*EFFECTIVE FIFO SIZE*
Compression Data In	8	Video In	16 x 8
Compression Data In/Out	32	Data Port	16 x 32
Compression Data In/Out	16	Data Port	16 x 16
Decompression Data In/Out	32	Data Port	16 x 32
Decompression Data In/Out	16	Data Port	16 x 16
Decompressed Data Out	8	Video Out	16 x 8

Table 2: AHA3431 Connection to Host Microprocessors

PIN NAME	*i960Cx*	*i960Kx*	*IDT3081*	*Motorola MCFS102(ColdFIRE)*
PA	A	LAD	Latched Address	Latched Address
CSN	$\overline{CS}$	$\overline{CS}$	System Dependent	Decoded Chip Select
DIR	W/$\overline{R}$	W/$\overline{R}$	$\overline{WR}$	R/$\overline{W}$
PD	D	LAD	A/D	A/D[7:0]
SD	$\overline{WAIT}$	$\overline{READY}$	System Dependent	System Dependent
RDYN	No Connect	$\overline{READY}$	$\overline{ACK}$	$\overline{TA}$
DRIVEN	$\overline{DEN}$	System Dependent	System Dependent	System Dependent
CLOCK	PCLK	No Connect	$\overline{SYSCLK}$	BCLOCK

Movement of data for compression or decompression is performed using synchronous DMA over the 32-bit data port. The Video ports support synchronous DMA mode transfers. The DMA strobe conditions are configurable for the 32-bit data port depending upon the system processor and the available DMA controller.

Data transfer for compression or decompression is synchronous over the three data ports functioning as DMA masters. To initiate a transfer into or out of the Video ports, the device asserts VxREQN, the external device responds with VxACKN and begins to transfer data over the VID or VOD busses on each succeeding rising edge of the clock until VxREQN is deasserted. The 32-bit port relies on the FIFO Threshold settings to determine the transfer.

The sections below describe the various configurations, programming and other special considerations in developing a compression system using AHA3431.

2.0 SYSTEM CONFIGURATION

This section provides information on connecting AHA3431 to various microprocessors.

2.1 MICROPROCESSOR INTERFACE

The device is capable of interfacing directly to various processors for embedded application. Table 2 and Table 3 show how AHA3431 should be connected to various host microprocessors.

All register accesses to AHA3431 are performed on the 8-bit PD bus. The PD bus is the lowest byte of the 32-bit microprocessor bus. During reads of the internal registers, the upper 24 bits are not driven. System designers should terminate these lines with Pullup resistors.

AHA3431 provides four modes of operation for the microprocessor port. Both active high and active low write enable signals are allowed as well as two modes for chip select. The mode of operation is set by the PROCMODE[1:0] pins. The PROCMODE[1] signal selects when CSN must be active and also how long an access lasts.

When PROCMODE[1] is high, CSN determines the length of the access. CSN must be at least 5 clocks in length. On a read, valid data is driven onto PD[7:0] during the 5th clock. If CSN is longer than 5 clocks, then valid data continues to be driven out onto PD[7:0]. When CSN goes inactive (high), PD[7:0] goes tristate (asynchronously) and RDYN is driven high asynchronously. CSN must be high for at least two clocks. RDYN is always driven (it is not tristated when PROCMODE[1] is high). The mode is typical of processors such as the Motorola 68xxx.

When PROCMODE[1] is low, accesses are fixed at 5 clocks, PD[7:0] is only driven during the fifth clock, and RDYN is driven high for the first 4 clocks and low during the fifth clock. RDYN is tristated at all other times. Write data must be driven the clock after CSN is sampled low. Accesses may be back to back with no delays in between. This mode is typical of RISC processors such as the i960.

PROCMODE[0] determines the polarity of the DIR pin. If PROCMODE[0] is high, then the DIR pin is an active low write enable. If PROCMODE[0] is low, then the DIR pin is an active high write enable. Figure 2 through Figure 5 illustrate the detailed timing diagrams for the microprocessor interface.

For additional notes on interfacing to various microprocessors, refer to AHA Application Note (ANDC16), *Designer's Guide for StarLite™ Family Products*. AHA Applications Engineering is available to support with other processors not in the Designer's Guide.

Table 3: Microprocessor Port Configuration

PROCMODE[1:0]	*DIR*	*CYCLE LENGTH*	*EXAMPLE PROCESSOR*
00	Active high write	fixed	i960
01	Active low write	fixed	
10	Active high write	variable	
11	Active low write	variable	68xxx, MIPS R3000

Figure 2: Microprocessor Port Write (PROCMODE[1:0]="01")

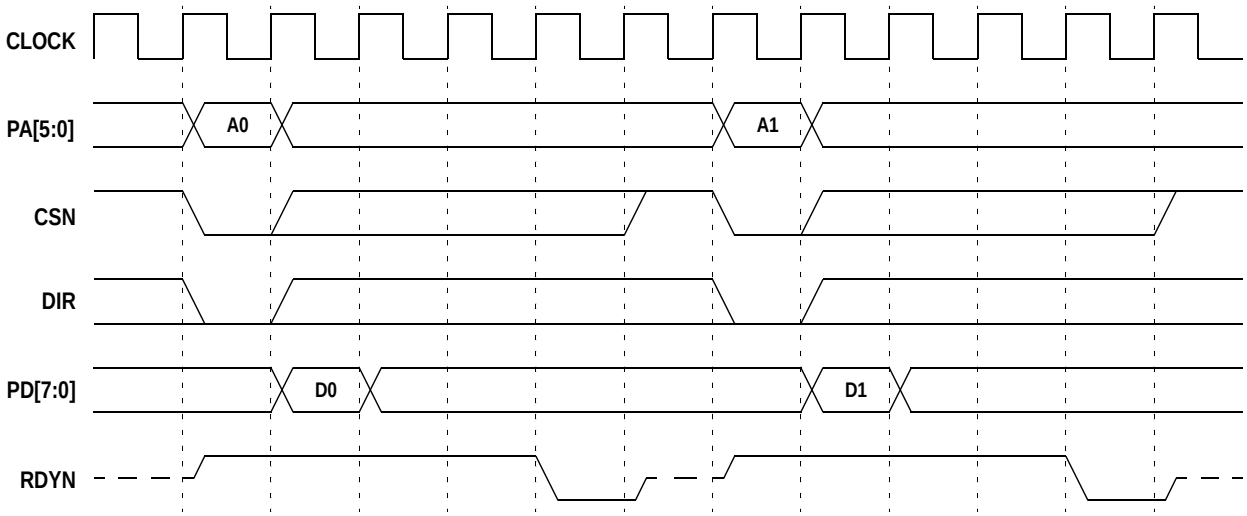


Figure 3: Microprocessor Port Read (PROCMODE[1:0]="01")

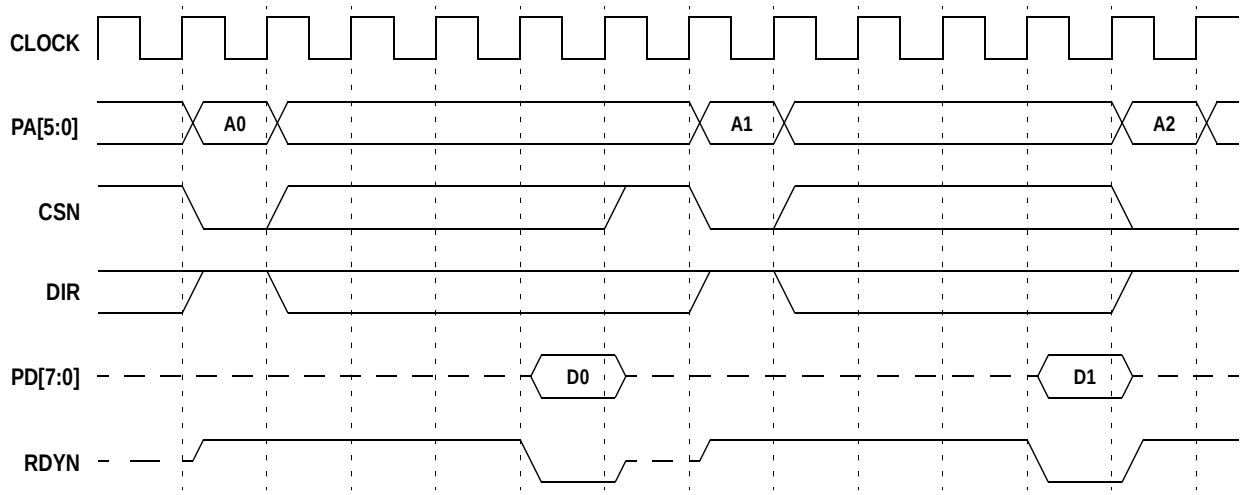


Figure 4: Microprocessor Port Write (PROCMODE[1:0]="11")

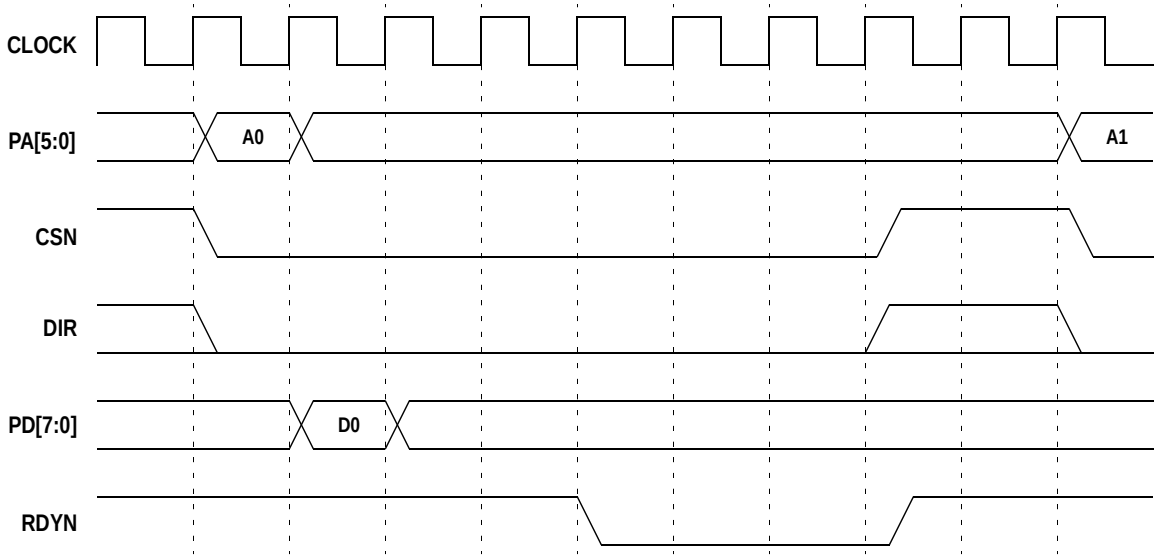
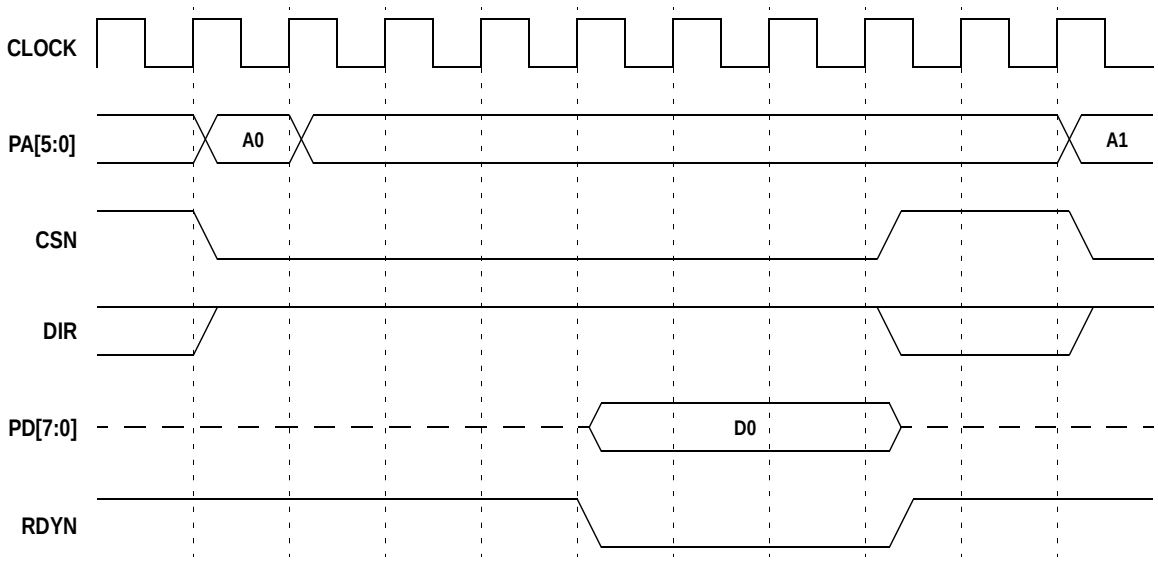


Figure 5: Microprocessor Port Read (PROCMODE[1:0]="11")



3.0 FUNCTIONAL DESCRIPTION

This section describes the various data ports, special handling, data formats and clocking structure.

3.1 DATA PORTS

AHA3431 contains two data input ports, CI and DI, and two data output ports, CO and DO on the same 32-bit data bus, D[31:0]. Data transfers are controlled by external DMA control. The logical conditions under which data is written to the input FIFOs or read from the output FIFOs are set by the DSC (Data Strobe Condition) field of the *System Configuration 1* register.

A strobe condition defines under what logical conditions the input FIFOs are written or the output FIFOs read. CIACKN, COACKN, DIACKN, DOACKN, and SD pins combine to strobe data in a manner similar to DMA controllers. The DMA Mode sub-section describes the various data strobe options.

3.2 DMA MODE

On the rising edge of CLOCK when the strobe condition is met, the port with the active acknowledge either strobes data into or out of the chip. No more than one port may assert acknowledge at any one time. Table 4 shows the various conditions that may be programmed into register DSC.

Figure 6 through Figure 11 illustrate the DMA mode timings for single, four word and eight word burst transfers for DSC=100 selection. For other DSC settings, please refer to Appendix A. Note that the only difference between odd and even values of DSC is the polarity of SD. Waveforms are only shown for polarities of SD corresponding to specific systems.

Table 4: Internal Strobe Conditions for DMA Mode

DSC[2:0]	*LOGIC EQUATION*	*SYSTEM CONFIGURATION*
000	$(\overline{ACKN})\&\ (\overline{ACKN_{delayed}})\&\ (SD)$	i960Cx with internal DMA controller. SD is connected to WAITN.
001	$(\overline{ACKN})\&\ (\overline{ACKN_{delayed}})\&\ (\overline{SD})$	No specific system
010	$(\overline{ACKN})\&\ (SD)$	General purpose DMA controller
011	$(\overline{ACKN})\&\ (\overline{SD})$	i960Kx with external, bus master type DMA controller. SD is connected to RDYN.
100	$(\overline{ACKN_{delayed}})\&\ (SD_{delayed})$	No specific system
101	$(\overline{ACKN_{delayed}})\&\ (\overline{SD_{delayed}})$	No specific system
110	$(ACKN)\&\ (\overline{ACKN_{delayed}})$	No specific system
111	$(ACKN)\&\ (\overline{ACKN_{delayed}})$	No specific system

$ACKN_{delayed}$ = $ACKN$ delayed 1 clock

$SD_{delayed}$ = SD delayed 1 clock

Figure 6: DMA Mode Timing for Single Word Writes, Strobe Condition of DSC=100

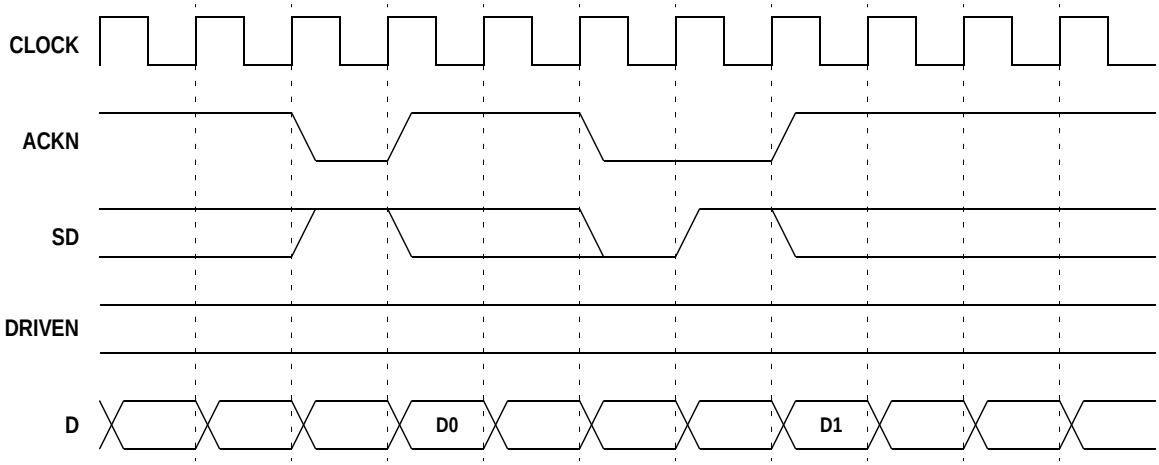


Figure 7: DMA Mode Timing for Single Word Reads, Strobe Condition of DSC=100

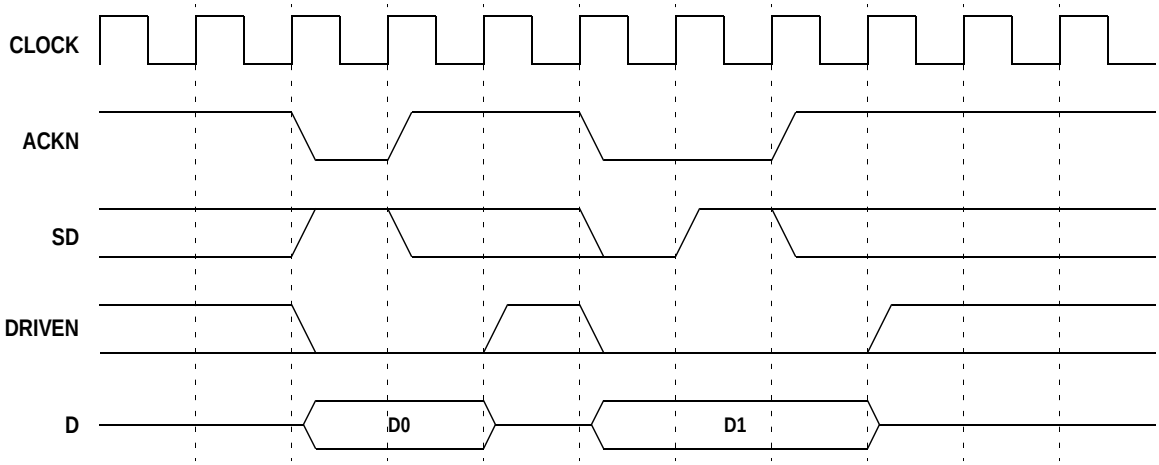


Figure 8: DMA Mode Timing for Four Word Burst Write, One Wait State, Strobe Condition of DSC=100

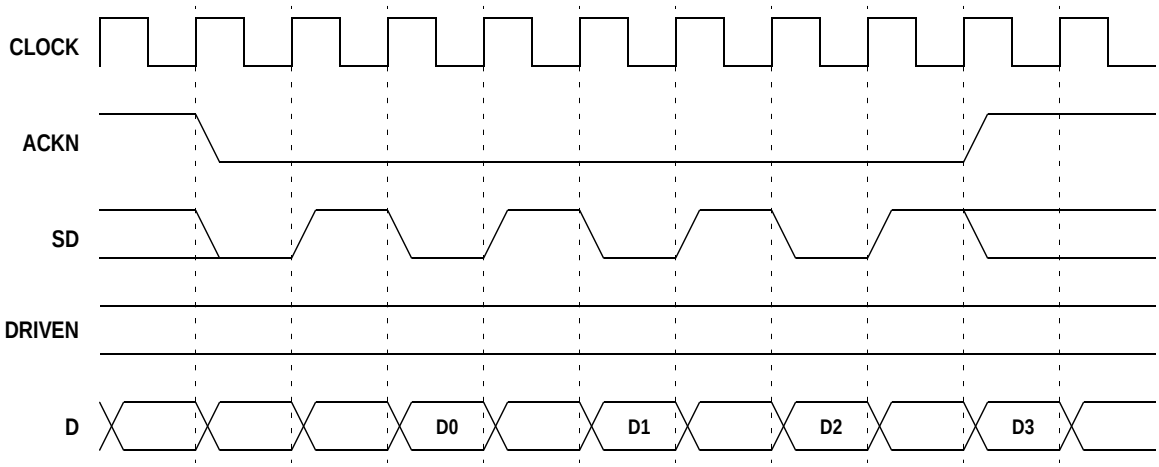


Figure 9: DMA Mode Timing for Four Word Burst Read, One Wait State, Strobe Condition of DSC=100

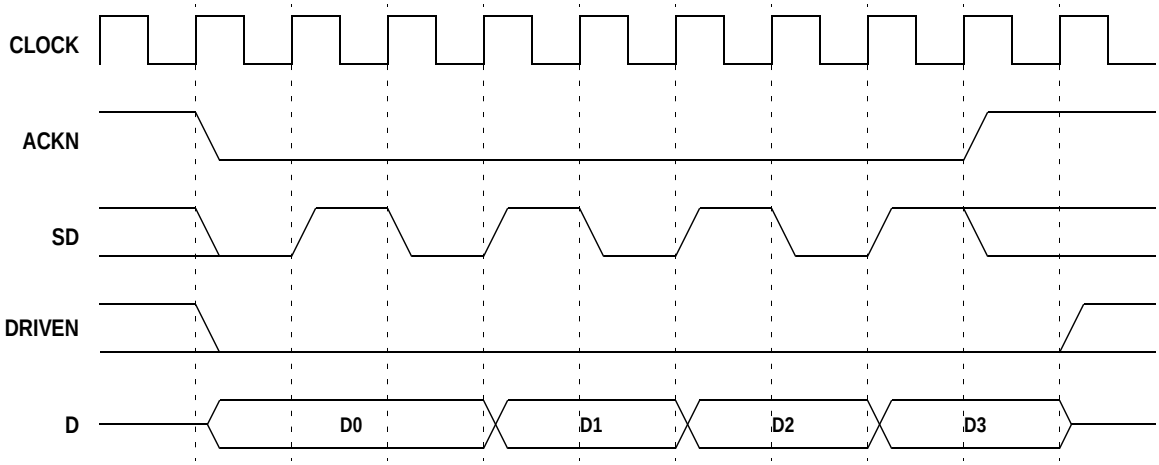


Figure 10: DMA Mode Timing for Eight Word Burst Write, Zero Wait State, Strobe Condition of DSC=100

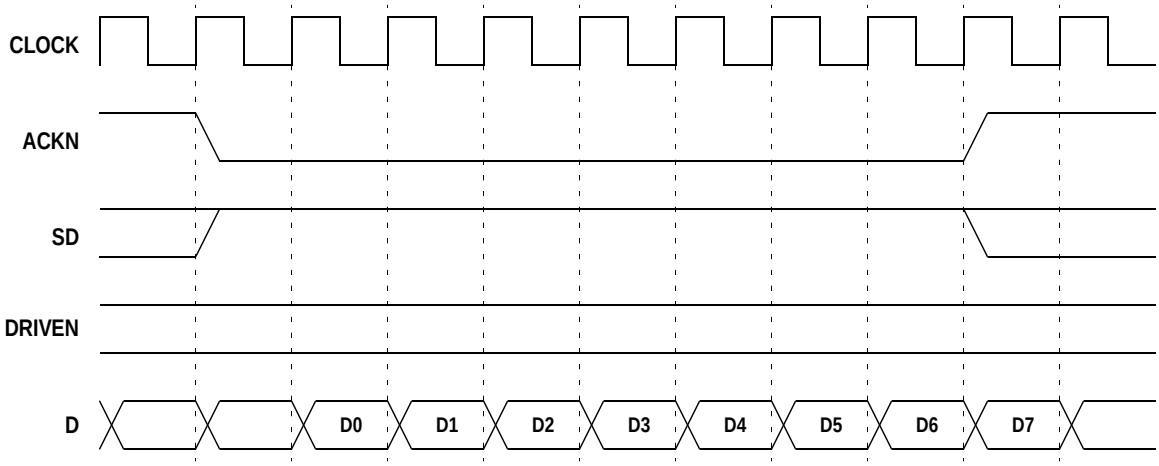
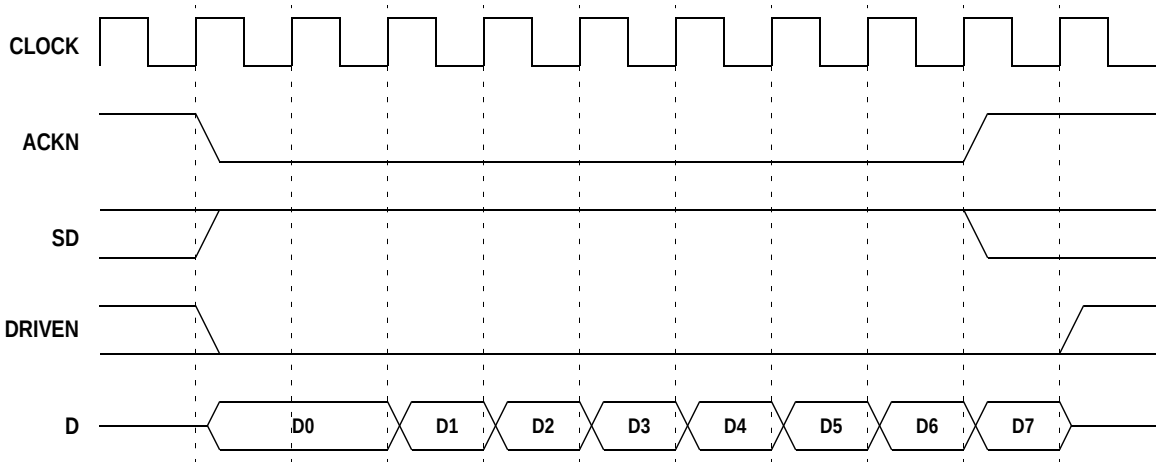


Figure 11: DMA Mode Timing for Eight Word Burst Read, Zero Wait State, Strobe Condition of DSC=100



3.3 PAD WORD HANDLING IN BURST MODE

The StarLite™ compression algorithm appends a 15 bit End-of-Record codeword to terminate a compression record. If a word containing an End-of-Record comes out during a burst read, the words following the End-of-Record are invalid (pad) words. This prevents a burst read from crossing record boundaries. The first word of the next burst read is the first word of the next record. Any pad words not previously removed must be deleted.

Two methods are available to delete pad words. During decompression pad words may be deleted by using the Decompression Pause on Record Boundaries bit (DPOR), in the Decompression Control register. After the part is paused, the DI FIFO must be reset by asserting the DIRST bit in the Port Control register. Decompressor must also be reset by asserting DDR bit in Decompression Control register. The COEOTN signal is asserted when an End-of-Record is present on the output of the CO FIFO and the compression record counter has decremented to zero, thus indicating the end of a transfer comprised of one or more compressed records.

Another method to remove pad words during compression is to read the Compressed Byte Count register after pausing at an End-of-Record and subtract this from the system's received word count. This difference is the number of pad words that must be removed from the end of the compressed record.

The COEORN signal is asserted when an End-of-Record is present on the output of the CO FIFO. COEORN is deasserted after the transfer. In some systems COEORN can be used to generate a DMA-done condition if conditioned with the acknowledge.

3.4 DMA REQUEST SIGNALS AND STATUS

AHA3431 requests data using request pins (CIREQN, DIREQN, COREQN, DOREQN). The requests are controlled by programmable FIFO thresholds. Both input and output FIFOs have programmable empty and full thresholds set in the *Input FIFO Threshold* and *Output FIFO Threshold* registers. By requesting only when a FIFO can sustain a certain burst size, the bus is used more efficiently.

Operation of these request signals should not be confused with the request signals on the video ports. CIREQN or DIREQN active indicates space available in the particular input FIFO, and COREQN or DOREQN active indicates data is available in the particular output FIFO. These request signals inactive does not prevent data transfers. The data transfers are controlled solely with the particular acknowledge signal being active.

The input requests, CIREQN and DIREQN, operate under the following prioritized rules, listed in order of highest to lowest:

1) If the FIFO reset in the *Port Control* register is active, the request is inactive.
2) If a FIFO overflow interrupt is active, the request is inactive.
3) If the FIFO is at or below the empty threshold, the request remains active.
4) If the FIFO is at or above the full threshold, the request stays inactive.

The output requests, COREQN and DOREQN, operate under the following prioritized rules, listed in order of highest to lowest:

1) If the FIFO reset in the *Port Control* register is active, the request is inactive.
2) If the output FIFO underflow interrupt is active, the request is inactive.
3) If an EOR is present in the output FIFO, the request goes active.
4) If the output FIFO is at or above the full threshold, the request goes active.
5) If an EOR is read (strobed) out of the FIFO, the request goes inactive during the same clock as the strobe (if ERC=0), otherwise it goes inactive on the next clock.
6) If the output FIFO is at or below the empty threshold, the request goes inactive.

3.4.1 FIFO THRESHOLDS

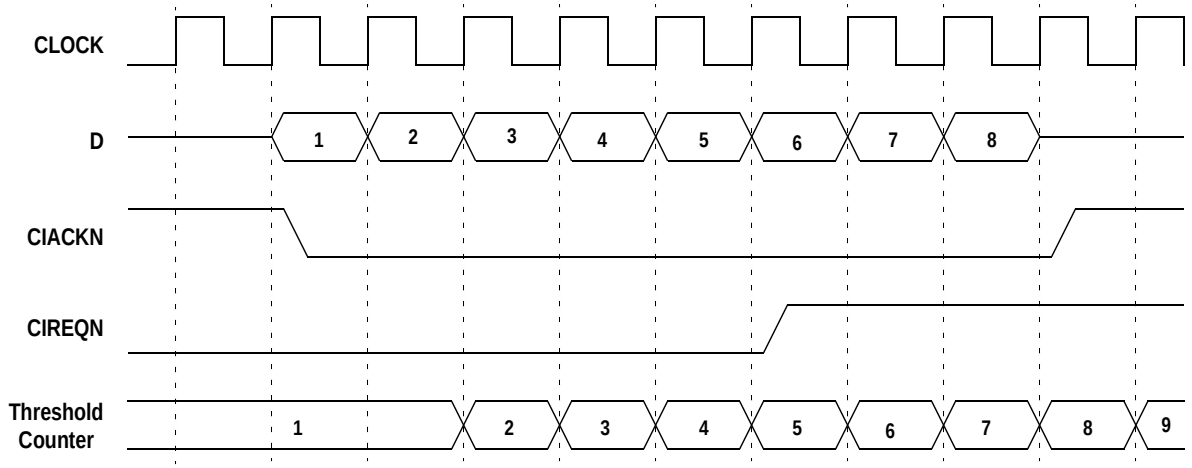
For maximum efficiency, the FIFO thresholds should be set in such a way that the compressor seldom runs out of data from the CI FIFO or completely fills the output FIFO. The FIFOs are 16 words deep.

For example, in a system with fixed 8-word bursts, good values for the thresholds are:

IET=3, IFT=4, OFT=D, OET=C

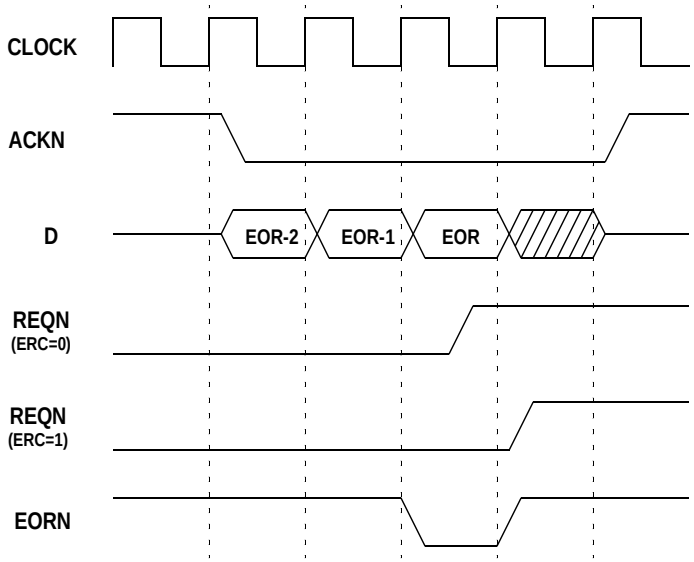
Setting the input full threshold to one higher than the input empty threshold simply guarantees that the request deasserts as soon as possible. The latency between a word being strobed in and the request changing due to a FIFO threshold condition is 3 clocks. This should be kept in mind when programming threshold values. Refer to Section 4.0 of AHA Application Note (ANDC16), *Designer's Guide for StarLite™ Family Products* for a more thorough discussion of FIFO thresholds. The following figure shows an example of an input FIFO crossing its full threshold.

Figure 12: FIFO Threshold Example (IFT=4, DSC=2, 1 Word Already in FIFO)



Note: CIREQN deasserted when threshold counter exceeds IFT=4, but additional words are reading as long as ACKN is asserted.

Figure 13: Request vs. End-of-Record, Strobe Condition of DSC=010



3.4.2 REQUEST DURING AN END-OF-RECORD

The request deasserts at an EOR in one of two ways. If ERC bit in *System Configuration 1* is zero, the request deasserts asynchronously during the clock where the EOR is strobed out of the FIFO. This leads to a long output delay for REQN, but may be necessary in some systems. For DSC values of 4 or 5, the request deasserts the first clock after the acknowledge pulse for the EOR. If ERC is set to one, then the request deasserts synchronously the clock after the EOR is strobed out. The minimum low time on the request in this case is one clock.

The request delay varies between the different strobe conditions. See Section 8.0 *AC Electrical Specifications* for further details.

3.4.3 REQUEST STATUS BITS

An external microprocessor can also read the value of each request using the CIREQ and COREQ bits in the *Compression Port Status* register and the DIREQ and DOREQ bits in the *Decompression Port Status* register. Please note the request status bits are active high while the pins are active low.

3.5 DATA FORMAT

The width of the D bus is selected with the WIDE bit in *System Configuration 0*. If WIDE=1, then D is a 32-bit bus. If WIDE=0, D is a 16-bit bus. If the bus is configured to be 16-bits wide (WIDE=0), all data transfers occur on D[15:0] and the upper 16 bits of the bus, D[31:16], should be terminated with Pullup resistors. If WIDE=0, the FIFO is sixteen words deep.

Since the compression algorithm is byte oriented, it is necessary for AHA3431 to know the ordering of the bytes within the word. The COMP and DECOMP BIG bits in *System Configuration 0* select between big endian and little endian byte ordering for the compression and decompression channel. Little endian stores the first byte in the lower eight bits of a word (D[7:0]). Big endian stores the first byte in the uppermost eight bits of a word (D[31:24] for WIDE=1, D[15:8] for WIDE=0) for the decompression engine or compression engine.

REVERSE BYTE in the *System Configuration 0* register allows the bit order into the compression engine to be swapped. This control is useful for reversing a page of data for duplex printing applications and has no significant impact on compression ratio performance.

3.6 ODD BYTE HANDLING

All data transfers to or from either the compression or decompression engines are performed on the D bus on word boundaries. Since no provision is made for single byte transfers, occasionally words will contain pad bytes. Following is a description of when these pad bytes are necessary for each of the data interfaces.

3.6.1 COMPRESSION INPUT AND PAD BYTES

Uncompressed data input into AHA3431 is treated as records. The length of these records is fixed by the value in the *Record Length* or RLEN register. This register contains the number of uncompressed bytes in each record. If the value in RLEN is not an integer multiple of number of bytes per word as selected by WIDE, the final word in the transfer of the record contains pad bytes. The compression engine simply discards these pad bytes and has no effect on either the dictionary or the output data stream. The next record must begin on a word boundary.

The minimum value for RLEN is 4 bytes.

3.6.2 COMPRESSION OUTPUT AND PAD BYTES

If a record ends on a byte other than the last byte in a word, the final word contains 1, 2 or 3 pad bytes. The pad bytes have a value of 0x00. This applies to the 32-bit data port only.

3.6.3 DECOMPRESSION INPUT, PAD BYTES AND ERROR CHECKING

This port recognizes the end of a record by the appearance of a special End-of-Record sequence in the data stream. Once this is seen, the remaining bytes in the current word are treated as pad bytes and discarded. The word following the end of the record is the beginning of the next record.

When operating in decompression mode, the *Decompression Record Length* (DRLEN) register can be used to provide error checking. The expected length of the decompressed record is programmed into the DRLEN register. The decompressor then counts down from the value in DRLEN to zero.

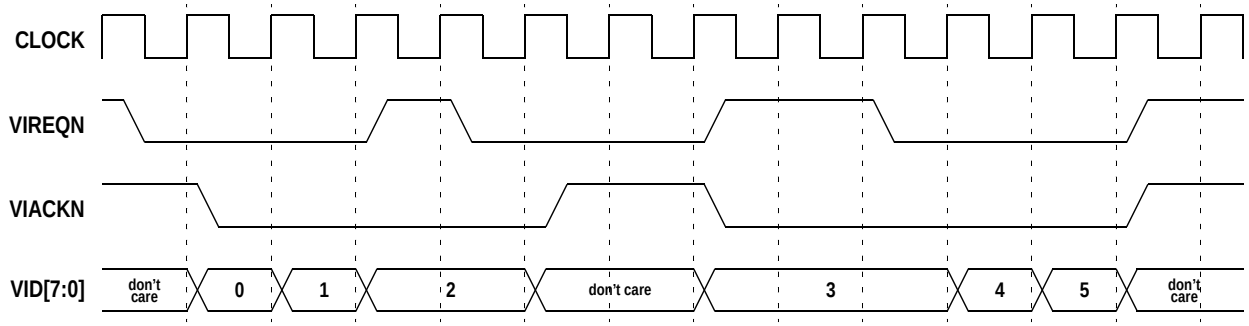
A DERR interrupt is issued if an EOR is not read out of the decompressor when the counter expires or if an EOR occurs before the counter expires (i.e., when the record lengths do not match). If the DERR interrupt is masked, use of the DRLEN register is optional.

When operating in pass-through mode, there is no End-of-Record codeword for the decompressor to see. In pass-through mode, the user must set the record length in the DRLEN register.

3.6.4 DECOMPRESSION OUTPUT AND PAD BYTES

When the decompressor detects an End-of-Record codeword, it will add enough pad bytes of value 0x00 to complete the current word as defined by the WIDE bit in the *System Configuration 0* register. For example, if a record ends on a byte other than the last byte in a word, the final word contains 1, 2 or 3 pad bytes. This applies to the 32-bit data port only, not the VOD port. The VOD port never outputs pad bytes since it is 8-bits wide.

Figure 14: Timing Diagram, Video Input



3.7 VIDEO INTERFACES

3.7.1 VIDEO INPUT

The video input port is enabled by the VDIE bit in the *System Configuration 1* register. The port uses VIREQN to indicate that the port can accept another byte. The value on VID[7:0] is written into AHA3431 each clock that VIREQN and VIACKN are both low.

The video input port asserts VIREQN whenever there is room in the CI FIFO. The values in IET and IFT are all ignored. The compression input FIFO is 16 bytes deep in this mode. The video input port can transfer up to one byte per clock (33 MB/sec). The DMA interface cannot access the compression input FIFO when VDIE is set.

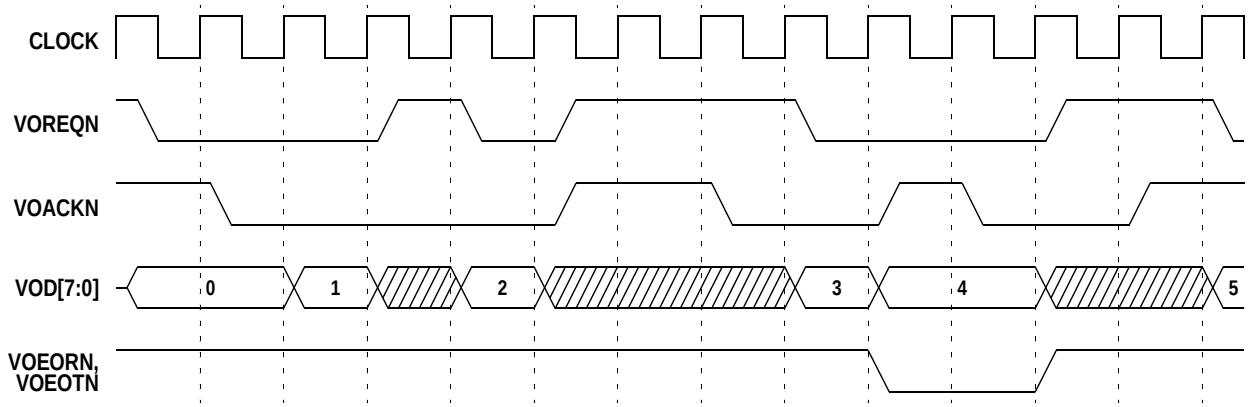
3.7.2 VIDEO OUTPUT

The video output port is enabled by the VDOE bit in the *System Configuration 1* register. The port uses VOREQN to indicate that the byte on VOD[7:0] is valid. An 8-bit word is read each clock when both VOREQN and VOACKN are sampled low on a rising edge of CLOCK. Pad bytes at an end of record are discarded by the video output port and do not appear on VOD[7:0]. When the byte on VOD[7:0] is the last byte in a record, the VOEORN signal goes low. To use VOEORN as an End-of-Record indicator, it should be conditioned with VOREQN and VOACKN. Unlike a DMA transfer, there are no pad bytes after an End-of-Record.

VOEOTN operates similar to VOEORN. It flags the end of an output transfer of one or more decompressed records. VOEOTN is asserted when the End-of-Record is at the output of the DO FIFO and the decompression record count has decremented to zero.

The port requests whenever a valid byte is present on the output. The values in OET and OFT are all ignored. The decompression output FIFO is 16 bytes deep in this mode. The video output port can output up to one byte per clock. The DMA interface cannot access the decompression output FIFO when VDOE is set.

Figure 15: Timing Diagram, Video Output



3.8 ALGORITHM

AHA3431 compression is an efficient implementation of an algorithm optimized for bitonal images. For some comparison data refer to the AHA Application Note (ANDC13), *Compression Performance: StarLite™: ENCODEB2 on Bitonal Images*. A software emulation of the algorithm is available for evaluation.

3.9 COMPRESSION ENGINE

The compression engine supports either compression or pass-through processes. The compression engine is enabled with the COMP bit in the *Compression Control* register. When the engine is enabled, it takes data from the CI FIFO as it becomes available. This data is either compressed by the engine or passed through unaltered. This pass-through mode is selected with the CPASS bit in the *Compression Control* register. The CPASS bit may only be changed when COMP is set to '0'. The contents of the dictionary are preserved when COMP is changed. However, when CPASS is changed, the contents are lost. Consequently, the device cannot be changed from pass-through mode to compression mode or vice versa without losing the contents of the dictionary.

The compressor can be instructed to halt at the end of a record or an end of multiple-record transfer. If the CPOR bit is set, the compressor stops taking data out of the CI FIFO immediately after the last byte of a record, and the COMP bit is cleared. If the CPOT bit is set the compressor halts at the end of the multiple-record transfer. The CEMP bit indicates the compressor has emptied all data. Compression is restarted by setting the COMP bit.

The compression engine takes data from the compression input FIFO at a maximum rate of 33 MBytes/sec. Two conditions cause the data rate to drop below the maximum. The first is caused by the compression input FIFO running empty of data to be compressed. The second condition is caused by the output FIFO filling. When this occurs, the engine halts and waits for the FIFO. While halted, the engine goes into a low power standby mode. Refer to the table in Section 7.1 for the extent of power savings.

The compression byte counter counts the number of bytes output from the CO data port. The counter is valid to read after a compression end of transfer interrupt (CEOT), or pausing after End-of-Record.

3.10 DECOMPRESSION ENGINE

The decompression engine is enabled with the DCOMP bit in the *Decompression Control* register. When the engine is enabled, it takes data from the DI FIFO as it becomes available. This data is either decompressed by the engine or passed through unaltered. Pass-through mode is selected with the DPASS bit. DPASS may only be changed when DCOMP is set to zero and DEMP is set to one. The contents of the dictionary are preserved when DCOMP is changed. However, when DPASS is changed, the contents are lost. Consequently, AHA3431 cannot be changed from pass-through mode to decompression mode or vice versa without losing the contents of the dictionary.

The decompressor can be instructed to halt at the end of a record or an end of multiple-record transfer. If the DPOR bit is set, the decompressor stops taking data out of the DI FIFO immediately after the last byte of a record, and the DCOMP bit is cleared. If DPOT bit is set the decompressor halts at the end of the multiple-record transfer. The DEMP bit indicates the decompressor has emptied of all data. Decompression is restarted by setting the DCOMP bit. If DPOR or DPOT is set and data from a second record enters the FIFO immediately after the first record, bytes from the second record will have entered the decompressor prior to decoding the EOR. An implication of this is that bytes from the second record will remain in the decompressor and prevent DEMP from setting after all of the data from the first record has left the decompressor. This differs from operation of the compression engine. In either mode, a DEOR interrupt is generated when the last byte of a decompressed record is read out of the chip, and DEOT when the last byte of a transfer is read out of the chip.

The decompressor takes data from the decompression input FIFO at the maximum clock rate. AHA3431 can maintain this data rate as long as the decompression input FIFO is not empty or the decompression output FIFO is not full.

Caveat: Changing the mode for the decompressor between records or multiple-record transfers must be done with the data of the following record or transfer held off until the DEOR status bit is true for the current record and the *Decompression Control* registers have been reprogrammed. This reprogramming can occur automatically with prearming.

3.11 PREARMING

Prearming is the ability to write certain registers that apply to the next record while the device is processing the current record. Prearming occurs automatically at the end of a record. If a prearmable register is written while the part is busy processing a record, at the end of the record the part takes its program from the register value last written. Compression Control and Decompression Control registers each have separate corresponding prearm registers.

The lower 3 bytes of both the *Compression Record Length* and the *Decompression Length* registers are prearmable. They may be changed and the new values loaded into the respective counter at the next End-of-Record. If the most significant byte is written in either of the *Record Length* registers, the counter is immediately reloaded with the new 4 byte value in the particular register.

3.12 INTERRUPTS

Nine conditions are reported in the *Interrupt Status/Control 1* and *Status/Control 2* registers as individual bits. All interrupts are maskable by setting the corresponding bits in the *Interrupt Mask* register. A one in the *Interrupt Mask* register means the corresponding bit in the *Interrupt Status/Control* register is masked and does not affect the interrupt pin (INTRN). The INTRN pin is active whenever any unmasked interrupt bit is set to a one.

An End-of-Record interrupt is posted when a word containing an end-of-record is strobed out of the compression or decompression output FIFO (CEOR and DEOR respectively). A DEOR interrupt is also reported if an end-of-record is read from the video output port. A compression or decompression end of transfer interrupt will also be posted if this is the last record of a transfer.

End-of-Transfer interrupts are posted when an EOR occurs that causes the counter to decrement to zero. These are CEOT and DEOT, and they apply to both the compression and decompression engines respectively.

Four FIFO error conditions are also reported. Overflowing the input FIFOs generates a CIOF or DIOF interrupt. An overflow can only be cleared by resetting the respective FIFO via the *Port Control* register.

Underflowing the output FIFOs (reading when they are not ready) generates a COUF or DOUF. Underflow interrupts are cleared by writing a one to COUF or DOUF. In the event of an underflow, the respective FIFO must be reset. Note that in systems using fixed length bursts which rearbitrate during a burst, the CO FIFO may request another burst when the record actually finishes near the end of the current burst. In this scenario a second burst takes place causing a FIFO underflow. As long as a pause on End-of-Record is used, data is not corrupted. The FIFO simply must be reset.

3.13 DUPLEX PRINTING

Duplex Printing is the ability to print on both sides of the page. AHA3431 supports this with separate endian control for the Compressor and Decompressor, and bit order control at the input to the compressor. Bit order control allows reversal of the data bits within each byte of data. For example, reverse order means bit-7 is swapped with bit-0, bit-6 is swapped with bit-1, etc.... During compression operation of the back side of the page the data words are sent to the AHA3431 device in reverse order. The byte order is swapped if necessary by the COMP BIG bit in the System Configuration 0 Register. The bit order within each byte is reversed with the REVERSE BYTE bit in this same register.

During decompression of this reversed page the DECOMP BIG bit in this register must be programmed to the same value used when this page of data was compressed. Use of this feature has virtually no effect on the compression ratio when compared to compressing in forward order.

3.14 BLANK BANDS

Setting DBLANK in the *Decompression Control* register causes the next record output from the Decompressor to be comprised of a repeating 8-bit pattern defined by the *Pattern* register. DBLANK automatically clears at the end of the next record. This command bit may be prearmed by writing to the *Decompression Control Prearm* register. When programming the device to generate blank records the system must not send data to be decompressed until the device has reached the end of record for the blank record.

3.15 LOW POWER MODE

The AHA3431 is a data-driven system. When no data transfers are taking place, only the clock and on-chip RAMs including the FIFOs require power. To reduce power consumption to its absolute minimum, the user can stop the clock when it is high. With the system clock stopped and at a high level, the current consumption is due to leakage. *Control* and *Status* registers are preserved in this mode. Reinitialization of *Control* registers are not necessary when switching from Low Power to Normal operating mode.

3.16 TEST MODE

In order to facilitate board level testing, the AHA3431 provides the ability to tristate all outputs. When the TEST0 pin is high, all outputs of the chip are tristated. When TEST0 is low, the chip returns to normal operation.

4.0 REGISTER DESCRIPTIONS

The microprocessor configures, controls and monitors IC operation through the use of the registers defined in this section. The bits labeled "*res*" are reserved and must be set to zero when writing to registers unless otherwise noted.

A summary of registers is listed below.

Table 5: Internal Registers

ADDRESS	*R/W*	*DESCRIPTION*	*FUNCTION*	*DEFAULT AFTER RSTN*	*PREARM*
0x00	R/W	System Configuration 0	Big Endian vs. Little Endian, 32-bit vs. 16-bit, Reverse Byte	Undefined	No
0x01	R/W	System Configuration 1	Data Strobe Condition, EOR Request Control, VDO Port Enable, VDI Port Enable	0x00	No
0x02	R/W	Input FIFO Thresholds	Input FIFOs Empty Threshold, Full Threshold	Undefined	No
0x03	R/W	Output FIFO Thresholds	Output FIFOs Empty Threshold, Full Threshold	Undefined	No
0x04	R	Compression Ports Status	FIFO Status, Request Status, EOR Status	Undefined	No
0x05	R	Decompression Ports Status	FIFO Status, Request Status, EOR Status	Undefined	No
0x06	R/W	Port Control	Reset Individual FIFOs	0x0F	No
0x07	R/W	Interrupt Status/Control 1	EOR, Overflow, Underflow	0x00	No
0x09	R/W	Interrupt Mask 1	Interrupt Mask bits	0xFF	No
0x0A	R	Version	Die Version Number	0x31	No
0x0C	R/W	Decompression Record Length 0	Bytes Remaining, Byte 0	0xFF	Yes
0x0D	R/W	Decompression Record Length 1	Bytes Remaining, Byte 1	0xFF	Yes
0x0E	R/W	Decompression Record Length 2	Bytes Remaining, Byte 2	0xFF	Yes
0x0F	R/W	Decompression Record Length 3	Bytes Remaining, Byte 3	0xFF	No
0x10	R/W	Compression Record Length 0	Length of Uncompressed Data in Bytes, Byte 0	Undefined	Yes
0x11	R/W	Compression Record Length 1	" " , Byte 1	Undefined	Yes
0x12	R/W	Compression Record Length 2	" " , Byte 2	Undefined	Yes
0x13	R/W	Compression Record Length 3	" " , Byte 3	Undefined	No
0x14	R/W	Compression Control	Pause on Record Boundaries, Enable Compression, Compression Engine Empty Status, Compression Dictionary Reset, Select Pass-Through Mode	0x04	Yes
0x15	R/W	Compression Reserved	Reserved	0x00	No
0x16	R/W	Compression Line Length 0	Line Length Register Lower 8 bits	Undefined	No
0x17	R/W	Compression Line Length 1	Line Length Register Upper 3 bits	Undefined	No

ADDRESS	R/W	DESCRIPTION	FUNCTION	DEFAULT AFTER RSTN	PREARM
0x18	R/W	Decompression Control	Pause on Record Boundaries, Enable Decompression Engine, Decompression Engine Empty Status, Dictionary Reset, Enable Pass-Through Mode	0x04	Yes
0x1A	R/W	Decompression Reserved 1	Reserved	0x00	No
0x1C	R/W	Decompression Line Length 0	Line Length Register Lower 8 bits	Undefined	No
0x1D	R/W	Decompression Line Length 1	Line Length Register Upper 3 bits	Undefined	No
0x20	R/W	Compression Record Count 0	Compressor number of records in a transfer	0xFF	No
0x21	R/W	Compression Record Count 1	Compressor number of records in a transfer	0xFF	No
0x27	R/W	Interrupt Status/Control 2	Compression EOT Interrupt, Decompression EOT Interrupt	0x00	No
0x29	R/W	Interrupt Mask 2	Interrupt Mask bits for CEOT, DEOT	0xFF	No
0x2C	R/W	Decompression Record Count 0	Decompressor number of records in a transfer	0xFF	No
0x2D	R/W	Decompression Record Count 1	Decompressor number of records in a transfer	0xFF	No
0x30	R	Compression Byte Count 0	Compressed byte count, byte 0	0x00	No
0x31	R	Compression Byte Count 1	Compressed byte count, byte 1	0x00	No
0x32	R	Compression Byte Count 2	Compressed byte count, byte 2	0x00	No
0x33	R	Compression Byte Count 3	Compressed byte count, byte 3	0x00	No
0x34	R/W	Compression Control Prearm	Prearm Register for Compression Control	0x00	No
0x35	R/W	Pattern	8-bit pattern for blank record generation	Undefined	No
0x38	R/W	Decompression Control Prearm	Prearm Register for Decompression Control	0x00	No
0x3A	R/W	Decompression Reserved 2	Reserved	0x00	No
0x3F		*Reserved*	Reserved	0x0F	No

4.1 SYSTEM CONFIGURATION 0, ADDRESS 0x00 - READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x00	*res*	WIDE	*res*			REVERSE BYTE	DECOMP BIG	COMP BIG

After reset, its contents are undefined. It must be written before any input or output data movement may be performed.

COMP BIG-Selects between little or big endian byte order for the compressor. See table.

DECOMP BIG-Selects between little or big endian byte order for the decompressor. See table.

REVERSE BYTE- When this bit is one the byte data entering the compressor is reversed. Bit0 is swapped with bit7, bit1 is swapped with bit6, bit2 is swapped with bit5, etc. . .

res - Bits must always be written with zeros.

WIDE - Selects between 32 and 16-bit D buses.

COMP BIG or DECOMP BIG	WIDE	DESCRIPTION
0	0	Little Endian data order, 16-bit words D[15:8] Byte 1, D[7:0] Byte 0
0	1	Little Endian data order, 32-bit words D[31:24] Byte 3, D[23:16] Byte 2, D[15:8] Byte 1, D[7:0] Byte 0
1	0	Big Endian data order, 16-bit words D[15:8] Byte 0, D[7:0] Byte 1
1	1	Big Endian data order, 32-bit words D[31:24] Byte 0, D[23:16] Byte 1, D[15:8] Byte 2, D[7:0] Byte 3

4.2 SYSTEM CONFIGURATION 1, ADDRESS 0x01 - READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x01	*res*	VDIE	VDOE	ERC	*res*	DSC[2:0]		

This register is cleared by reset.

DSC[2:0] - Data Strobe Condition. Control the condition used to strobe data into and out of the data ports on the D bus. Table 4 shows the programming for the strobe condition for various DMA modes.

res - Bits must always be written with zeros.

ERC - EOR Request Control. Determines when COREQN and DOREQN deassert at an End-of-Record. If ERC=0, then the request deasserts asynchronously during the clock when an EOR is strobed out. If ERC=1, then the request deasserts synchronously the clock after an EOR is strobed out. See Figure 18 through Figure 21.

VDOE - VDO Port Enable. When this bit is set, the data from the decompression output FIFO goes to the VDO port. When the bit is clear, the decompressed data is read by DMA on the D bus.

VDIE - VDI Port Enable. When this bit is set, the VDI port handshakes data and writes it into the compression input FIFO. When the bit is clear, the compression input FIFO is written by DMA from the D bus.

4.3 INPUT FIFO THRESHOLDS, ADDRESS 0x02 - READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x02	IFT[3:0]				IET[3:0]			

After reset, its contents are undefined. It must be written before any input or output data movement may be performed.

IET[3:0] - Empty threshold for input FIFOs. If the number of words in the input FIFO (CI or DI) is less than or equal to this number, the request for that channel is asserted.

IFT[3:0] - Full threshold for input FIFOs. If the number of words in the input FIFO (CI or DI) is greater than or equal to this number, the request for the channel is deasserted.

4.4 OUTPUT FIFO THRESHOLDS, ADDRESS 0x03 - READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x03	OFT[3:0]				OET[3:0]			

After reset, its contents are undefined. It must be written before any input or output data movement may be performed.

OET[3:0] - Empty threshold for output FIFOs. If the number of words in the output FIFO (CO or DO) is less than or equal to this number, the request for the channel is deasserted (except in the case of an End-of-Record).

OFT[3:0] - Full threshold for output FIFOs. If the number of words in the output FIFO (CO or DO) is greater than or equal to this number, the request for that channel is asserted.

4.5 COMPRESSION PORTS STATUS, ADDRESS 0x04 - READ ONLY

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x04	COEMP	CIEMP	res	CEOR	COREQ	COET	CIREQ	CIFT

This is a read only register. Writing to this register has no effect. After reset, its contents are undefined.

CIFT - Compression input FIFO full threshold. This signal is active when the CI FIFO is greater than or equal to the programmed FIFO full threshold. After reset and the *Input FIFO Threshold* register has been written, this bit contains a zero.

CIREQ - Compression input request signal state. Reports the current state for the CIREQN pin. Notice that this bit is active high while the pin is active low. Therefore, the value of this bit is always the inverse of the value of the signal. After reset this bit contains a zero.

COET - Compression output FIFO empty threshold. This bit is active when the CO FIFO is less than or equal to the programmed FIFO empty threshold. After reset and the *Output FIFO Threshold* register has been written, this bit contains a one.

COREQ - Compression output request signal state. Reports the current state for the COREQN pin. Notice that this bit is active high while the pin is active low. Therefore, the value of this bit is always the inverse of the value of the signal. After reset this bit contains a zero.

CEOR - Compression output end of record. This bit is active when the output FIFO contains the end-of-record code. After reset this bit contains a zero.

res - Bits must always be written with zeros.

CIEMP - Compression input empty. This bit is active when the CI FIFO is empty. After reset this bit contains a one.

COEMP - Compression output empty. This bit is active when the CO FIFO is empty. After reset this bit contains a one.

4.6 DECOMPRESSION PORTS STATUS, ADDRESS 0x05 - READ ONLY

Address	***bit7***	***bit6***	***bit5***	***bit4***	***bit3***	***bit2***	***bit1***	***bit0***
0x05	DOEMP	DIEMP	res	DEOR	DOREQ	DOET	DIREQ	DIFT

This is a read only register. Writing to this register has no effect. After reset, its contents are undefined.

DIFT - Decompression input FIFO full threshold. This signal is active when the DI FIFO is at or above the programmed FIFO full threshold. After reset and the *Input FIFO Threshold* register has been written, this bit contains a zero.

DIREQ - Decompression input request signal state. Reports the current state for the DIREQN pin. Notice that this bit is active high while the pin is active low. Therefore, the value of this bit is always the inverse of the value of the signal. After reset this bit contains a zero.

DOET - Decompression output FIFO empty threshold. This bit is active when the DO FIFO is at or below the programmed FIFO empty threshold. After reset and the *Output FIFO Threshold* register has been written, this bit contains a one.

DOREQ - Decompression output request signal state. Reports the current state for the DOREQN pin. Notice that this bit is active high while the pin is active low. Therefore, the value of this bit is always the inverse of the value of the signal. After reset this bit contains a zero.

DEOR - Decompression output end of record. This bit is active when the output FIFO contains the End-of-Record code. After reset this bit contains a zero.

res - Bits must always be written with zeros.

DIEMP - Decompression input empty. This bit is active when the DI FIFO is empty. After reset this bit contains a one.

DOEMP - Decompression output empty. This bit is active when the DO FIFO is empty. After reset this bit contains a one.

4.7 PORT CONTROL, ADDRESS 0x06 - READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x06	res				DORST	DIRST	CORST	CIRST

This register is initialized to 0x0F after reset.

CIRST - Compression input reset. Setting this bit to a one resets the CI FIFO and clears state machines on the compression input port. The reset condition remains active until the microprocessor writes a zero to this bit.

CORST - Compression output reset. Setting this bit to a one resets the CO FIFO and clears state machines on the compression output port. The reset condition remains active until the microprocessor writes a zero to this bit.

DIRST - Decompression input reset. Setting this bit to a one resets the DI FIFO and clears the state machines in the decompression input port. The reset condition remains active until the microprocessor writes a zero to this bit.

DORST - Decompression output reset. Setting this bit to a one resets the DO FIFO and clears the state machines in the decompression output port. The reset condition remains active until the microprocessor writes a zero to this bit.

res - Bits must always be written with zeros.

4.8 INTERRUPT STATUS/CONTROL 1, ADDRESS 0x07 - READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x07	DOUF	COUF	DIOF	CIOF	res	DERR	DEOR	CEOR

This register is initialized to 0x00 after reset.

CEOR- Compression End-of-Record interrupt. This bit is set when an End-of-Record codeword is strobed out of the compression output port. The microprocessor must write a one to this bit to clear this interrupt.

DEOR - Decompression End-of-Record interrupt. This bit is set when the last byte of a record is strobed out of the decompression DMA or video output port. The microprocessor must write a one to this bit to clear this interrupt.

DERR - Decompression Error. This bit is set if an EOR leaves the decompressor before DRLEN has counted down to zero or if DRLEN counts to zero and the last byte is not an EOR. DERR is only active in decompression mode (DPASS=0). The microprocessor must write a one to this bit to clear this interrupt.

res - Bits must always be written with zeros.

CIOF - Compression Input FIFO Overflow. This interrupt is generated when a write to an already full CI FIFO is performed. Data written in this condition is lost. The only means of recovery from this error is to reset the FIFO with the CIRST bit. Resetting the FIFO causes this interrupt to clear. CIREQN is inactive while the interrupt is set.

DIOF - Decompression Input FIFO Overflow. This interrupt is generated when a write to an already full DI FIFO is performed. Data written in this condition is lost. The only means of recovery from this error is to reset the FIFO with the DIRST bit. Resetting the FIFO causes this interrupt to clear. DIREQN is inactive while the interrupt is set.

COUF - Compression Output FIFO underflow. This interrupt is generated when a read from an empty CO FIFO is performed. Once this interrupt is set, the CO FIFO must be reset with the CORST bit. The microprocessor must write a one to this bit to clear this interrupt. COREQN is inactive while the interrupt is set.

DOUF - Decompression Output FIFO underflow. This interrupt is generated when a read from an empty DO FIFO is performed. Once this interrupt is set, the DO FIFO must be reset with the DORST bit. The microprocessor must write a one to this bit to clear this interrupt. DOREQN is inactive while the interrupt is set.

4.9 INTERRUPT MASK 1, ADDRESS 0x09 - READ/WRITE

Address	*bit7*	*bit6*	*bit5*	*bit4*	*bit3*	*bit2*	*bit1*	*bit0*
0x09	DOUFM	COUFM	DIOFM	CIOFM	res	DERRM	DEORM	CEORM

This register is initialized to 0xFF after reset.

CEORM - Compression End-of-Record Interrupt Mask. When set to a one, prevents Compression End-of-Record from causing INTRN to go active.

DEORM - Decompression End-of-Record Interrupt Mask. When set to a one, prevents Decompression End-of-Record from causing INTRN to go active.

DERRM - Decompression Error Mask. When set to a one, prevents a decompression error (DERR) from causing INTRN to go active.

res - Bits must always be written with zeros.

CIOFM - Compression Input FIFO Overflow Mask. When set to a one, prevents a compression input FIFO overflow (CIOF) from causing INTRN to go active.

DIOFM - Decompression Input FIFO Overflow Mask. When set to a one, prevents a decompression input FIFO overflow (DIOF) from causing INTRN to go active.

COUFM - Compression Output FIFO Underflow Mask. When set to a one, prevents a compression output FIFO underflow (COUF) from causing INTRN to go active.

DOUFM - Decompression Output FIFO Underflow Mask. When set to a one, prevents a decompression output FIFO underflow (DOUF) from causing INTRN to go active.

4.10 VERSION, ADDRESS 0x0A - READ ONLY

Address	*bit7*	*bit6*	*bit5*	*bit4*	*bit3*	*bit2*	*bit1*	*bit0*
0x0A	VERSION[7:0]							

VERSION[7:0] - Contains version number of the die. The AHA3431 returns the version number 0x31.

4.11 DECOMPRESSION RECORD LENGTH, ADDRESS 0x0C, 0x0D, 0x0E, 0x0F - READ/WRITE

Address	*bit7*	*bit6*	*bit5*	*bit4*	*bit3*	*bit2*	*bit1*	*bit0*
0x0C	DRLEN[7:0]							
0x0D	DRLEN[15:8]							
0x0E	DRLEN[23:16]							
0x0F	DRLEN[31:24]							

These registers are initialized to 0xFF after reset.

DRLEN[31:0]-Decompression Record Length. Contains the number of bytes in a decompressed record. These registers provide different functions depending on whether the decompressor is in pass-through or decompression mode. In decompress mode, the data itself contains EOR information and DRLEN is only used for error checking. DRLEN is decremented each time a byte leaves the decompressor.

In decompression mode, a DERR interrupt is issued if an EOR is not read out of the decompressor when the counter expires or if an EOR occurs before the counter expires (i.e., when the record lengths do not match). If the DERR interrupt is masked, use of the DRLEN register is optional in decompression mode.

In pass-through mode, DRLEN determines the size of records read out of the decompressor. The counter is decremented for each byte read into the decompressor.

In either mode, the counter reloads when it reaches zero or when DRLEN[31:24] is written. Reading DRLEN returns the number of bytes left in the count. The lower three bytes of this register may be prearmed since the counter is automatically reloaded at the end of a record when the part is not programmed to pause on End-of-Record. The upper byte is not prearmable since writing to this byte triggers an immediate reload to the counter.

4.12 COMPRESSION RECORD LENGTH, ADDRESS 0x10, 0x11, 0x12, 0x13 - READ/WRITE

Address	*bit7*	*bit6*	*bit5*	*bit4*	*bit3*	*bit2*	*bit1*	*bit0*
0x10	RLEN[7:0]							
0x11	RLEN[15:8]							
0x12	RLEN[23:16]							
0x13	RLEN[31:24]							

These registers are undefined after reset.

RLEN[31:0]-Record Length. Length of an uncompressed record in bytes. Writing these addresses sets a register containing the length of a record. Reading these addresses returns a counter indicating the number of bytes remaining in the current record. The counter is decremented each time a byte leaves the CI FIFO. The counter automatically reloads from the register at the end of a record. The counter is also reloaded when RLEN[31:24] is written. The record length register is also valid during pass-through operation. The lower three bytes of this register may be prearmed since the counter is automatically reloaded at the end of a record when the part is not programmed to pause on End-of-Record. The upper byte is not prearmable since writing to this byte triggers an immediate reload to the counter.

The minimum value for RLEN is 4.

4.13 COMPRESSION CONTROL, ADDRESS 0x14 - READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x14	CPREARM	res	CPOT	CPASS	CDR	CEMP	COMP	CPOR

This register is initialized to 0x04 after reset.

CPOR - Compression Pause on record boundaries. When this bit is set to one, the compressor stops taking data from the input FIFO once a record boundary is found. A record boundary is indicated by the RLEN register decrementing to zero. Upon finding the record boundary, COMP is cleared. This bit may only be changed when COMP is set to zero. After system reset, this bit is cleared.

COMP - Compression. Setting this bit to a one enables the data compression engine (or pass-through mode if CPASS is set) to take data from the compression input FIFO. If this bit is cleared, compression stops. The bit is automatically cleared at the end of a record if CPOR is set or at the end of a transfer if CPOT is set. The compression can be restarted without loss of data by setting COMP. After reset, this bit is cleared.

CEMP - Compression engine empty. This bit is set to a one when no data is present inside the compressor. Writing to this bit has no effect. After system reset, this bit is set.

CDR - Compression Dictionary Reset. Setting this bit immediately resets the compressor including the compression dictionary. The reset condition remains active until the microprocessor writes a zero to this bit.

CPASS - Compression pass-through mode. While this bit is set, data is passed directly through the compression engine without any effect on either the dictionary or the data itself. This bit may only be changed when compression is disabled (COMP=0) and the compression engine is empty of data (CEMP=0). The pass-through operation is started by setting COMP. To stop the pass-through operation, COMP should be cleared (to pause operation) and then CPASS may be cleared.

CPOT - Compression Pause on Transfer boundaries. When this bit is set the compressor stops taking data from the input FIFO once the end of transfer is reached indicated by the Record Counter decrementing to zero. Upon finding the End of Transfer boundary the COMP bit is cleared. CPOT can only be set when COMP is cleared.

res - Bits must always be written with zeros.

CPREARM -Prearm Enable. When this bit is set, Compression Control Prearm register is loaded into the Compression Control register when the next end of record leaves the compressor.

4.14 COMPRESSION RESERVED, ADDRESS 0x15 - READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x15	res							

This register is used for production testing. Must be written with zero if at all. Resets to zero.

res - Bits must always be written with zeros.

4.15 COMPRESSION LINE LENGTH, ADDRESS 0x16, 0x17 - READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x16	LINE[7:0]							
0x17	res					LINE[10:8]		

This register contains information necessary for the compression operation. It must be set prior to any compression operation. It should only be changed when COMP is cleared and CEMP is set. After changing compression line length, the compressor should be reset using CDR. These registers are undefined after reset.

res - Bits must always be written with zeros.

LINE[10:0]-Line length. The number of bytes in the scan line is programmed here. Minimum value is 16.

4.16 DECOMPRESSION CONTROL, ADDRESS 0x18 - READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x18	DPREARM	DBLANK	DPOT	DPASS	DDR	DEMP	DCOMP	DPOR

This register is initialized to 0x04 after reset. This register can be prearmed.

DPOR - Decompression Pause on record boundaries. When this bit is set to one, the decompressor stops taking data from the input FIFO once a record boundary is found. Upon finding the record boundary, DCOMP is cleared. This bit may only be changed when DCOMP is set to zero. After system reset or DDR, this bit is cleared.

DCOMP - Decompression. Setting this bit to a one enables the decompression engine (or pass-through mode if DPASS is set) to take data from the decompression input FIFO. If this bit is cleared, decompression stops. The bit is automatically cleared at the end of a record if DPOR is set. Decompression can be restarted without loss of data by setting DCOMP. After system reset or DDR, this bit is cleared.

DEMP - Decompression engine empty. This bit is set when the decompression engine is cleared of data. Writing to this bit has no effect. After system reset, this bit is set.

DDR - Decompression Dictionary Reset. Setting this bit immediately resets the decompressor including the decompression dictionary. The reset condition remains active until the microprocessor writes a zero to this bit.

DPASS - Decompression pass-through mode. While this bit is set, data is passed directly through the decompression engine without any effect on the data. This bit may only be changed when decompression is disabled (DCOMP=0) and the decompression engine is empty of data (DEMP=1). The pass-through operation is started by setting DCOMP. To stop the pass-through operation, DCOMP should be cleared (to pause operation) and then DPASS may be cleared.

DPOT - Decompression Pause on Transfer Boundaries. When this bit is set the decompressor stops taking data from the input FIFO once a decompression end of transfer boundary is found indicated by the Decompression Record Counter decrementing to zero.

DBLANK - Decompression Blank record. The data in the next record output from the decompressor is a repeating byte pattern using the 8-bit data defined in the PATTERN register. DBLANK automatically clears at the end of the record when the Decompression Record Count decrements to zero. When using DBLANK to generate a blank record the device must not contain data to be decompressed and the system must not send data to be decompressed for any future records until the part has reached the End-of-Record for the blank record.

DPREARM -Prearm Enable. When this bit is set, Decompression Control Prearm register is loaded into the Decompression Control register when the next end of record leaves the decompressor.

4.17 DECOMPRESSION RESERVED, ADDRESS 0x1A - READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x1A	res							

This register is used for production testing only. Must be written with zero if at all. Initialized to 0x00 after reset.

4.18 DECOMPRESSION LINE LENGTH, ADDRESS 0x1C, 0x1D - READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x1C	LINE[7:0]							
0x1D	res						LINE[10:8]	

This register contains information necessary for the decompression operation. It must be set prior to any decompression operation. It should only be changed between records when DCOMP is cleared and DEMP is set. These registers are undefined after reset.

res - Bits must always be written with zeros.

LINE[10:0]-Line length. The number of bytes in the scan line is programmed here. Minimum value is 16. For scan line lengths larger than the maximum allowed, set to 16.

4.19 COMPRESSION RECORD COUNT, ADDRESS 0x20, 0x21 - READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x20	RC[7:0]							
0x21	RC[15:8]							

These registers are initialized to 0xFFFF after reset.

RC[15:0] - Record Count is the number of records in the current transfer. This counter is decremented as the last byte of a record is compressed.

4.20 INTERRUPT STATUS/CONTROL 2, ADDRESS 0x27 - READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x27	res						DEOT	CEOT

This register is initialized to 0x00 after reset.

CEOT - Compression End-of-Transfer Interrupt. This bit is set when an end of transfer condition is reached indicated by the compression Record Counter counting down to zero. The microprocessor must write a one to this bit to clear this interrupt.

DEOT - Decompression End-of-Transfer Interrupt. This bit is set when a decompression end of transfer condition is reached indicated by the Decompression Record Counter counting down to zero. The microprocessor must write a one to this bit to clear this interrupt.

res - Bits must always be written with zeros.

4.21 INTERRUPT MASK 2, ADDRESS 0x29 - READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x29	res						DEOTM	CEOTM

This register is initialized to 0xFF after reset.

CEOTM - Compression End-of-Transfer Interrupt Mask. When set to a one, prevents Compression End-of-Transfer from causing INTRN to go active.

DEOTM - Decompression End-of-Transfer Interrupt Mask. When set to a one, prevents Decompression End-of-Transfer from causing INTRN to go active.

res - Bits must always be written with zeros.

4.22 DECOMPRESSION RECORD COUNT, ADDRESS 0x2C, 0x2D - READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x2C	DRC[7:0]							
0x2D	DRC[15:8]							

These registers are initialized to 0xFFFF after reset.

DRC[15:0] -Decompression Record Count is the number of records in the current transfer. Expiration of this counter causes a CEOT interrupt to be posted.

4.23 COMPRESSION BYTE COUNT, ADDRESS 0x30, 0x31, 0x32, 0x33 - READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x30	BCNT[7:0]							
0x31	BCNT[15:8]							
0x32	BCNT[23:16]							
0x33	BCNT[31:24]							

BCNT[31:0]-Compressed Byte Count is the number of bytes output from the CO FIFO, rounded up to a word boundary defined by WIDE, for the current record. Systems may use this data to remove pad words from the compressed data stream. The count gets reset at the beginning of each record and when CORST is active.

4.24 COMPRESSION CONTROL PREARM, ADDRESS 0x34 - READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x34	NCPREARM	*res*	NCPOT	NCPASS	NCDR	*res*	NCOMP	NCPOR

This register is initialized to 0x00 after reset.

res - Bits must always be written with zeros.

See Compression Control register for bit descriptions. This register is the prearm register for the Compression Control register.

4.25 PATTERN, ADDRESS 0x35 - READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x35	PATTERN[7:0]							

This register is undefined after reset.

PATTERN[7:0]-Pattern is the 8-bit data used to generate blank bands or records. If DBLANK is set, the part outputs this register value repeatedly for the entire record (or band).

4.26 DECOMPRESSION CONTROL PREARM, ADDRESS 0x38 - READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x38	NDPREARM	NDBLANK	NDPOT	NDPASS	NDDR	res	NDCOMP	NDPOR

This register initializes to 0x00 after reset.

res - Bits must always be written with zeros.

4.27 DECOMPRESSION RESERVED, ADDRESS 0x3A - READ/WRITE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x3A	res							

This register is used for production testing only. Must be written with zero if at all. Initialized to 0x00 after reset.

See Decompression Control register for bit descriptions. This register is the prearm register for the Decompression Control register.

5.0 SIGNAL DESCRIPTIONS

This section contains descriptions for all the pins. Each signal has a type code associated with it. The type codes are described in the following table.

TYPE CODE	DESCRIPTION
I	Input only pin
O	Output only pin
I/O	Input/Output pin
S	Synchronous signal
A	Asynchronous signal

5.1 MICROPROCESSOR INTERFACE

MICROPROCESSOR INTERFACE		
SIGNAL	***TYPE***	***DESCRIPTION***
PD[7:0]	I/O S	Processor Data. Data for all microprocessor reads and writes of registers within AHA3431 are performed on this bus. This bus may be tied to the Data bus, D[31:0], provided microprocessor accesses do not occur at the same time as DMA accesses.
PA[5:0]	I S	Processor Address Bus. Used to address internal registers within AHA3431.
CSN	I S	Chip Select. Selects AHA3431 as the source or destination of the current microprocessor bus cycle. CSN needs only be active for one clock cycle to start a microprocessor access.
DIR	I S	Direction. This signal indicates whether the access to the register specified by the PA bus is a read or a write. The polarity of this signal is programmed with the PROCMODE0 pin.
RDYN	O A,S	Ready. Indicates valid data is on the data bus during read operation and completion of write operation. Its operation depends on PROCMODE[1:0] settings.
INTRN	O S	Interrupt. The compression and decompression processes generate interrupts that are reported with this signal. INTRN is low whenever any non-masked bits are set in the *Interrupt Status/Control* register.
PROCMODE[1:0]	I S	Microprocessor Port Configuration Mode. Selects the polarity of the DIR pin and operation of the CSN pin. Refer to Section 2.1 *Microprocessor Interface* for details. (Figure 2 through Figure 5)

5.2 DATA INTERFACE

DATA INTERFACE		
SIGNAL	***TYPE***	***DESCRIPTION***
D[31:0]	I/O S	Data for all channels is transmitted on this bus. The ACKN is used to distinguish between the four channels. Data being written to AHA3431 is latched on the rising edge of CLOCK when the strobe condition is met. Data setup and hold times are relative to CLOCK. If the bus is configured to 16-bit transfers (WIDE=0), data is carried on D[15:0]. In this case, D[31:16] should be terminated with pullup resistors.
DRIVEN	I A	Drive Enable. Active low output driver enable. This input must be low in order to drive data onto D[31:0] in accordance with the current strobe condition.
SD	I S	Strobe Delay. Active high. Allows insertion of wait states for DMA access to the FIFOs. The strobe condition, as programmed in the DSC field of *System Configuration 1*, enables this signal and selects its polarity.
CIREQN	O S	Compression Input Data Request, active low. This signal, when active, indicates the ability of the CI FIFO to accept data.
CIACKN	I S	Compression Input Data Acknowledge. Active low. This signal, when active, indicates the data on D is for the compression input FIFO. Data on D is latched on the rising edge of CLOCK when the strobe condition is met.
COREQN	O A,S	Compression Output Data Request, active low. When this signal is active, it indicates the ability of the CO FIFO to transmit data.
COACKN	I S	Compression Output Data Acknowledge. Active low. The definition of COACKN varies with the data strobe condition in *System Configuration 1*. See Table 4.
COEORN	O S	Compression Output End-of-Record, active low. COEORN is active when the word currently on the output of the CO FIFO contains an End-of-Record.
COEOTN	O S	Compression Output End-of-Transfer, active low. COEOTN is active when the word currently on the output of the CO FIFO contains the End-of-Transfer.
DIREQN	O S	Decompression Input Data Request, active low. When this signal is active, it indicates the ability of the DI port to accept data.
DIACKN	I S	Decompression Input Data Acknowledge. Active low decompression data input. When this signal is active, it indicates the data on D is for the decompression input port. Data on D is latched on the rising edge of CLOCK when the strobe condition is met.
DOREQN	O A, S	Decompression Output Data Request, active low. When this signal is active, it indicates the ability of the DO port to transmit data.
DOACKN	I S	Decompression Output Data Acknowledge. The definition of DOACKN varies with the data strobe condition in *System Configuration 1*. See Table 4.

5.3 VIDEO INTERFACE

VIDEO INTERFACE		
SIGNAL	***TYPE***	***DESCRIPTION***
VIREQN	O S	Video Input Request. Active low output indicating that the VDI port is ready to accept another byte on VID[7:0].
VIACKN	I S	Video Input Acknowledge. Active low input indicating that VID[7:0] is being driven with a valid byte.
VID[7:0]	I S	Video Input Data. The value on this input bus is written into AHA3431 when both VIREQN and VIACKN are active.
VOREQN	O S	Video Output Request. Active low output indicating that the byte on VOD[7:0] is valid.
VOACKN	I S	Video Output Acknowledge. Active low input indicating that the external system is ready to read VOD[7:0].
VOD[7:0]	O S	Video Output Data. The value on this output bus is read when both VOREQN and VOACKN are low.
VOEORN	O S	Video Output End of Record is active low indicating the byte on VOD[7:0] contains the last byte in a record.
VOEOTN	O S	Video Output End of Transfer is active low indicating the byte on VOD[7:0] contains the last byte in a multi-record transfer.

5.4 SYSTEM CONTROL

SYSTEM CONTROL		
SIGNAL	***TYPE***	***DESCRIPTION***
CLOCK	I	System Clock. This signal is connected to the clock of the microprocessor. The Intel i960Cx calls this pin PCLK.
RSTN	I A	Power on Reset. Active low reset signal. AHA3431 must be reset before any DMA or microprocessor activity is attempted. RSTN should be a minimum of 10 CLOCK periods.
TEST0	I A	Board Test mode. When TEST is high, all outputs are tristated. When TEST is low, the chip performs normally.
TEST1	I A	Used for production tests. This input should always be tied low.

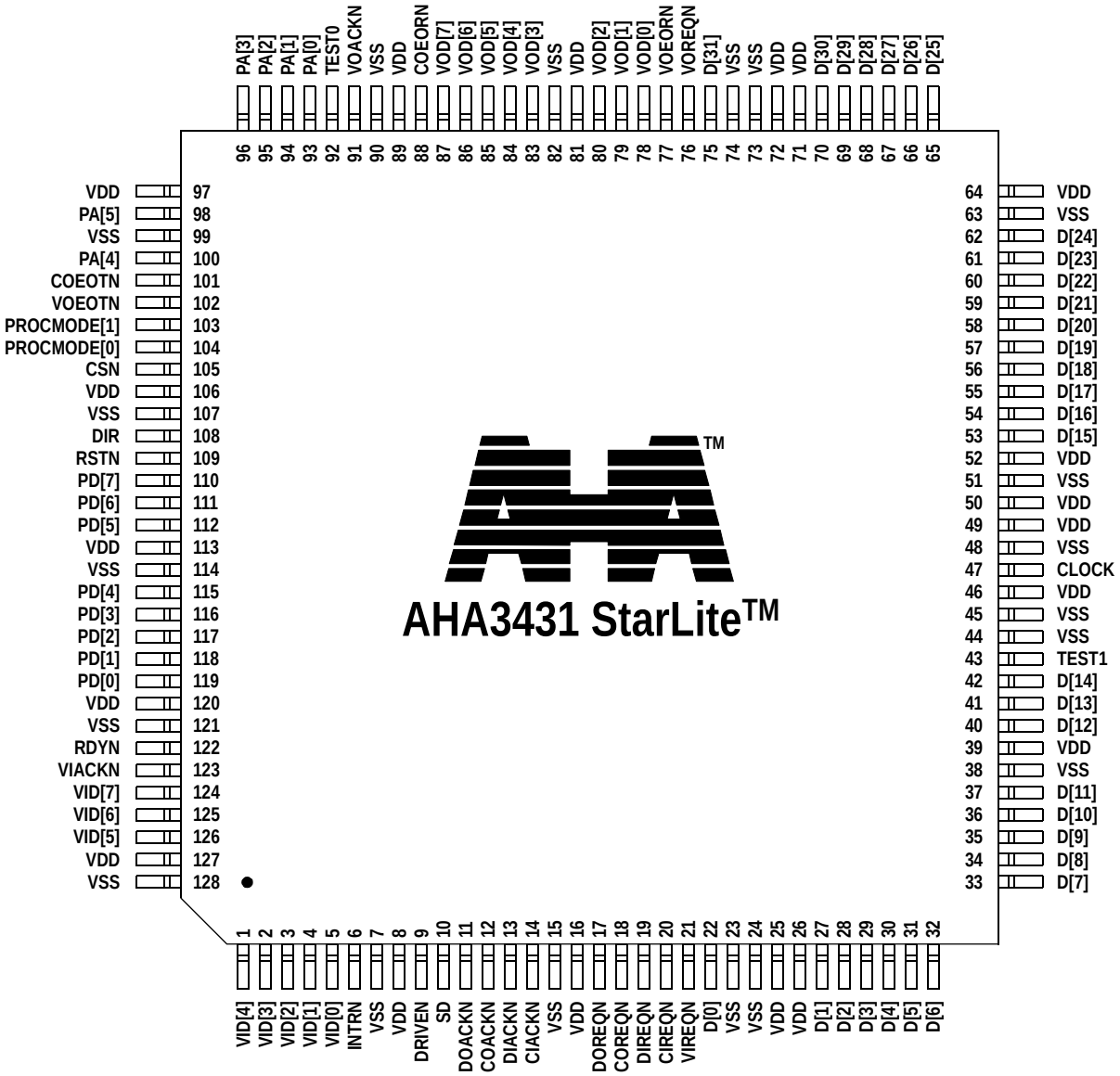
6.0 PINOUT

PIN	SIGNAL
1	VID[4]
2	VID[3]
3	VID[2]
4	VID[1]
5	VID[0]
6	INTRN
7	VSS
8	VDD
9	DRIVEN
10	SD
11	DOACKN
12	COACKN
13	DIACKN
14	CIACKN
15	VSS
16	VDD
17	DOREQN
18	COREQN
19	DIREQN
20	CIREQN
21	VIREQN
22	D[0]
23	VSS
24	VSS
25	VDD
26	VDD
27	D[1]
28	D[2]
29	D[3]
30	D[4]
31	D[5]
32	D[6]
33	D[7]
34	D[8]
35	D[9]
36	D[10]
37	D[11]
38	VSS
39	VDD
40	D[12]
41	D[13]
42	D[14]
43	TEST1

PIN	SIGNAL
44	VSS
45	VSS
46	VDD
47	CLOCK
48	VSS
49	VDD
50	VDD
51	VSS
52	VDD
53	D[15]
54	D[16]
55	D[17]
56	D[18]
57	D[19]
58	D[20]
59	D[21]
60	D[22]
61	D[23]
62	D[24]
63	VSS
64	VDD
65	D[25]
66	D[26]
67	D[27]
68	D[28]
69	D[29]
70	D[30]
71	VDD
72	VDD
73	VSS
74	VSS
75	D[31]
76	VOREQN
77	VOEORN
78	VOD[0]
79	VOD[1]
80	VOD[2]
81	VDD
82	VSS
83	VOD[3]
84	VOD[4]
85	VOD[5]
86	VOD[6]

PIN	SIGNAL
87	VOD[7]
88	COEORN
89	VDD
90	VSS
91	VOACKN
92	TEST0
93	PA[0]
94	PA[1]
95	PA[2]
96	PA[3]
97	VDD
98	PA[5]
99	VSS
100	PA[4]
101	COEOTN
102	VOEOTN
103	PROCMODE[1]
104	PROCMODE[0]
105	CSN
106	VDD
107	VSS
108	DIR
109	RSTN
110	PD[7]
111	PD[6]
112	PD[5]
113	VDD
114	VSS
115	PD[4]
116	PD[3]
117	PD[2]
118	PD[1]
119	PD[0]
120	VDD
121	VSS
122	RDYN
123	VIACKN
124	VID[7]
125	VID[6]
126	VID[5]
127	VDD
128	VSS

Figure 16: Pinout



7.0 DC ELECTRICAL SPECIFICATIONS

7.1 OPERATING CONDITIONS

OPERATING CONDITIONS					
SYMBOL	**PARAMETER**	**MIN**	**MAX**	**UNITS**	**NOTES**
Vdd	Supply voltage	3.0	3.6	V	
Idd	Supply current (active)		160	mA	4
Idd	Supply current (typical)		120	mA	1, 4
Idd	Supply current (static)		1	mA	2, 4
Ta	Ambient temperature	0	70	°C	
Vil	Input low voltage	Vss-0.3	0.8	V	
Vih	Input high voltage	2.0	Vdd+0.3	V	
Iil	Input leakage current	-10	10	µA	
Vol	Output low voltage (Iol=-4mA)		0.4	V	
Voh	Output high voltage (Ioh=4mA)	2.4		V	
Iol	Output low current		4	mA	
Ioh	Output high current		-4	mA	
Ioz	Output leakage current during tristate	-10	10	µA	
Cin	Input capacitance		10	pF	
Cout	Output capacitance		7	pF	
Cio	Input/Output capacitance		10	pF	
Comax	Maximum capacitance load for all signals (including self loading)		50	pF	3

Notes:

1) Dynamic current; typical operating conditions (3.3V)
2) Static current (clock high)
3) Timings referenced to this load
4) ILOAD=0 mA

7.2 ABSOLUTE MAXIMUM STRESS RATINGS

ABSOLUTE MAXIMUM STRESS RATINGS					
SYMBOL	**PARAMETER**	**MIN**	**MAX**	**UNITS**	**NOTES**
Tstg	Storage temperature	-50	150	°C	
Vdd	Supply voltage	-0.5	4.5	V	
Vin	Input voltage	Vss-0.5	Vdd+0.5	V	

8.0 AC ELECTRICAL SPECIFICATIONS

Notes:

1) Production test condition is 50 pF.
2) All timings are referenced to 1.4 volts.

Figure 17: Data Interface Timing

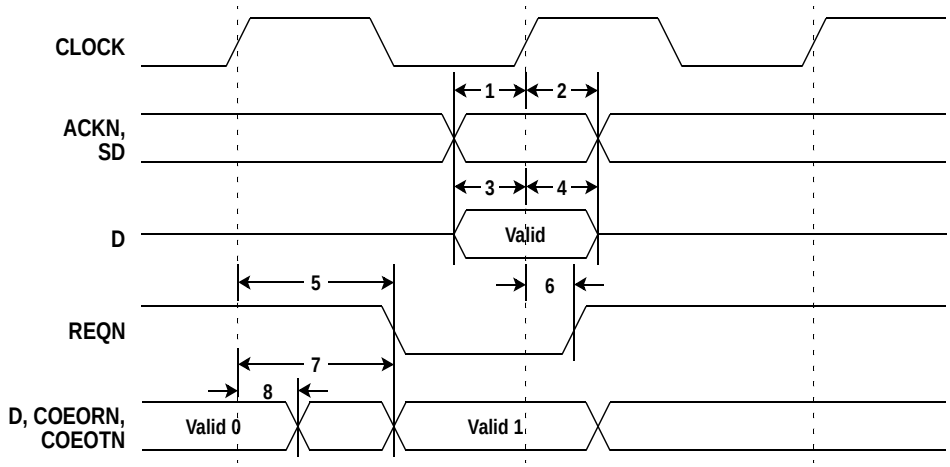


Table 6: Data Port Timing Requirements

NUMBER	PARAMETER	MIN	MAX	UNITS
1	CIACKN, DIACKN, COACKN, DOACKN and SD setup time	7		ns
2	CIACKN, DIACKN, COACKN, DOACKN and SD hold time	2		ns
3	D-bus input setup time	7		ns
4	D-bus input hold time	2		ns
5	REQN delay (non-EOR case)		12	ns
6	REQN hold (non-EOR case)	2		ns
7	D-bus, COEORN, COEOTN output delay		12	ns
8	D-bus, COEORN, COEOTN output hold	2		ns

Figure 18: Request Deasserts at EOR, Strobe Condition of DSC=0-3, 6-7; ERC=0

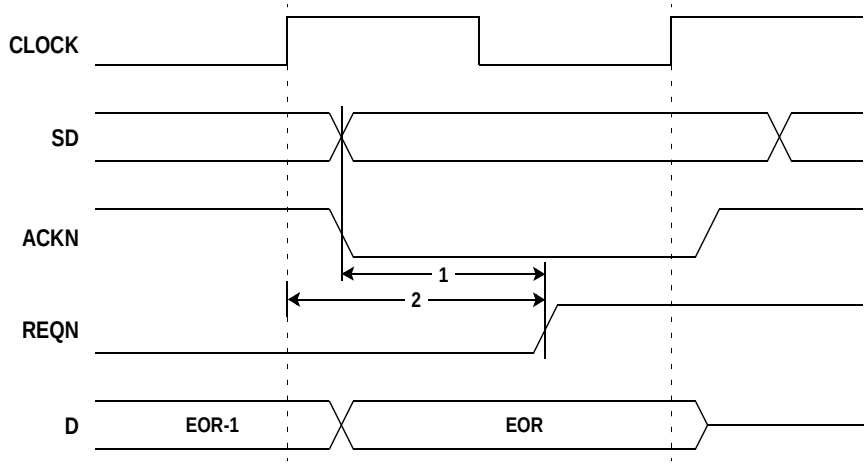


Figure 19: Request Deasserts at EOR, Strobe Condition of DSC=0-3, 6-7; ERC=1

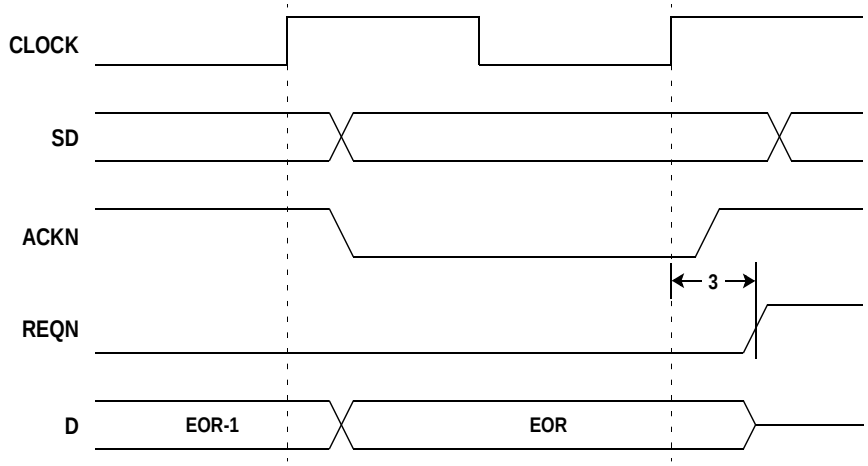


Figure 20: Request Deasserts at EOR, Strobe Condition of DSC=4 or 5; ERC=0

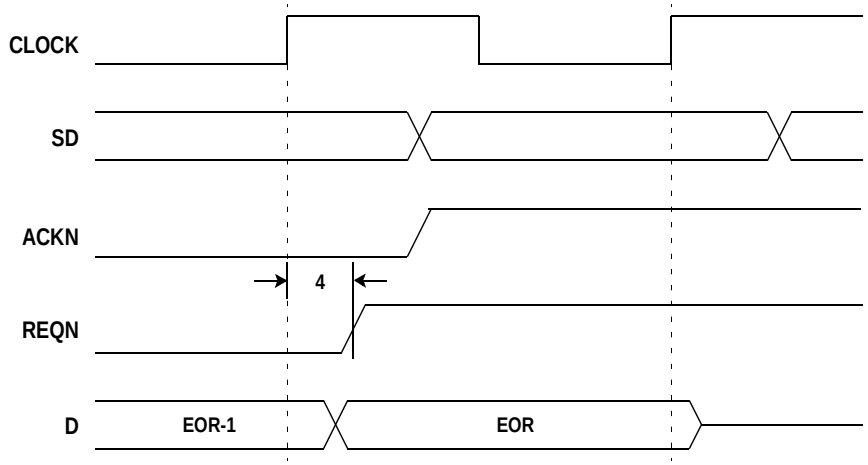


Figure 21: Request Deasserts at EOR, Strobe Condition of DSC=4 or 5; ERC=1

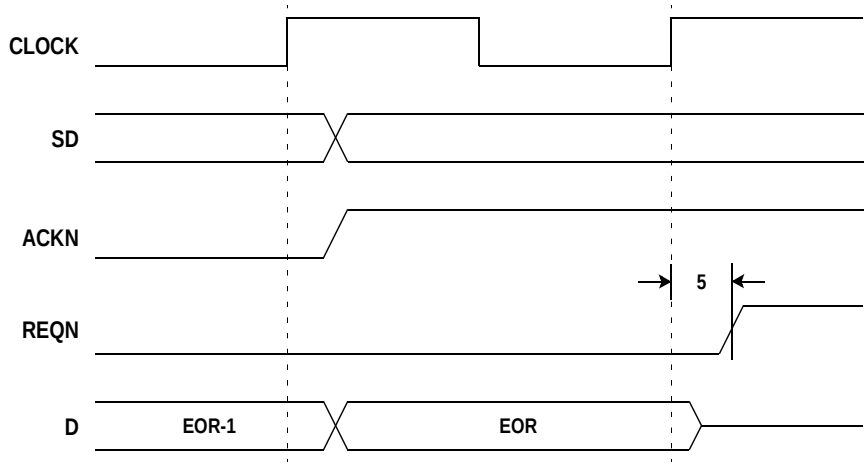


Table 7: Request vs. EOR Timing

NUMBER	PARAMETER	MIN	MAX	UNITS
1	ACKN, SD to REQN ERC=0		12	ns
2	CLOCK to REQN ERC=0		12	ns
3	CLOCK to REQN DSC=0-3, 6, 7; ERC=1		12	ns
4	CLOCK to REQN DSC=4, 5; ERC=0		12	ns
5	CLOCK to REQN DSC=4, 5; ERC=1		12	ns

Figure 22: Output Enable Timing

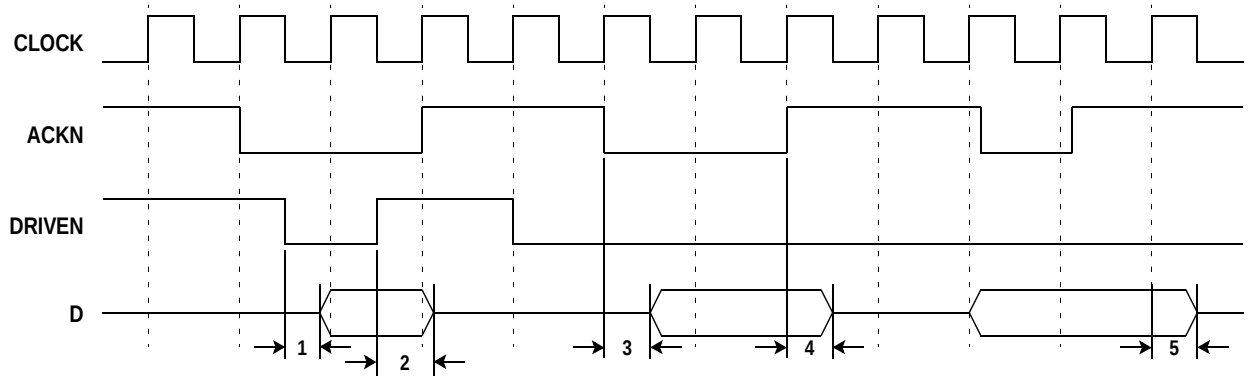


Table 8: Output Enable Timing Requirements

NUMBER	PARAMETER	MIN	MAX	UNITS
1	DRIVEN to D valid		12	ns
2	DRIVEN to D tristate		6	ns
3	ACKN to D valid		12	ns
4	ACKN to D tristate		6	ns
5	CLOCK to D tristate (DSC=100, 101)		8	ns

Figure 23: Video Input Port Timing

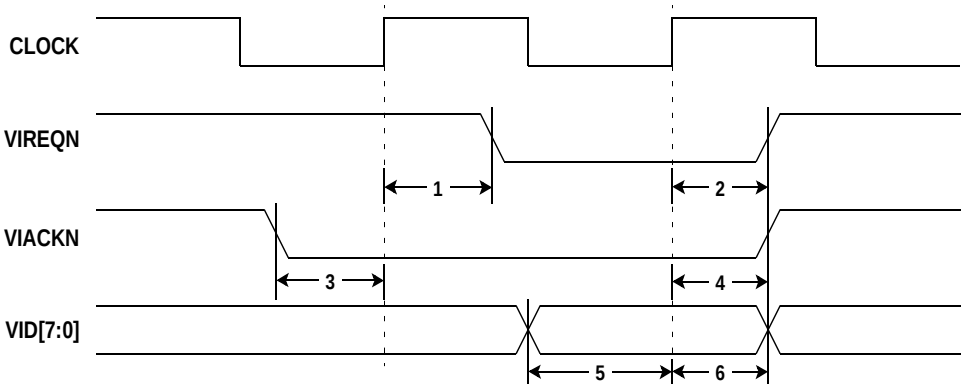


Table 9: Video Input Port Timing Requirements

NUMBER	PARAMETER	MIN	MAX	UNITS
1	VIREQN delay		12	ns
2	VIREQN hold	2		ns
3	VIACKN setup	7		ns
4	VIACKN hold	1		ns
5	VID setup	7		ns
6	VID hold	1		ns

Figure 24: Video Output Port Timing

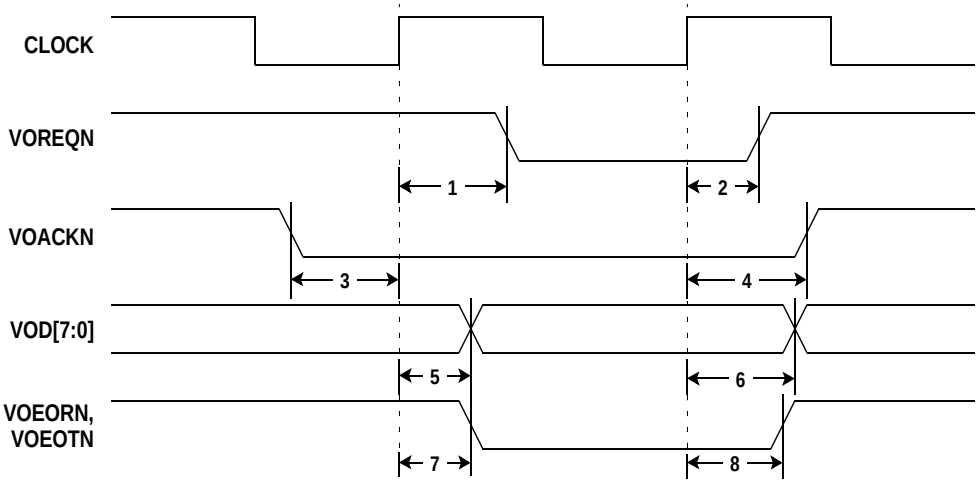


Table 10: Video Output Port Timing Requirements

NUMBER	*PARAMETER*	*MIN*	*MAX*	*UNITS*
1	VOREQN delay		12	ns
2	VOREQN hold	2		ns
3	VOACKN setup	7		ns
4	VOACKN hold	1		ns
5	VOD delay		12	ns
6	VOD hold	2		ns
7	VOEORN, VOEOTN hold	2		ns
8	VOEORN, VOEOTN delay		12	ns

Figure 25: Microprocessor Interface Timing (PROCMODE[1]=0)

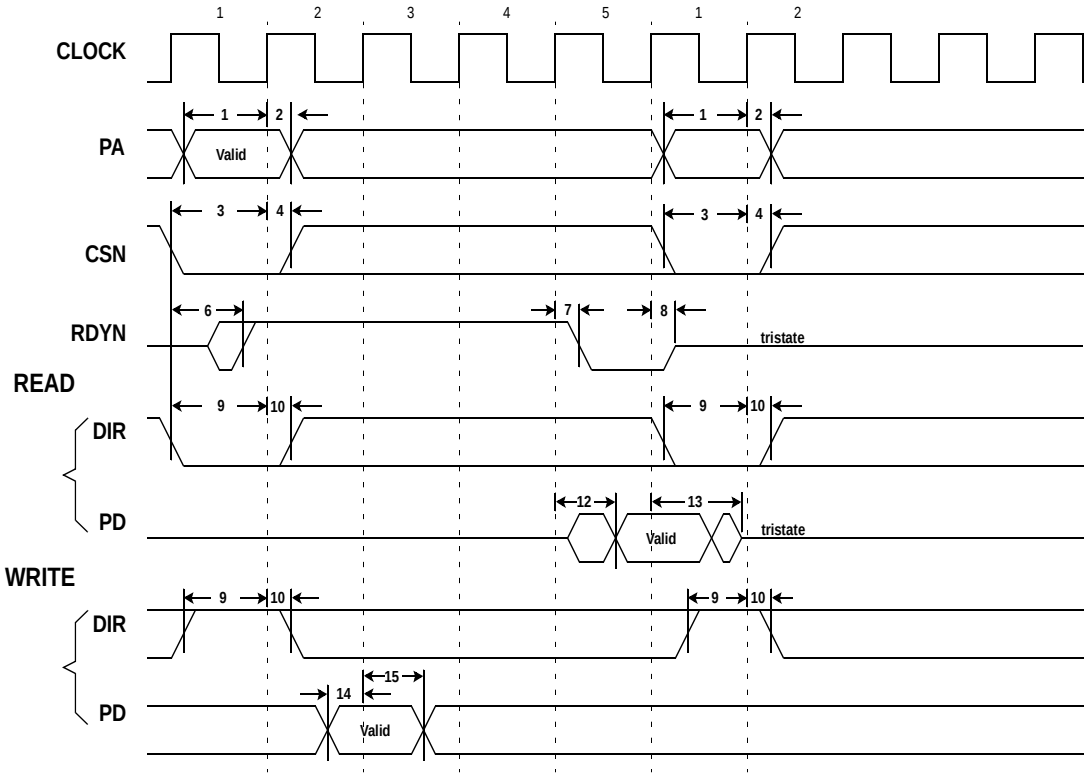


Figure 26: Microprocessor Interface Timing (PROCMODE[1]=1)

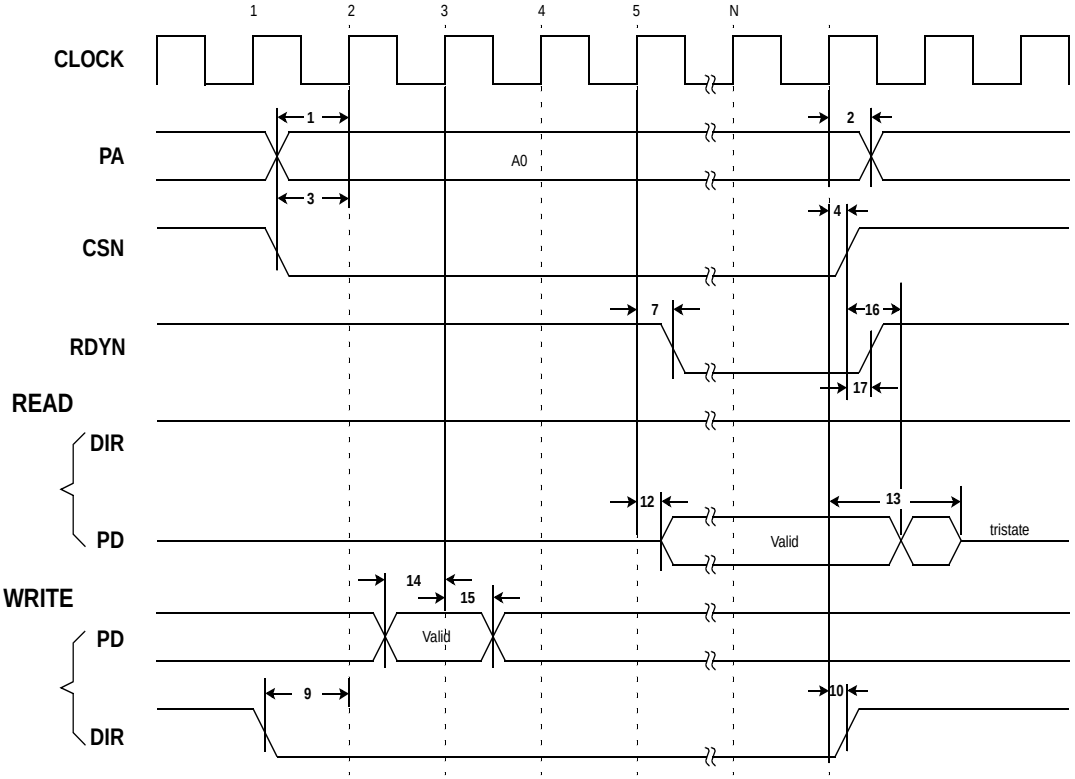


Table 11: Microprocessor Interface Timing Requirements

NUMBER	*PARAMETER*	*MIN*	*MAX*	*UNITS*
1	PA setup time	7		ns
2	PA hold time	1		ns
3	CSN setup time	7		ns
4	CSN hold time	2		ns
6	CSN to valid RDYN		12	ns
7	RDYN valid delay		12	ns
8	RDYN drive disable		8	ns
9	DIR setup time	7		ns
10	DIR hold time	2		ns
12	PD valid delay		12	ns
13	PD drive disable		8	ns
14	PD setup time	7		ns
15	PD hold time	1		ns
16	CSN high to PD tristate		8	ns
17	CSN high to RDYN high		12	ns

Figure 27: Interrupt Timing

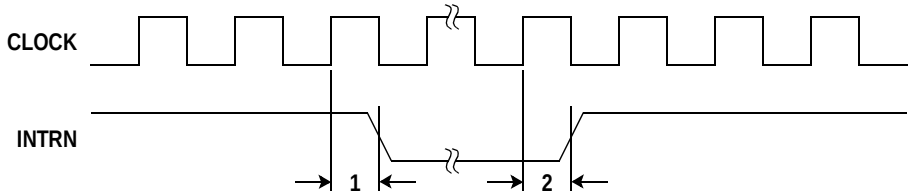


Table 12: Interrupt Timing Requirements

NUMBER	PARAMETER	MIN	MAX	UNITS
1	INTRN delay time		12	ns
2	INTRN hold time	2		ns

Figure 28: Clock Timing

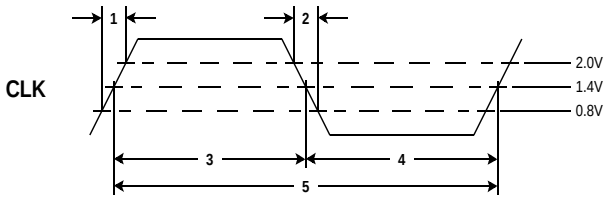


Table 13: Clock Timing Requirements

NUMBER	PARAMETER	MIN	MAX	UNITS
1	CLOCK rise time		4	ns
2	CLOCK fall time		4	ns
3	CLOCK high time	10		ns
4	CLOCK low time	10		ns
5	CLOCK period	25		ns

Figure 29: Power On Reset Timing

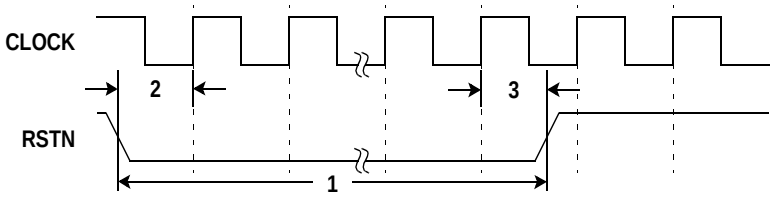


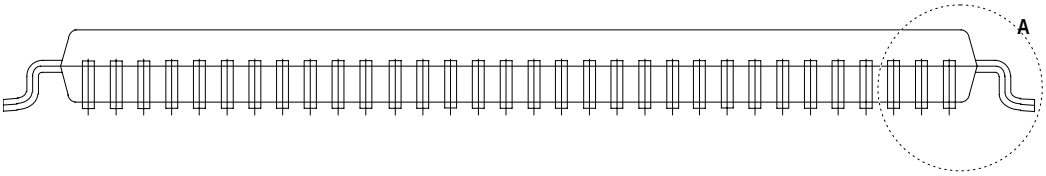
Table 14: Power On Reset Timing Requirements

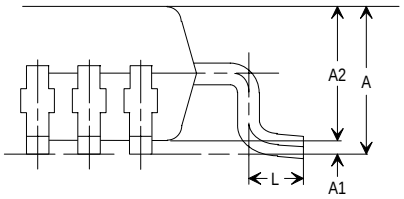
NUMBER	PARAMETER	MIN	MAX	UNITS
1	RSTN low pulsewidth	10		clocks
2	RSTN setup to CLOCK rise	10		ns
3	RSTN hold time	2		ns

Notes:

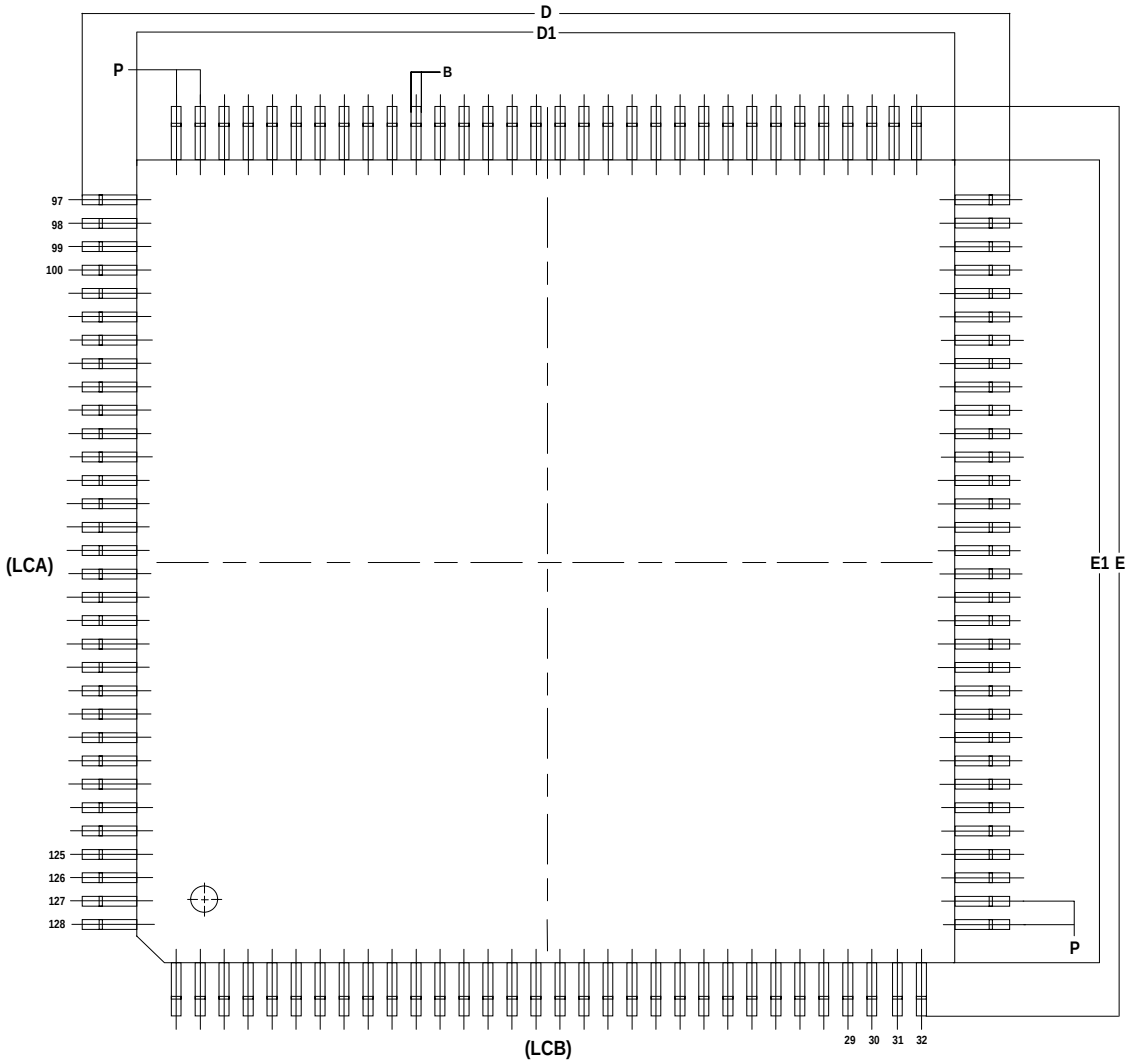
1) RSTN signal can be asynchronous to the CLOCK signal. It is internally synchronized to the rising edge of CLOCK.

9.0 PACKAGE SPECIFICATIONS





DETAIL A



JEDEC outline is MO-108

PLASTIC QUAD FLAT PACK PACKAGE DIMENSIONS

SYMBOL	***NUMBER OF PIN AND SPECIFICATION DIMENSION***		
	128		
	SB		
	MIN	NOM	MAX
(LCA)	32		
(LCB)	32		
A		3.7	4.07
A1	0.25	0.33	
A2	3.2	3.37	3.6
D	30.95	31.2	31.45
D1	27.99	28	28.12
E	30.95	31.2	31.45
E1	27.99	28	28.12
L	0.73	0.88	1.03
P		0.8	
B	0.3	0.35	0.4

10.0 ORDERING INFORMATION

10.1 AVAILABLE PARTS

PART NUMBER	***DESCRIPTION***
AHA3431A-040 PQC	40 MBytes/sec Simultaneous Lossless Data Compression/ Decompression Coprocessor IC

10.2 PART NUMBERING

AHA	***3431***	***A-***	***040***	***P***	***Q***	***C***
Manufacturer	Device Number	Revision Level	Speed Designation	Package Material	Package Type	Test Specification

Device Number:

3431

Revision Letter:

A

Package Material Codes:

P Plastic

Package Type Codes:

Q Quad Flat Pack

Test Specifications:

C Commercial 0°C to +70°C

11.0 RELATED TECHNICAL PUBLICATIONS

DOCUMENT #	*DESCRIPTION*
PS3411	AHA Product Specification – AHA3411 StarLite™ 16 MBytes/sec Simultaneous Compressor/Decompressor IC
ABDC18	AHA Application Brief – AHA3410C, AHA3411 and AHA3431 Device Differences
ANDC12	AHA Application Note – AHA3410C StarLite™ Designer's Guide
ANDC13	AHA Application Note – Compression Performance on Bitonal Images
ANDC14	AHA Application Note – StarLite™ Evaluation Software
ANDC15	AHA Application Note – ENCODEB2 Compression Algorithm Description
ANDC16	AHA Application Note – Designer's Guide for StarLite™ Family Products: AHA3411, AHA3422 and AHA3431
ANDC17	AHA Application Note – StarLite™ Compression on Continuous Tone Images
GLGEN1	General Glossary of Terms
STARSW	StarLite™ Evaluation Software (Windows™)

APPENDIX A: ADDITIONAL TIMING DIAGRAMS FOR DMA MODE TRANSFERS

Figure A1: DMA Mode Timing for Single Word Writes, Strobe Condition of DSC=000

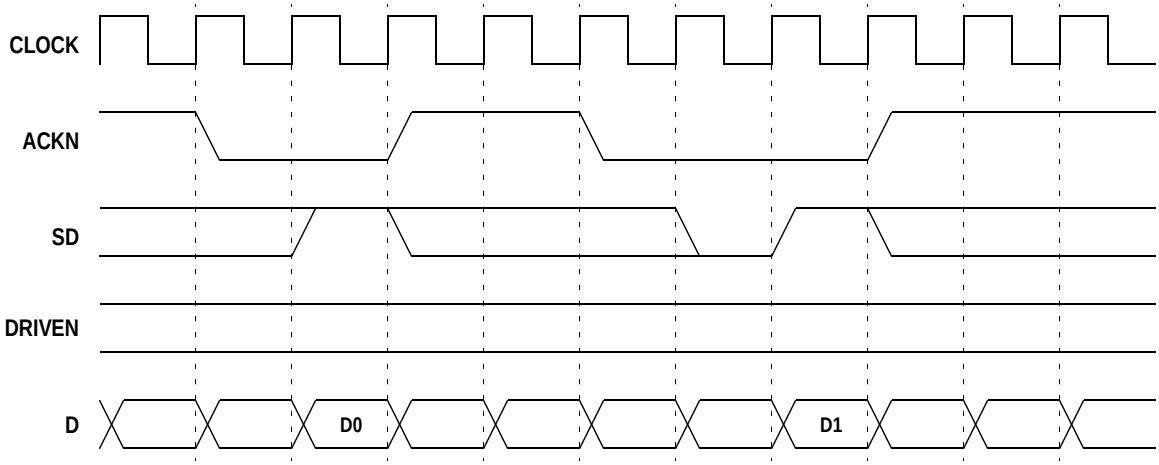


Figure A2: DMA Mode Timing for Single Word Reads, Strobe Condition of DSC=000

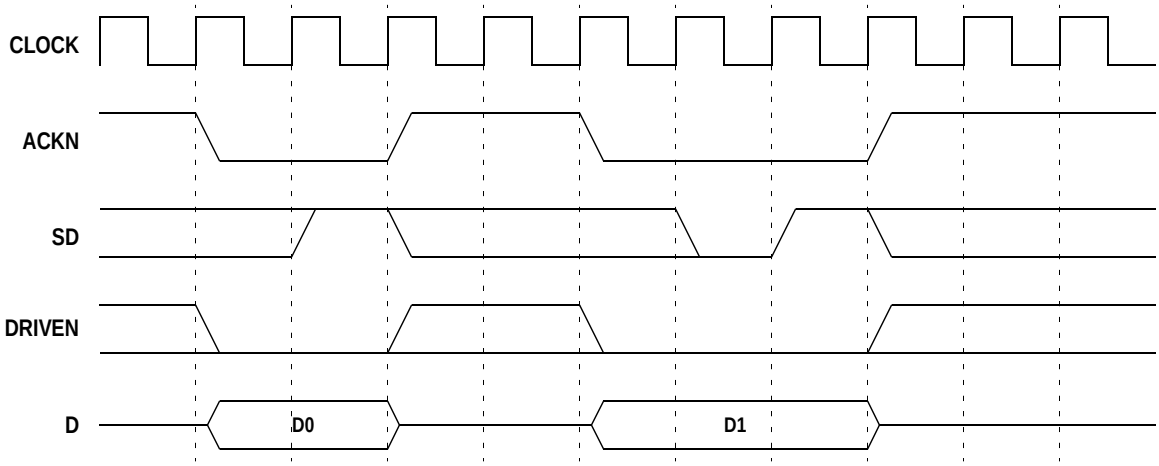


Figure A3: DMA Mode Timing for Four Word Burst Write, One Wait State, Strobe Condition of DSC=000

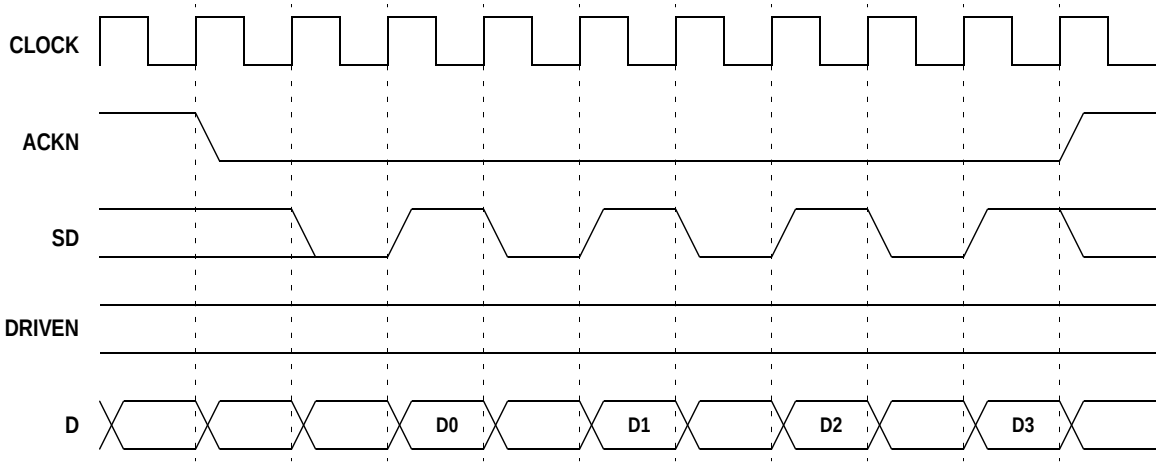


Figure A4: DMA Mode Timing for Four Word Burst Read, One Wait State, Strobe Condition of DSC=000

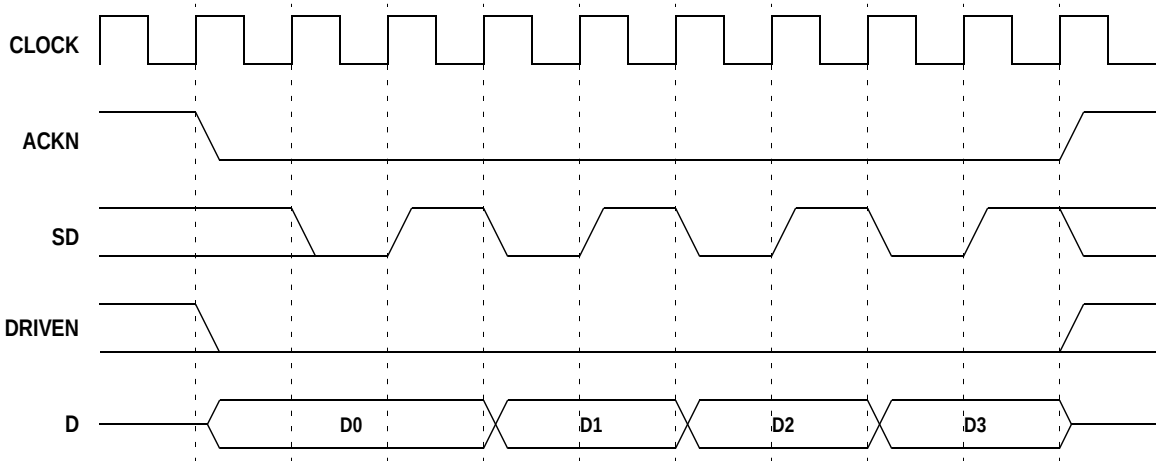


Figure A5: DMA Mode Timing for Eight Word Burst Write, Zero Wait State, Strobe Condition of DSC=000

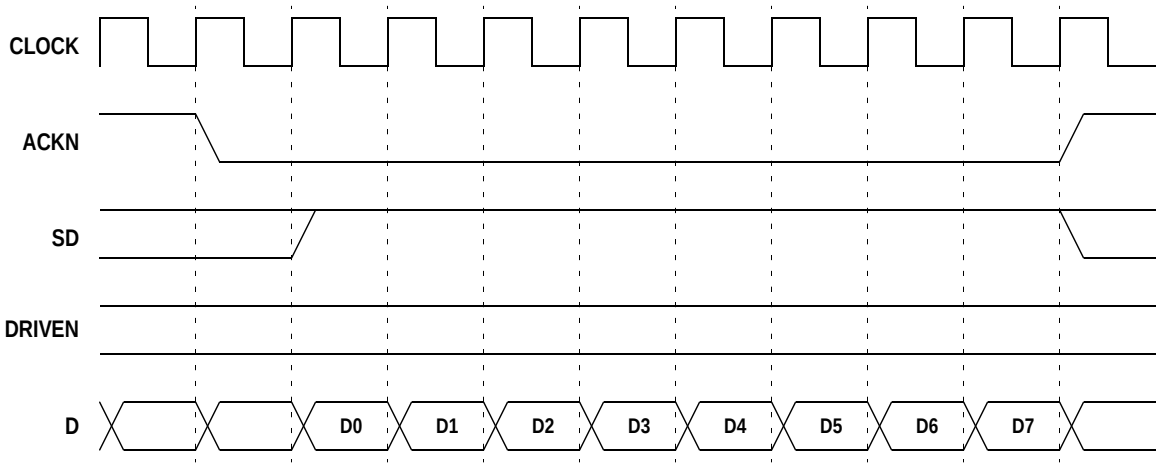


Figure A6: DMA Mode Timing for Eight Word Burst Read, Zero Wait State, Strobe Condition of DSC=000

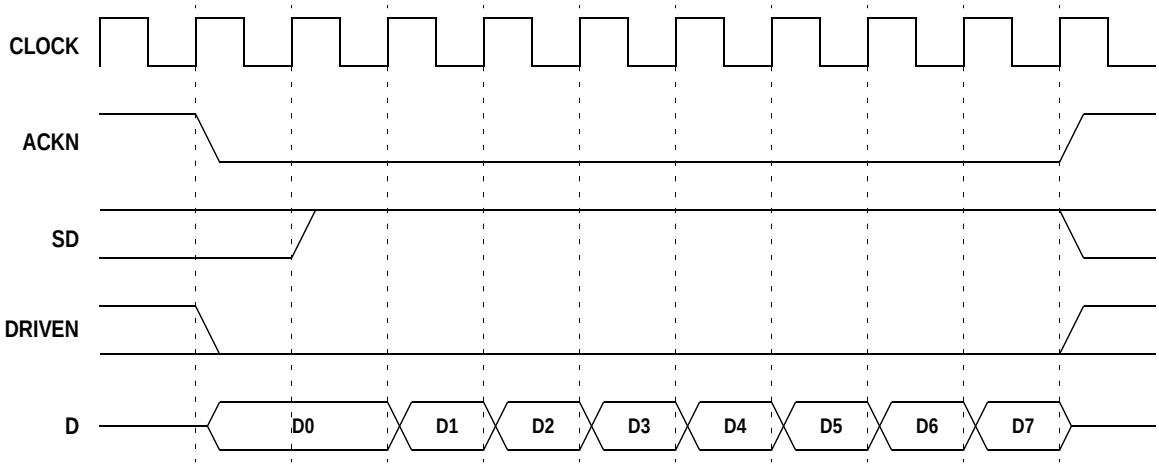


Figure A7: DMA Mode Timing for Single Word Writes, Strobe Condition of DSC=010

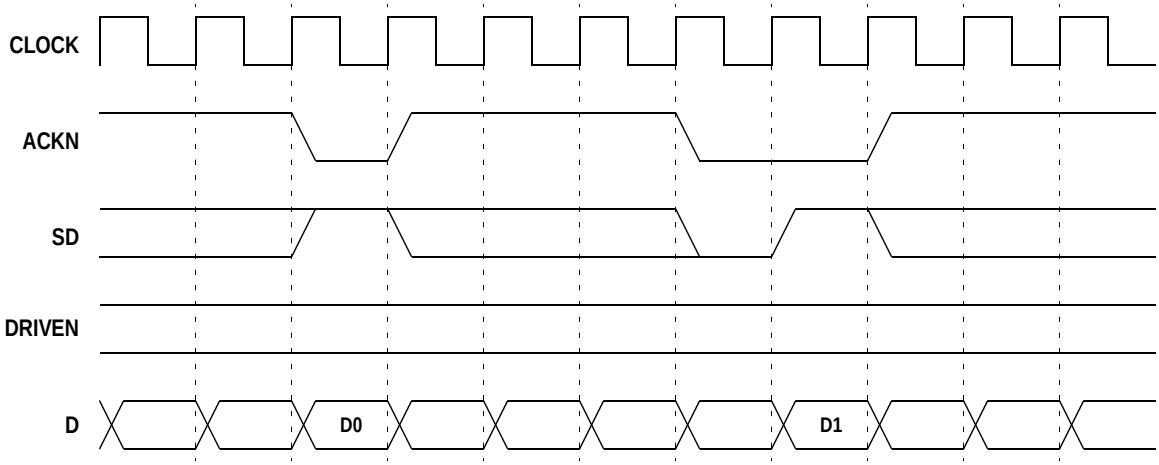


Figure A8: DMA Mode Timing for Single Word Reads, Strobe Condition of DSC=010

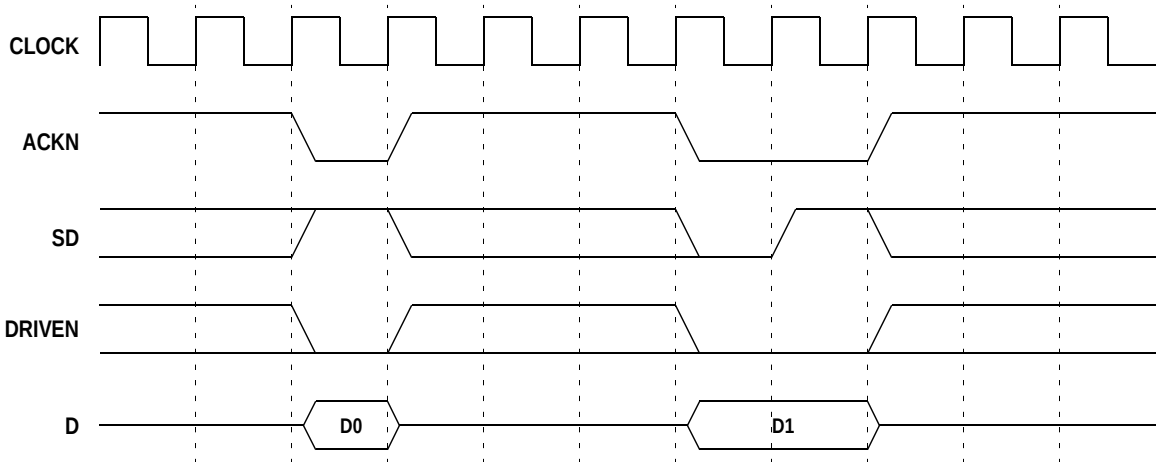


Figure A9: DMA Mode Timing for Four Word Burst Write, One Wait State, Strobe Condition of DSC=010

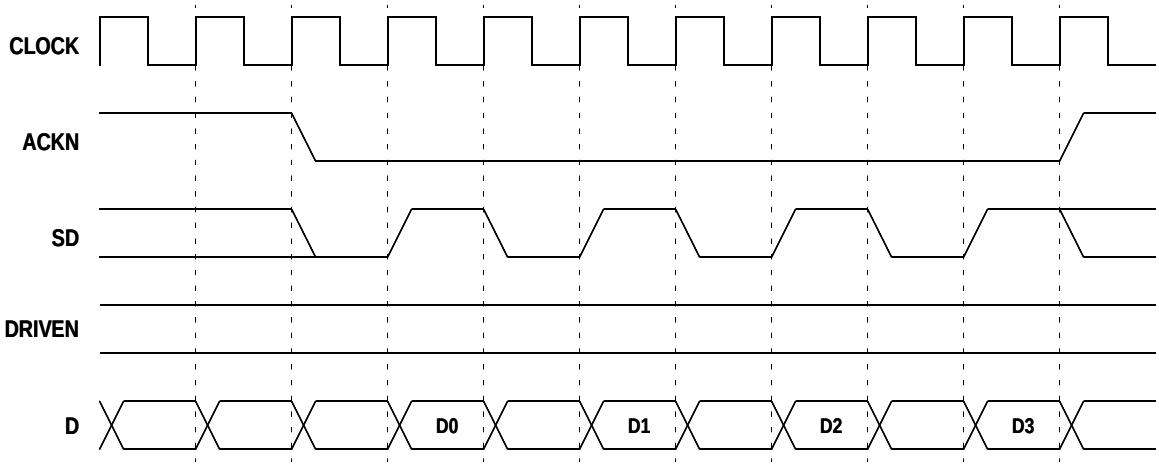


Figure A10: DMA Mode Timing for Four Word Burst Read, One Wait State, Strobe Condition of DSC=010

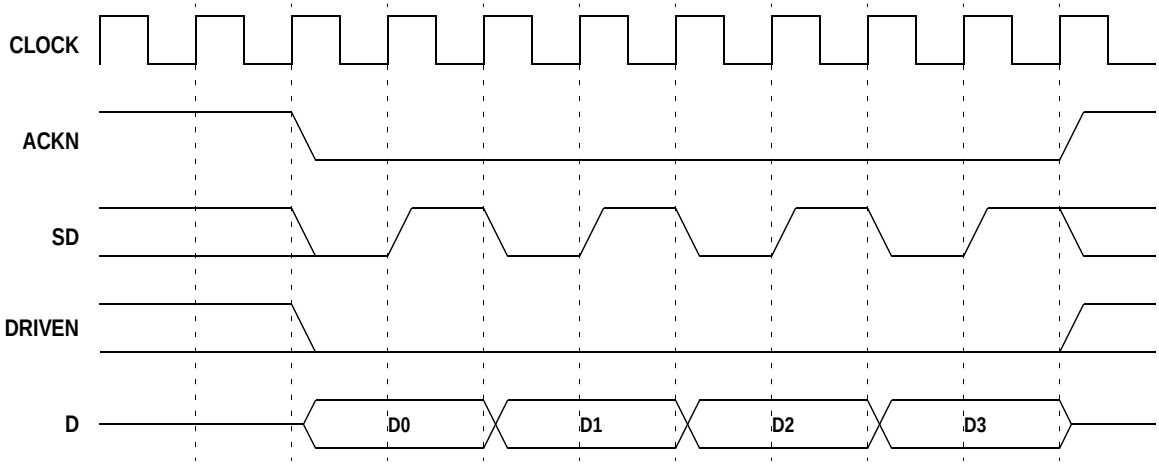


Figure A11: DMA Mode Timing for Eight Word Burst Write, Zero Wait State, Strobe Condition of DSC=010

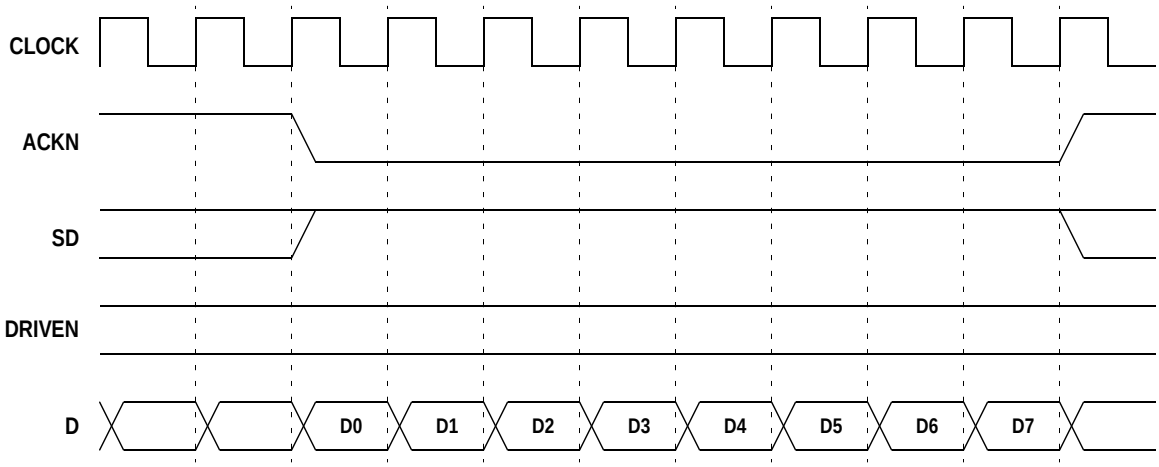


Figure A12: DMA Mode Timing for Eight Word Burst Read, Zero Wait State, Strobe Condition of DSC=010

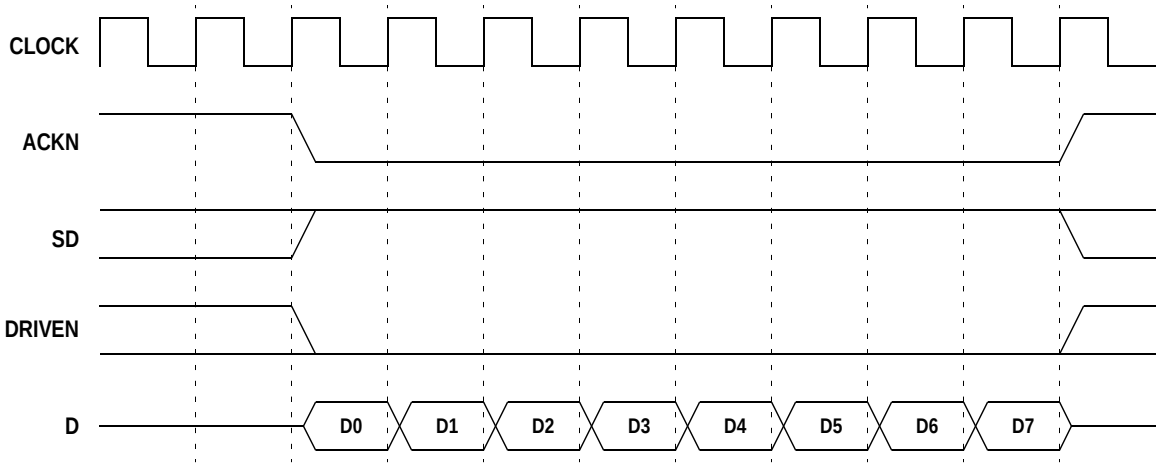


Figure A13: DMA Mode Timing for Single Word Writes, Strobe Condition of DSC=011

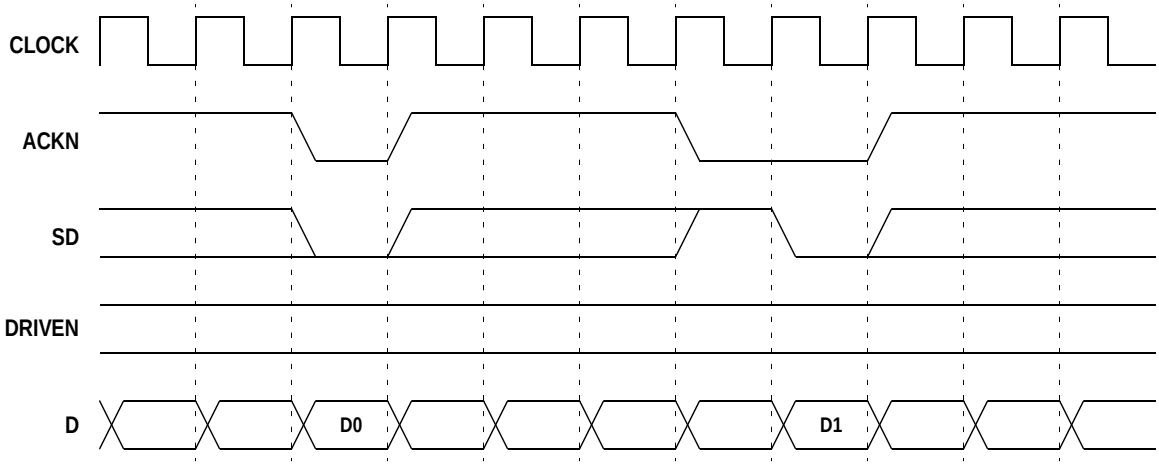


Figure A14: DMA Mode Timing for Single Word Reads, Strobe Condition of DSC=011

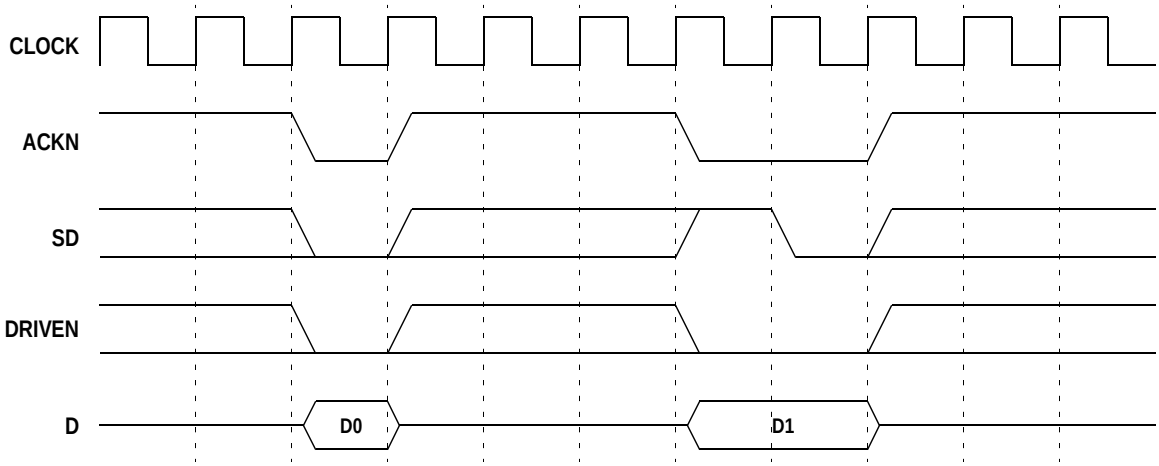


Figure A15: DMA Mode Timing for Four Word Burst Write, One Wait State, Strobe Condition of DSC=011

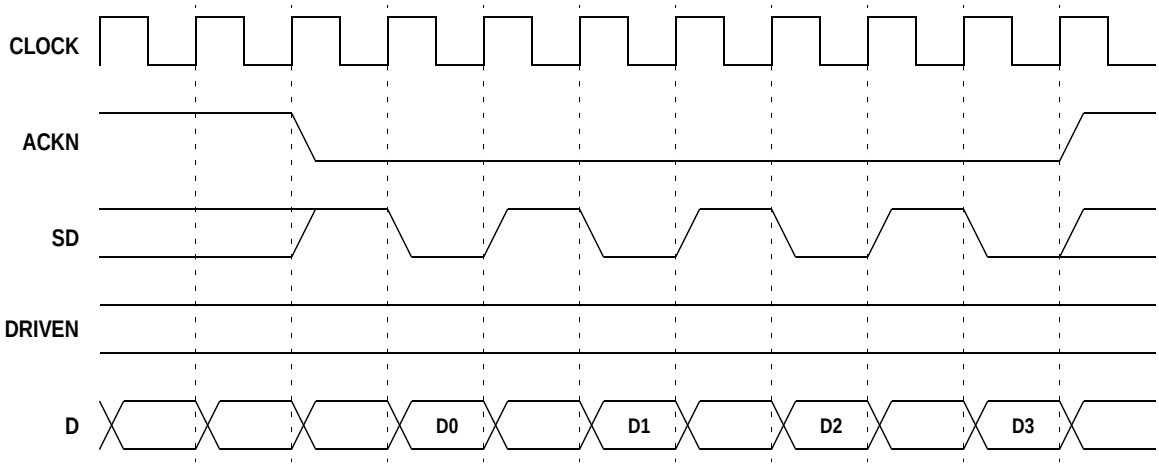


Figure A16: DMA Mode Timing for Four Word Burst Read, One Wait State, Strobe Condition of DSC=011

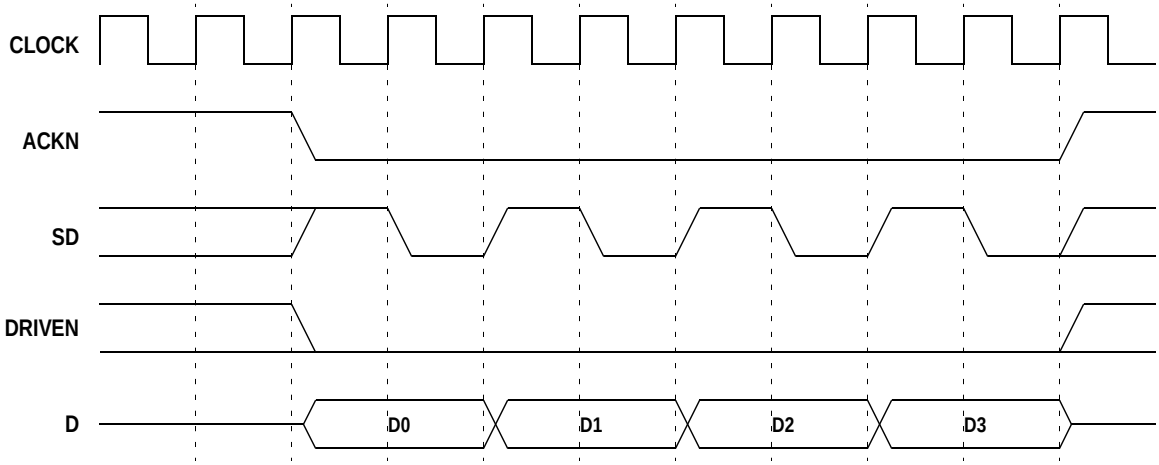


Figure A17: DMA Mode Timing for Eight Word Burst Write, Zero Wait State, Strobe Condition of DSC=011

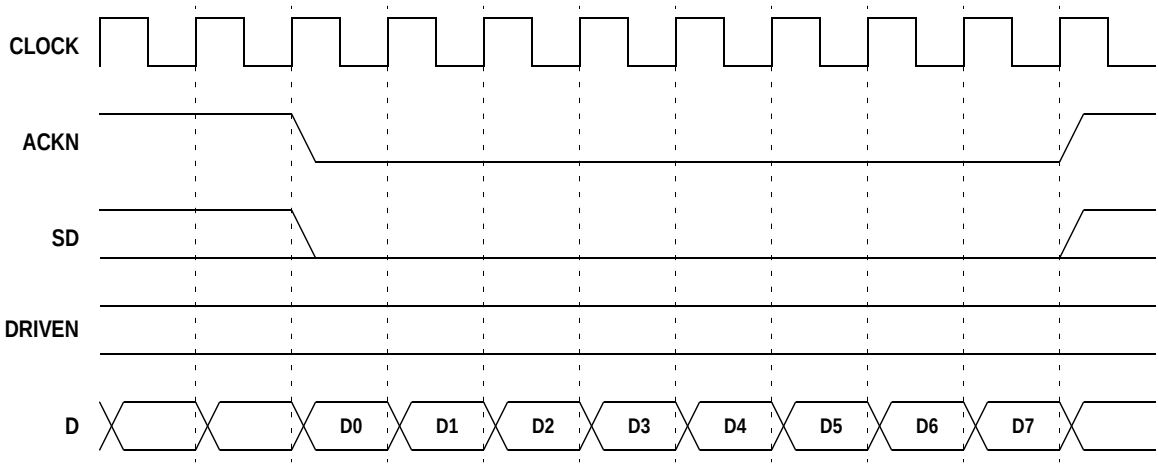


Figure A18: DMA Mode Timing for Eight Word Burst Read, Zero Wait State, Strobe Condition of DSC=011

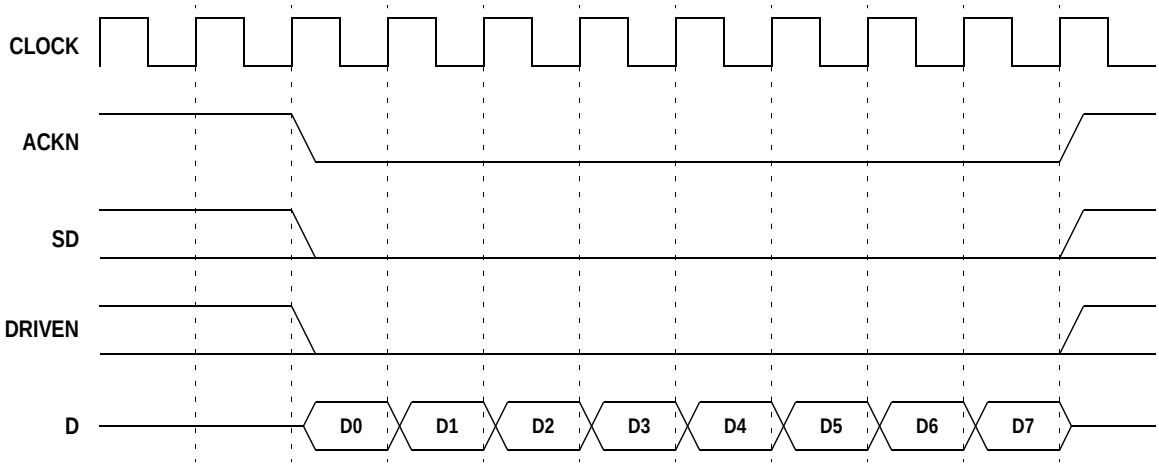


Figure A19: DMA Mode Timing for Single Word Writes, Strobe Condition of DSC=111

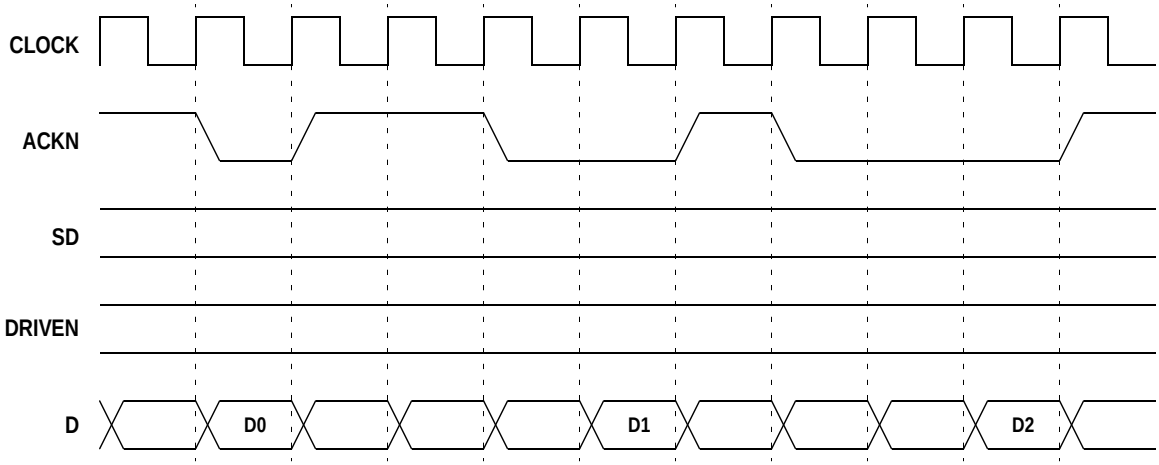
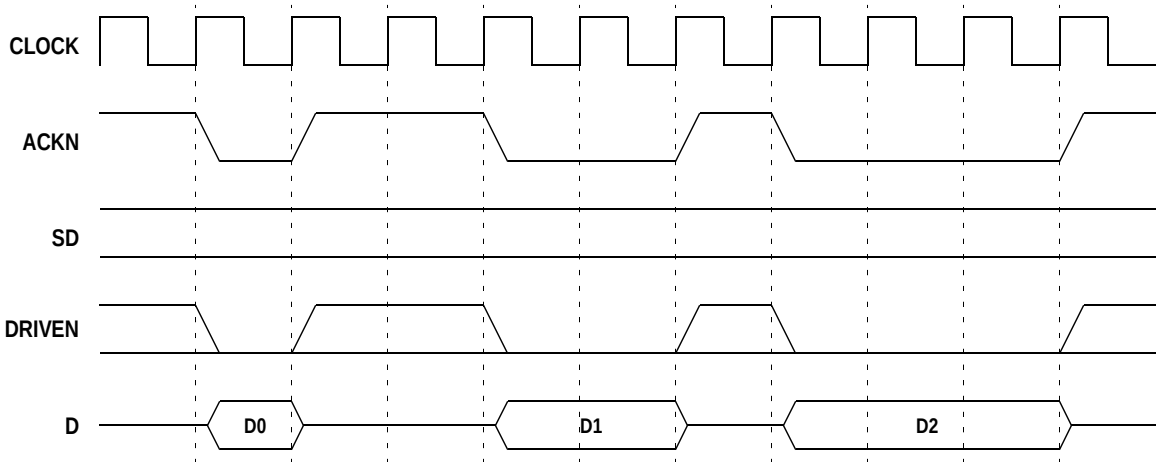
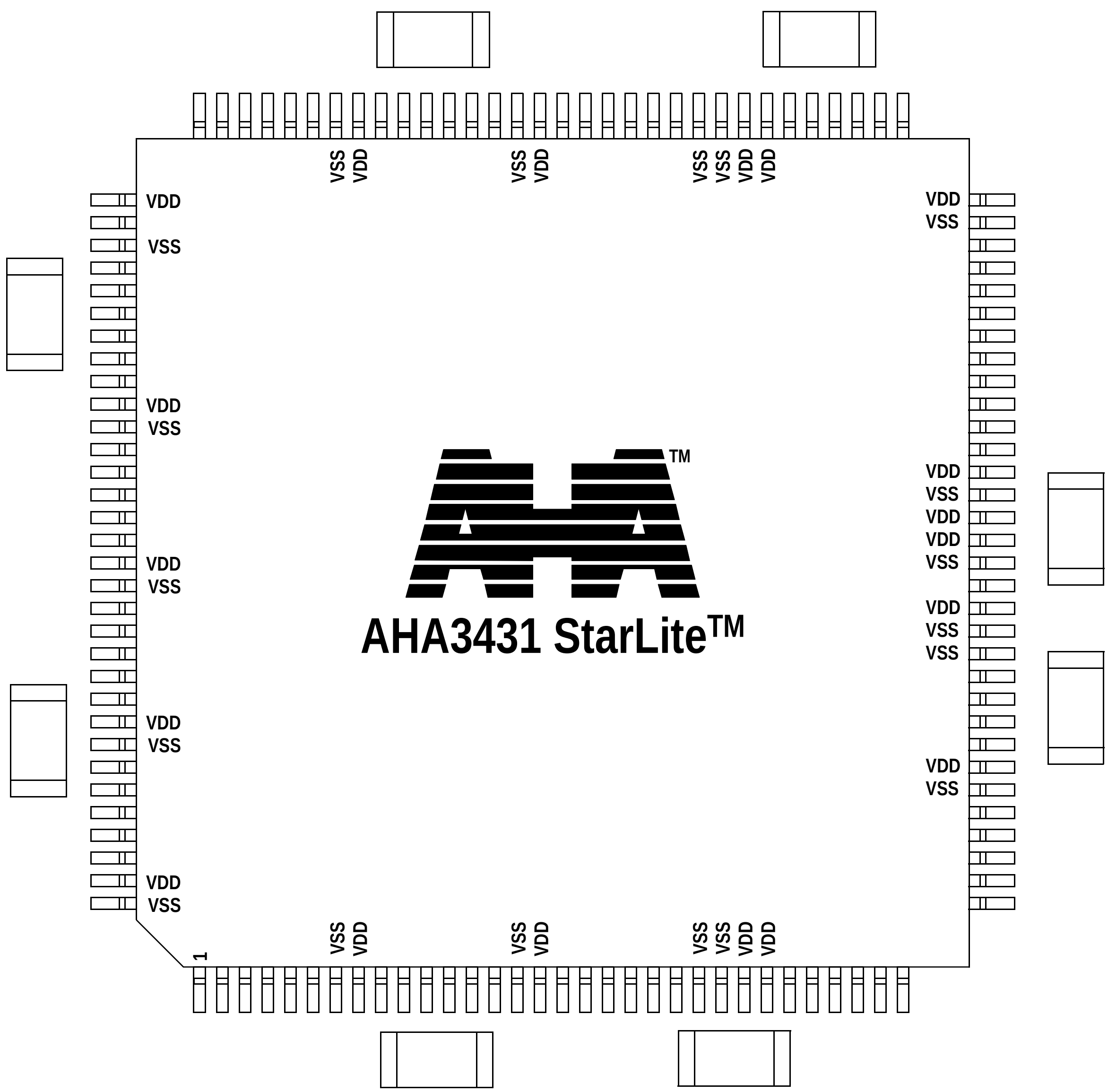


Figure A20: DMA Mode Timing for Single Word Reads, Strobe Condition of DSC=111



APPENDIX B: RECOMMENDED POWER DECOUPLING CAPACITOR PLACEMENT

RECOMMENDED POWER DECOUPLING CAPACITOR PLACEMENT



GUIDELINES FOR LOW NOISE OPERATION:

1) Use of dedicated power and ground planes within a multilayer printed circuit board is highly recommended for high speed designs.
2) Use (8) 0.047uF ceramic leadless chip capacitors placed as shown.
3) Minimize VDD trace distance from IC to capacitor VDD pad.
4) Minimize VDD trace from capacitor VDD pad to power plane via.
5) Minimize VSS trace from IC to ground plane via.