WHITE ELECTRONIC DESIGNS

PCMCIA Flash Memory Card
1 MEGABYTE through 40 MEGABYTE (Intel/Sharp based)

FEATURES

- Low cost High Density Linear Flash Card
- Supports 5V only systems or 5V systems with 12V VPP
- Based on Intel/Sharp FlashFile Components
- Fast Read Performance
  - 150ns or 200ns Maximum Access Time
- x8 / x16 Data Interface
- High Performance Random Writes
  - 8µs Typical Word Write Time
- Automated Write and Erase Algorithms
  - Command User Interface
- 100,000 Erase Cycles per Block
- 64K word symmetrical Block Architecture
- PC Card Standard Type I Form Factor

GENERAL DESCRIPTION

WEDC's FLA Series Flash memory cards offer high density linear Flash solid state storage solutions for code and data storage, high performance disk emulation and execute in place (XIP) applications in mobile PC and dedicated (embedded) equipment.

FLA series cards conform to PCMCIA international standard.

The card's control logic provides the system interface and controls the internal Flash memories. Card can be read/written in byte-wide or word-wide mode which allows for flexible integration into various systems. Combined with file management software, such as Flash Translation Layer (FTL), FLA Flash cards provide removable high-performance disk emulation.

The FLA series offers low power modes controlled by registers. Standard cards contain separate 2kB EEPROM memory for Card Information Structure (CIS) which can be used for easy identification of card characteristics.

The WEDC FLA series is based on Intel/Sharp Flash memories.

Note: Standard options include attribute memory. Cards without attribute memory are available. Cards are also available with or without a hardware write protect switch.

ARCHITECTURE OVERVIEW

WEDC's FLA series is designed to support from 2 to 20, 4Mb, 8Mb or 16Mb components, providing a wide range of density options. Cards are based on the 28F008SA (8Mb) for 12V VPP applications or on the 28F004S5 (4Mb), 28F008S5 (8Mb) and 28F016S5 (16Mb) devices for 5V only applications. Devices codes for the 28F004S5, 28F008SA, 28F008S5 and the 28F016S5 are: A7H, A2H, A6H and AAh respectively. Systems should be able to recognize all four codes. Cards utilizing the 8Mb components provide densities ranging from 2MB to 20MB in 2MB increments, cards utilizing 16Mb components provide densities ranging from 4MB to 40MB in 4MB increments. 4 Mbit memory devices are used only for smallest capacity cards (1MB).

In support of the PC Card 95 standard for word wide access devices are paired. Therefore, the Flash array is structured in 64K word (128kBytes) blocks. Write, read and block erase operations can be performed as either a word or byte wide operation . By multiplexing A_0, $CE_{1\#}$ and $CE_{2},\#$ 8-bit hosts can access all data on data lines DQ_0-DQ_7.

The **FLA21-FLA36** series also supports the following PCMCIA compatible register functions: Soft Reset via the Configuration Option Register, Power Down (sleep mode) via the Configuration and Status Register and monitoring of Ready/Busy, Soft Reset and Power Down via the Card Status Register (cards without attribute memory and versions **FLA51 - FLA66** do not have registers).

The FLA series cards conform with the PC Card Standard (PCMCIA) and JEIDA, providing electrical and physical compatibility. The PC Card form factor offers an industry standard pinout and mechanical outline, allowing density upgrades without system design changes.
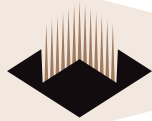
WEDC's standard cards are shipped with WEDC's Logo. Cards are also available with blank housings (no Logo). The blank housings are available in both a recessed (for label) and flat housing. Please contact WEDC sales representative for further information on Custom artwork.

WHITE ELECTRONIC DESIGNS
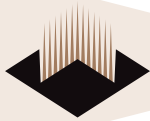
BLOCK DIAGRAM
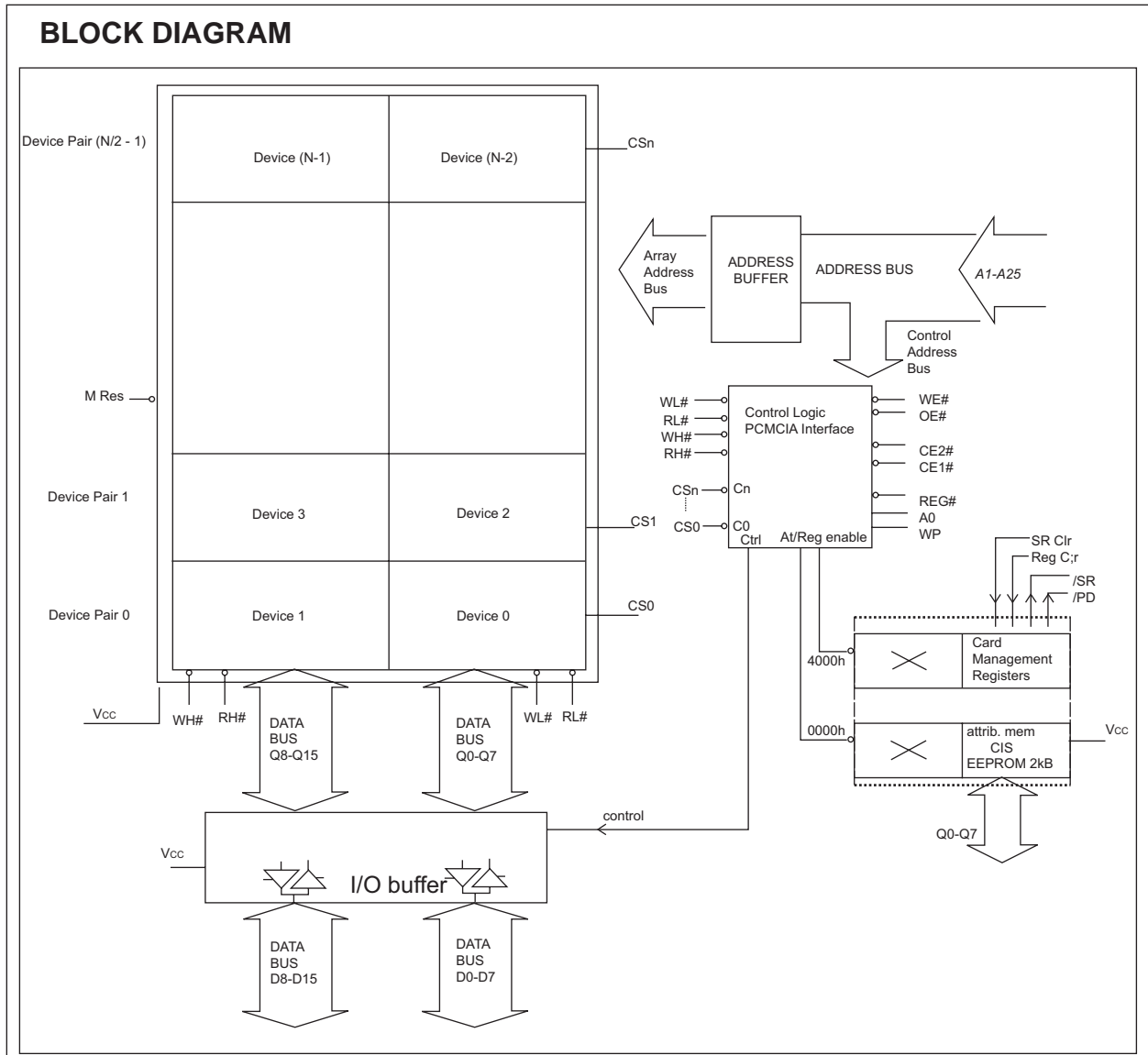
Device type	Manuf ID	Device ID
28F004S5	89$_H$	A7$_H$
28F008SA	89$_H$	A2$_H$
28F008S5	89$_H$	A6$_H$
28F016S5	89$_H$	AA$_H$

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REGISTERS IN ATTRIBUTE MEMORY SPACE*

ADDRESS	REGISTER NAME
4100h	Status Register
4002h	Config. and Status Register
4000h	Configuration Option Register

*Cards without Att. Mem and FLA51- FLA66 do not have registers

COR
CONFIGURATION OPTION REGISTER: ADRS = 4000H WRITE ONLY

SRES	LREQ	Configuration Index					
D7	D6	D5	D4	D3	D2	D1	D0

D7   Soft Reset, active High

    1 = Reset State

    0 = End Reset State

D6   Level Req (not supported)

D5-D0 Configuration index (not supported)

CSR
CONFIGURATION STATUS REGISTER: ADRS = 4002H WRITE ONLY

Not Supported					PDwn	Not Supported	
D7	D6	D5	D4	D3	D2	D1	D0

D2   Power Down, active High

    1 = Place all memory devices in power down mode
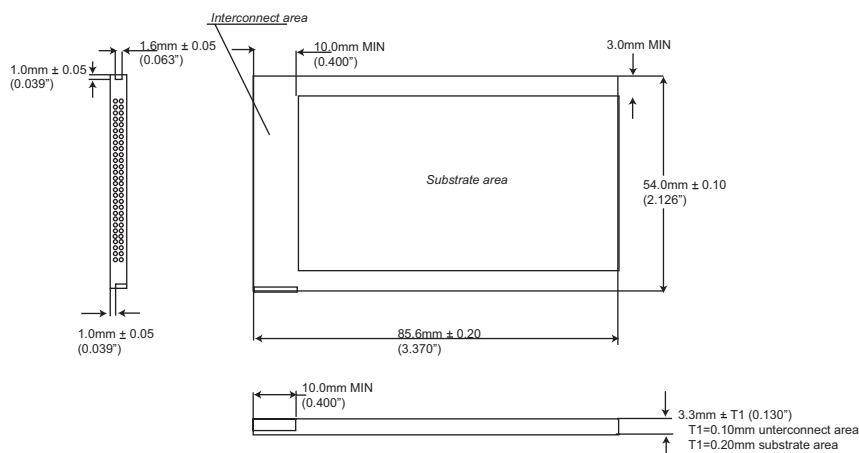
    0 = Normal Operation   Power On default = 0

SR
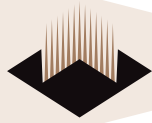## STATUS REGISTER: ADRS = 4100H
READ ONLY

Not Supported		SReset		PDwn	Not Supported		R/BSY
D7	D6	D5	D4	D3	D2	D1	D0

D5   Represents the state of SRESET bit in COR (4000h)

    1 = Reset

    0 = Normal Operation

    Power On default   D5 = 0

D3   Represents the state of Power Down bit (D2) in CSR (4002h)

    1 = Power Down

D0   Reflects the card's Ready/Busy signal (pin 16) driven by memory components Ready/Busy outputs. This bit allows software polling of the card's Ready/Busy status.

    1 = Ready

MECHANICAL

1.6mm ± 0.05 (0.063")

1.0mm ± 0.05 (0.039")

Interconnect area

10.0mm MIN (0.400")

3.0mm MIN

Substrate area

54.0mm ± 0.10 (2.126")

1.0mm ± 0.05 (0.039")

85.6mm ± 0.20 (3.370")

10.0mm MIN (0.400")

3.3mm ± T1 (0.130")
T1=0.10mm unterconnect area
T1=0.20mm substrate area

PINOUT

Pin	Signal name	I/O	Function	Active	Pin	Signal name	I/O	Function	Active
1	GND		Ground		35	GND		Ground	
2	DQ_3	I/O	Data bit 3		36	$CD_{1\#}$	O	Card Detect 1	LOW
3	DQ_4	I/O	Data bit 4		37	$DQ_{11\#}$	I/O	Data bit 11	
4	DQ_5	I/O	Data bit 5		38	DQ_{12}	I/O	Data bit 12	
5	DQ_6	I/O	Data bit 6		39	DQ_{13}	I/O	Data bit 13	
6	DQ_7	I/O	Data bit 7		40	DQ_{14}	I/O	Data bit 14	
7	$CE_{1\#}$	I	Card enable 1	LOW	41	DQ_{15}	I	Data bit 15	
8	A_{10}	I	Address bit 10		42	CE_2	I	Card Enable 2	LOW
9	OE#	I	Output enable	LOW	43	$VS_{1\#}$	O	Voltage Sense 1	NC
10	A_{11}	I	Address bit 11		44	RFU		Reserved	
11	A_9	I	Address bit 9		45	RFU		Reserved	
12	A_8	I	Address bit 8		46	A_{17}	I	Address bit 17	
13	A_{13}	I	Address bit 13		47	A_{18}	I	Address bit 18	
14	A_{14}	I	Address bit 14		48	A_{19}	I	Address bit 19	
15	WE#	I	Write Enable	LOW	49	A_{20}	I	Address bit 20	2MB(3)
16	RDY/BSY#	O	Ready/Busy	LOW (4)	50	A_{21}	I	Address bit 21	4MB(3)
17	V_{CC}		Supply Voltage		51	V_{CC}		Supply Voltage	
18	V_{PP1}		Prog. Voltage	NC	52	V_{PP2}		Prog. Voltage	NC
19	A_{16}	I	Address bit 16		53	A_{22}	I	Address bit 22	8MB(3)
20	A_{15}	I	Address bit 15		54	A_{23}	I	Address bit 23	16MB(3)
21	A_{12}	I	Address bit 12		55	A_{24}	I	Address bit 24	32MB(3)
22	A_7	I	Address bit 7		56	A_{25}	I	Address bit 25	64MB(3)
23	A_6	I	Address bit 6		57	VS_2	O	Voltage Sense 2	NC
24	A_5	I	Address bit 5		58	RST	I	Card Reset	HIGH (4)
25	A_4	I	Address bit 4		59	Wait	O	Extended Bus cycle	Low(2,4)
26	A_3	I	Address bit 3		60	RFU#		Reserved	
27	A_2	I	Address bit 2		61	REG	I	Attrib Mem Select	
28	A_1	I	Address bit 1		62	$BVD_{2\#}$	O	Bat. Volt. Detect 2	(2)
29	A_0	I	Address bit 0		63	BVD_1	O	Bat. Volt. Detect 1	(2)
30	DQ_0	I/O	Data bit 0		64	DQ_8	I/O	Data bit 8	
31	DQ_1	I/O	Data bit 1		65	DQ_9	I/O	Data bit 9	
32	DQ_2	I/O	Data bit 2		66	DQ_{10}	O	Data bit 10	
33	WP	O	Write Potect	HIGH	67	CD_2	O	Card Detect 2	LOW
34	GND		Ground		68	GND#		Ground	

Notes:

1. RDY/BSY signal is an "Open drain" type output, pull-up resistor on host side is required.
2. Wait#, BVD_1 and BVD_2 are driven high for compatibility.
3. Shows density for which specified address bit is MSB. Higher order address bits are no connects
   (ie 4MB A21 is MSB A22 - A25 are NC).
4. NC - No Connection for FLA51 - FLA66.

CARD SIGNAL DESCRIPTION

Symbol	Type	Name and Function
A0 - A25	INPUT	ADDRESS INPUTS: A0 through A25 enable direct addressing of up to 64MB of memory on the card. Signal A0 is not used in word access mode. A25 is the most significant bit
DQ0 - DQ15	INPUT/OUTPUT	DATA INPUT/OUTPUT: DQ0 THROUGH DQ15 constitute the bi-directional databus. DQ15 is the MSB.
CE1#, CE2#	INPUT	CARD ENABLE 1 AND 2: CE1# enables even byte accesses, CE2# enables odd byte accesses. Multiplexing A0, CE1# and CE2# allows 8-bit hosts to access all data on DQ0 - DQ7.
OE#	INPUT	OUTPUT ENABLE: Active low signal gating read data from the memory card.
WE#	INPUT	WRITE ENABLE: Active low signal gating write data to the memory card.
RDY/ BSY#(*)	OUTPUT	READY/BUSY OUTPUT: Indicates status of internally timed erase or program algorithms. A high output indicates that the card is ready to accept accesses. A low output indicates that one or more devices in the memory card are busy with internally timed erase or write activities.
CD1#, CD2#	OUTPUT	CARD DETECT 1 and 2: Provide card insertion detection. These signals are internally connected to ground on the card. The host shall monitor these signals to detect card insertion (pulled-up on host side).
WP	OUTPUT	WRITE PROTECT: Write protect reflects the status of the Write Protect switch on the memory card. WP set to high = write protected, providing internal hardware write lockout to the Flash array.If card does not include optional write protect switch, this signal will be pulled low internally indicating write protect = "off".
$V_{PP}1$, $V_{PP}2$	N.C.	PROGRAM/ERASE POWER SUPPLY: Provides programming voltages for card (12V). Not connected for 5V only card.
V_{CC}		CARD POWER SUPPLY: (5.0V).
GND		CARD GROUND
REG#	INPUT	ATTRIBUTE MEMORY SELECT : Active low signal, enables access to Attribute Memory Plane, occupied by Card Information Structure and Card Registers.
RST(*)	INPUT	RESET: Active high signal for placing card in Power-on default state. Reset can be used as a Power-Down signal for the memory array.
WAIT#(*)	OUTPUT	WAIT: This signal is pulled high internally for compatibility. No wait states are generated.
BVD1, BVD2	OUTPUT	BATTERY VOLTAGE DETECT: These signals are pulled high to maintain SRAM card compatibility.
VS1, VS2	OUTPUT	VOLTAGE SENSE: Notifies the host socket of the card's Vcc requirements. VS1 and VS2 are open to indicate a 5V card .
RFU		RESERVED FOR FUTURE USE
NC		NO INTERNAL CONNECTION TO CARD: pin may be driven or left floating

(*) Signals not supported by FLA51-66 (N.C)

FUNCTIONAL TRUTH TABLE

READ function							Common Memory		Attribute Memory		
Function Mode	CE2#	CE1#	A0	OE#	WE#	REG#	D_{15}-D_8	D_7-D_0	REG#	D_{15}-D_8	D_7-D_0
Standby Mode	H	H	X	X	X	X	High-Z	High-Z	X	High-Z	High-Z
Byte Access (8 bits)	H	L	L	L	H	H	High-Z	Even-Byte	L	High-Z	Even-Byte
	H	L	H	L	H	H	High-Z	Odd-Byte	L	High-Z	Not Valid
Word Access (16 bits)	L	L	X	L	H	H	Odd-Byte	Even-Byte	L	Not Valid	Even-Byte
Odd-Byte Only Access	L	H	X	L	H	H	Odd-Byte	High-Z	L	Not Valid	High-Z
WRITE function											
Standby Mode	H	H	X	X	X	X	X	X	X	X	X
Byte Access (8 bits)	H	L	L	H	L	H	X	Even-Byte	L	X	Even-Byte
	H	L	H	H	L	H	X	Odd-Byte	L	X	X
Word Access (16 bits)	L	L	X	H	L	H	Odd-Byte	Even-Byte	L	X	Even-Byte
Odd-Byte Only Access	L	H	X	H	L	H	Odd-Byte	X	L	X	X

ABSOLUTE MAXIMUM RATINGS [1]

Operating Temperature TA (ambient)	
Commercial	0°C to +60 °C
Industrial	-40°C to +85 °C
Storage Temperature	
Commercial	0°C to +60 °C
Industrial	-40°C to +85 °C
Voltage on any pin relative to Vss	-0.5V to VCC+0.5V
Vcc supply Voltage relative to Vss	-0.5V to +7.0V

Note:

(1) Stress greater than those listed under "Absolute Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS [1]

Symbol	Parameter	Density(Mbytes)	Notes	Typ[3]	Max	Units	Test Conditions
I_{CCR}	Vcc Read Current	All			35	mA	VCC = VCCmax tcycle = 150ns,CMOS levels
I_{CCW}	Vcc Program Current	All	28F008S5 28F016S5		75	mA	
I_{CCW}	Vcc Program Current	All	28F008SA		30	mA	
I_{PPW}	Vpp Program Current	All	Vpp=12V		30	mA	
I_{CCE}	Vcc Erase Current	All			100	mA	
I_{CCS} (CMOS)	Vcc Standby Current	2MB	2	110	230	µA	Vcc = VCCmax Control Signals = Vcc Reset = Vss, CMOS levels
		20MB	28F008SA	900			
		2MB	2	600			
		20MB	28F008S5	420			
		4MB	2	60			
		40MB	28F016S5	380			

CMOS Test Conditions: Vcc = 5V ± 5%, V_{IL} = Vss ± 0.2V, V_{IH} = Vcc ± 0.2V

Notes:

1. All currents are RMS values unless otherwise specified. I_{CCR}, I_{CCW} and I_{CCE} are based on Byte wide operations. For 16 bit operation values are double.
2. Control Signals: CE1#, CE2#, OE#, WE#, REG#.
3. Typical: Vcc = 5V, T = +25C.

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
I_{LI}	Input Leakage Current	1		±20	µA	Vcc = VccMAX V_{IN} =Vcc or VSS
I_{LO}	Output Leakage Current	1		±20	µA	Vcc = VccMAX V_{OUT} =Vcc or Vss
V_{IL}	Input Low Voltage	1	0	0.8	V	
V_{IH}	Input High Voltage	1	0.7Vcc	Vcc+0.5	V	
V_{OL}	Output Low Voltage	1		0.4	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage	1	Vcc-0.4	Vcc	V	I_{OH} = -2.0mA
V_{LKO}	Vcc Erase/Program Lock Voltage	1	2.0		V	

Notes:

1. Values are the same for byte and word wide modes for all card densities.

2. Exceptions: Leakage currents on CE1, CE2, OE, REG and WE will be < 500 µA when V_{IN} = GND due to internal pull-up resistors. Leakage currents on RST will be <150µA when V_{IN}=Vcc due to internal pull-down resistor.

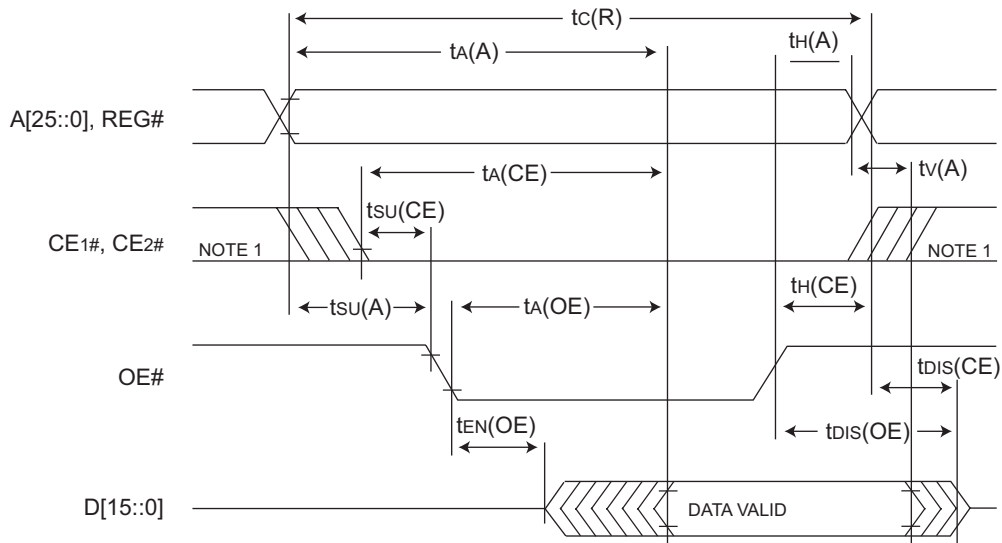White Electronic Designs Corp. reserves the right to change products or specifications without notice.
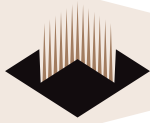
AC CHARACTERISTICS - READ TIMING PARAMETERS

SYMBOL (PCMCIA)	Parameter	150ns		
		Min	Max	Unit
$t_C(R)$	Read Cycle Time	150		ns
$t_A(A)$	Address Access Time		150	ns
$t_A(CE)$	Card Enable Access Time		150	ns
$t_A(OE)$	Output Enable Access Time		75	ns
$t_{SU}(A)$	Address Setup Time		20	ns
$t_{SU}(CE)$	Card Enable Setup Time		0	ns
$t_H(A)$	Address Hold Time		20	ns
$t_H(CE)$	Card Enable Hold Time		20	ns
$t_V(A)$	Output Hold from Address Change		0	ns
$t_{DIS}(CE)$	Output Disable Time from CE#		75	ns
$t_{DIS}(OE)$	Output Disable Time from OE#		75	ns
$t_{EN}(CE)$	Output Enable Time from CE#	5		ns
$t_{EN}(OE)$	Output Enable Time from OE#	5		ns
$t_{REC}(RSR)$	Power Down recovery to Output Delay. V_{CC} = 5V		500	ns

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

READ TIMING DIAGRAM
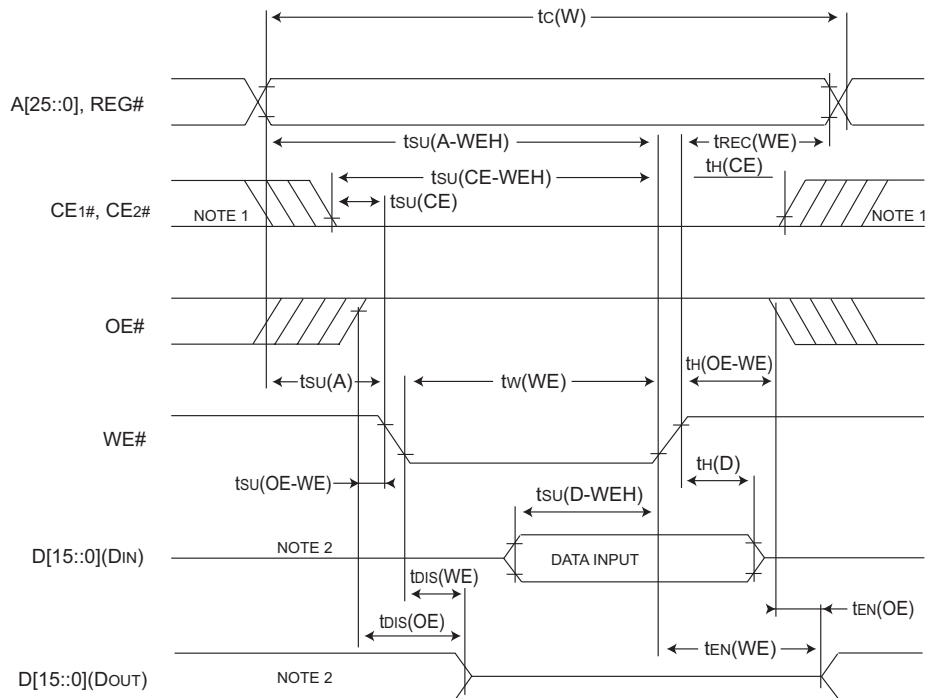

Note: Signal may be high or low in this area.

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AC CHARACTERISTICS - WRITE TIMING PARAMETERS

SYMBOL (PCMCIA)	Parameter	150ns Min	150ns Max	Unit
tcW	Write Cycle Time	150		ns
tw(WE)	Write Pulse Width	80		ns
tsu(A)	Address Setup Time	20		ns
tsu(A-WEH)	Address Setup Time for WE#	100		ns
tsu(CE-WEH)	Card Enable Setup Time for WE#	100		ns
tsu(D-WEH)	Data Setup Time for WE#	50		ns
tH(D)	Data Hold Time	20		ns
tREC(WE)	Write Recover Time	20		ns
tDIS(WE)	Output Disable Time from WE#		75	ns
tDIS(OE)	Output Disable Time from OE#		75	ns
tEN(WE)	Output Enable Time from WE#	5		ns
tEN(OE)	Output Enable Time from OE#	5		ns
tsu(OE-WE)	Output Enable Setup from WE#	10		ns
tH(OE-WE)	Output Enable Hold from WE#	10		ns
tsu(CE)	Card Enable Setup Time from OE#	0		ns

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

WRITE TIMING DIAGRAM

Note:
1. Signal may be high or low in this area.
2. When the data I/O pins are in the output state, no signals shall be applied to the data pins (D15-D0) by the host system.

DATA WRITE AND ERASE PERFORMANCE [1,3]
V_{CC} = 5V ± 5%, TA = 0C TO + 70C

Symbol	Parameter	Notes	Min	Typ[1]	Max	Units
t_{WHQV1}	Word/Byte Program time	4		8		µs
t_{EHQV1}						
t_{WHQV2}	Block Program Time	device SA		0.6	2.1	sec
t_{EHQV2}		device S5	0.4	0.5		
	Block Erase Time	device SA		1.6	10	sec

Notes:
1. Typical: Nominal voltages and T_A = 25C.
2. Excludes system overhead.
3. Valid for all speed options.
4. To maximize system performance RDY/BSY# signal should be polled.

PRODUCT MARKING

EDI
WED 7P016FLA6200C15 C995 9915

COMPANY NAME
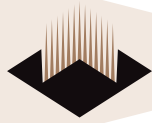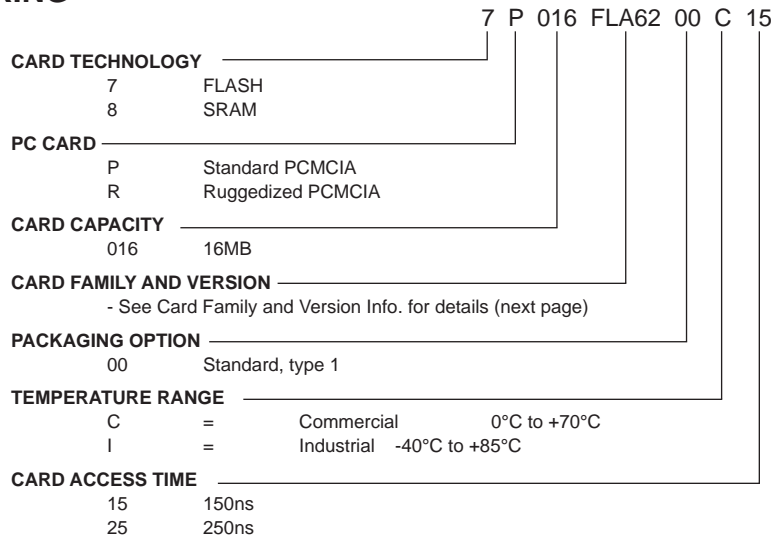
PART NUMBER

LOT CODE/TRACE NUMBER

DATE CODE

Note:
Some products are currently marked with our pre-merger company name/acronym (EDI). During our
transition period, some products will also be marked with our new company name/acronym (WED).
Starting October 2000 all PCMCIA products will be marked only with the WED prefix.

WHITE ELECTRONIC DESIGNS

PART NUMBERING

7 P 016 FLA62 00 C 15

CARD TECHNOLOGY
7   FLASH
8   SRAM

PC CARD
P   Standard PCMCIA
R   Ruggedized PCMCIA

CARD CAPACITY
016   16MB

CARD FAMILY AND VERSION
- See Card Family and Version Info. for details (next page)

PACKAGING OPTION
00   Standard, type 1

TEMPERATURE RANGE
C   =   Commercial   0°C to +70°C
I   =   Industrial   -40°C to +85°C

CARD ACCESS TIME
15   150ns
25   250ns

CARD FAMILY AND VERSION INFORMATION

FLA21-FLA24   Based on **28F008SA** (requires 12V VPP for programming and erase functions)

FLA21   No Attribute Memory, no Write Protect

FLA22   With Attribute Memory, no Write Protect

FLA23   No Attribute Memory, with Write Protect

FLA24   With Attribute Memory, with Write Protect

Example P/N   **7P004FLA2200C15**

FLA25-FLA28   Based on **28F008S5** for 5V only applications

FLA25   No Attribute Memory, no Write Protect

FLA26   With Attribute Memory, no Write Protect

FLA27   No Attribute Memory, with Write Protect

FLA28   With Attribute Memory, with Write Protect

Example P/N   **7P004FLA2600C15**

FLA29-FLA32   Based on **28F016S5** for 5V only applications

FLA29   No Attribute Memory, no Write Protect

FLA30   With Attribute Memory, no Write Protect

FLA31   No Attribute Memory, with Write Protect

FLA32   With Attribute Memory, with Write Protect

Example P/N   **7P004FLA3000C15**

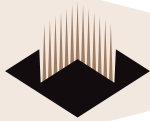**FLA33-FLA36**   Based on **28F004S5** for 5V only applications

FLA33   No Attribute Memory, no Write Protect

FLA34   With Attribute Memory, no Write Protect

FLA35   No Attribute Memory, with Write Protect

FLA36   With Attribute Memory, with Write Protect

Example P/N   **7P004FLA3600C15**

FLA51-FLA54   Based on **28F008SA**; the same as FLA21-FLA24 with exception:

- no registers

- signals RST, RDY/BSY, Wait are not connected

FLA51   No Attribute Memory, no Write Protect

FLA52   With Attribute Memory, no Write Protect

FLA53   No Attribute Memory, with Write

Protect

FLA54   With Attribute Memory, with Write Protect

Example P/N   **7P004FLA5200C15**

FLA55-FLA58   Based on **28F008S5**; the same as FLA25-FLA28 with exception:

- no registers

- signals RST, RDY/BSY, Wait are not connected

FLA55   No Attribute Memory, no Write Protect
FLA56   With Attribute Memory, no Write Protect
FLA57   No Attribute Memory, with Write Protect
FLA58   With Attribute Memory, with Write Protect

Example P/N   **7P004FLA5600C15**

FLA59-FLA62   Based on **28F016S5;** the same as FLA29-FLA32 with exception:

- no registers

- signals RST, RDY/BSY, Wait are not connected

FLA59   No Attribute Memory, no Write Protect

FLA60   With Attribute Memory, no Write Protect

FLA61   No Attribute Memory, with Write Protect

FLA62   With Attribute Memory, with Write Protect

Example P/N   **7P004FLA6000C15**

FLA63-FLA66   Based on **28F004S5**; the same as FLA33-FLA36 with exception:

- no registers

- signals RST, RDY/BSY, Wait are not connected

FLA63   No Attribute Memory, no Write Protect

FLA64   With Attribute Memory, no Write Protect

FLA65   No Attribute Memory, with Write Protect
FLA66   With Attribute Memory, with Write Protect
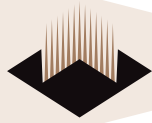
Example P/N   **7P004FLA6600C15**

ORDERING INFORMATION

7P XXX FLAYY SS T ZZ

XXX

002[1]	2MB	018[1]	18MB
004	4MB	020	20MB
006[1]	6MB	024[2]	24MB
008	8MB	028[2]	28MB
010[1]	10MB	032[2]	32MB
012	12MB	036[2]	36MB
014[1]	14MB	040[2]	40MB
016	16MB		

[1)]   *Available only for FLA21-FLA24, FLA25-FLA28, FLA51-FLA54, and FLA55-FLA59*
[2)]   *Available only for FLA29-FLA32 and FLA59-FLA62*

FLAYY

Card Family and Version (See Card Family and Version Information)

SS

00	WEDC Logo Silkscreen
01	Blank Housing, Type I
02	Blank Housing, Type I Recessed

T

C	=	Commercial	0°C to +70°C
I**	=	Industrial	-40°C to +85°C

ZZ

15	150ns

Notes: Options without attribute memory and with hardware write protect switch are available.

** Denotes advanced information.

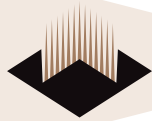White Electronic Designs Corp. reserves the right to change products or specifications without notice.

WHITE ELECTRONIC DESIGNS

CIS INFORMATION FOR FLA SERIES CARDS

ADDRESS	VALUE	DESCRIPTION
00H	01H	CISTPL_DEVICE
02H	03H	TPL_LINK
04H	53H	FLASH = 150ns (device writable)
06H	06H	CARD SIZE: 2MB
	0EH	4MB
	16H	6MB
	1EH	8MB
	26H	10MB
	2EH	12MB
	36H	14MB
	3EH	16MB
	46H	18MB
	4EH	20MB
	5EH	24MB
	6EH	28MB
	7EH	32MB
	8EH	36MB
	9EH	40MB
08H	FFH	END OF DEVICE
0AH	18H	CISTPL_JEDEC_C
0CH	02H	TPL_LINK
0EH	89H	INTEL - ID
10H	A2H	INTEL 28F008SA - ID
	A6H	INTEL 28F008S5 - ID
	AAH	INTEL 28F016S5 - ID
12H	17H	CISTPL_DEVICE_A
14H	03H	TPL_LINK
16H	42H	EEPROM - 200ns
18H	01H	Device Size = 2KBytes
1AH	FFH	END OF TUPLE
1CH	1EH	CISTPL_DEVICEGEO
1EH	06H	TPL_LINK
20H	02H	DGTPL_BUS
22H	11H	DGTPL_EBS
24H	01H	DGTPL_RBS
26H	01H	DGTPL_WBS
28H	01H	DGTPL_PART
2AH	01H	FLASH DEVICE NON-INTERLEAVED
2CH	20H	CISTPL_MANFID
2EH	04H	TPL_LINK(04H)
30H	F6H	EDI TPLMID_MANF: LSB
32H	01H	EDI TPLMID_MANF: MSB
34H	00H	LSB: Number Not Assigned
36H	00H	MSB: Number Not Assigned
38H	15H	CISTPL_VERS1
3AH	47H	TPL_LINK
3CH	05H	TPLLV1_MAJOR
3EH	00H	TPLLV1_MINOR
40H	45H	E
42H	44H	D

ADDRESS	VALUE	DESCRIPTION
44H	49H	I
46H	37H	7
48H	50H	P
4AH	30H	0
4CH		*x*
4EH		x
50H	46H	F
52H	4CH	L
54H	41H	A
56H	32H	2 based on 28F008SA
58H	32H	2 with Att. Mem. no WP
	32H	2 based on 28F008S5
	36H	6 with Att. Mem. no WP
	33H	3 based on 28F016S5
	30H	0 with Att. Mem. no WP
5AH	2DH	-
5CH	2DH	-
5EH	2DH	-
60H	31H	1
62H	35H	5
64H	20H	SPACE
66H	00H	END TEXT
68H	43H	C
6AH	4FH	O
6CH	50H	P
6EH	59H	Y
70H	52H	R
72H	49H	I
74H	47H	G
76H	48H	H
78H	54H	T
7AH	20H	SPACE
66H	00H	END TEXT
68H	43H	C
6AH	4FH	O
6CH	50H	P
6EH	59H	Y
70H	52H	R
72H	49H	I
74H	47H	G
76H	48H	H
78H	54H	T
7AH	20H	SPACE
7CH	45H	E
7EH	4CH	L
80H	45H	E
82H	43H	C
84H	54H	T

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WHITE ELECTRONIC DESIGNS

CIS INFORMATION FOR FLA SERIES CARDS (CONT.)

ADDRESS	VALUE	DESCRIPTION
86H	52H	R
88H	4FH	O
8AH	4EH	N
8CH	49H	I
8EH	43H	C
90H	20H	SPACE
92H	44H	D
94H	45H	E
96H	53H	S
98H	49H	I
9AH	47H	G
9CH	4EH	N
9EH	53H	S
A0H	20H	SPACE
A2H	49H	I
A4H	4EH	N
A6H	43H	C
A8H	4FH	O
AAH	52H	R
ACH	50H	P
AEH	4FH	O
B0H	52H	R
B2H	41H	A
B4H	54H	T
B6H	45H	E
B8H	44H	D
BAH	20H	SPACE
BCH	00H	END TEXT
BEH	31H	1
C0H	39H	9
C2H	39H	9
C4H	37H	7
C6H	00H	END TEXT
C8H	FFH	END OF LIST
CAH	1AH	CISTPL_CONF
CCH	05H	TPL_LINK
CEH	01H	TPCC_SZ
D0H	00H	TPCC_LAST
D2H	00H	TPCC_RADR
D4H	40H	TPCC_RADR
D6H	03H	TPCC_RMSK
D8H	00H	NULL CONTROL TUPLE
DAH	FFH	CISTPL_END
DCH	00H	INVALID ADDRESS

The shaded area (addresses BEH C0H C2H C4H) can be different. It represents the year of introducing the version of the card.

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WHITE ELECTRONIC DESIGNS
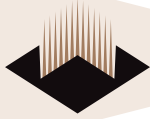
Document Title

PCMCIA Flash Memory Card FLA Series

Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	April 2007	Final
Rev 6	1.0 Update absolute maximum ratings commercial temperature to 0°C to +60 °C from 30°C to +80 °C	July 2007	Final