405EX

Preliminary Data Sheet

PowerPC 405EX Embedded Processor

Features

- AMCC PowerPC® 405 32-bit RISC processor core operating from 333 MHz to 600 MHz including 16 KB I- and D-caches with parity checking
- On-chip 128-bit processor local bus (PLB) operating up to 200 MHz
- On-chip 32-bit peripheral bus (OPB) operating up to 100 MHz
- External 8-,16-, or 32-bit peripheral bus (EBC) operating up to 100 MHz
- External bus master (EBM) operating up to 100 MHz
- On-chip Security feature with True Random Number generation
- Eight- and 16-bit NAND Flash interface
- Inter-chip connectivity (SCP and IIC)
- Boot from NOR Flash on the external peripheral bus or NAND Flash on the NAND Flash interface
- DMA (4-channel) support for all on-chip slaves and external bus, UARTs, and devices on the EBC
- DDR1/2 SDRAM interface operating up to 400 Mbps
- Two one-lane PCI Express interfaces operating up to 2.5 Gbps
- Two Gigabit Ethernet interfaces (half- and full-duplex) to external PHY (GMII/RGMII)
- USB 2.0 OTG port configurable as either Host or Device
- Programmable universal interrupt controller (UIC)
- General Purpose Timer (GPT)
- Up to two serial ports (16750 compatible UART)
- Two IIC interfaces operating up to 400 kHz and supporting all standard IIC EEPROMs
- One SCP (SPI) synchronous full-duplex channel operating up to 25 MHz
- General purpose I/Os (GPIOs), each with programmable interrupts and outputs
- Supports JTAG for board-level testing
- System power management, low power dissipation and small form factor
- Available in a RoHS compliant (lead-free) package

Description

With speeds up to 600 MHz, a flexible off-chip memory architecture, and a diverse communications package that includes PCI Express, USB 2.0 OTG, and 10/100/1000 Ethernet, the PowerPC 405EX embedded processor provides a low power and small footprint system-on-a-chip (SOC) solution for a wide range of high performance, cost-constrained embedded applications. This includes wireless LAN applications, security appliances, internet appliances, line cards, and intelligent USB peripherals. It is an easily programmable general purpose, 32-bit RISC controller that offers an upgrade path for applications in need of performance and connectivity improvements.

Technology: Cu-08 CMOS, 90 nm

Package: 388-ball, 27 mm × 27 mm, enhanced plastic ball grid array (EPBGA), 1 mm ball pitch

Power consumption (est.): less than 2 W, typical

Voltages required: 3.3 V, 2.5 V, 1.8 V (DDR2 SDRAM only), and 1.2 V

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Ordering, PVR, and JTAG Information

This section provides the part number nomenclature. For availability, contact your local AMCC sales office.

Product Name	Order Part Number (see **Notes:**)	Package	Rev Level	PVR Value	JTAG ID
PPC405EX	PPC405EX-SpBfffTx	27mm, 388-ball, EPBGA	B	0x12911477	0x1405B1E1
PPC405EX	PPC405EX-NpBfffTx	27mm, 388-ball, EPBGA	B	0x12911475	0x1405B1E1

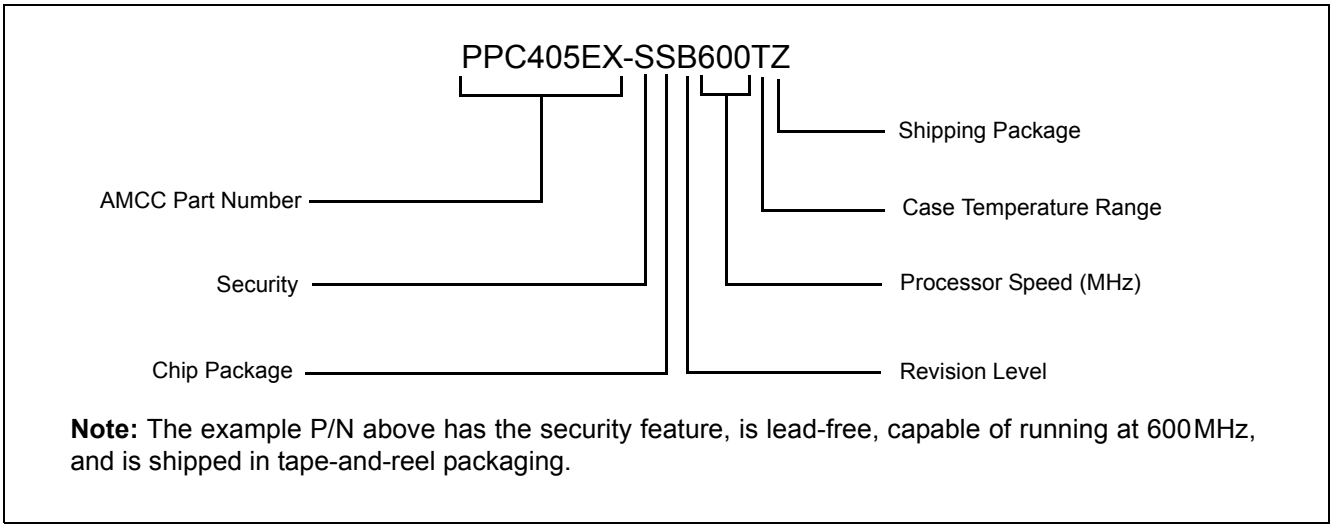
Notes:

1. S = security feature present, N = security feature not present
2. p = Package: S = lead-free (RoHS compliant), P = leaded
3. B = Chip revision level B
4. fff = Processor frequency
   - 333 = 333MHz
   - 400 = 400MHz
   - 533 = 533MHz
   - 600 = 600MHz
5. T = Case temperature range, -40°C to +85°C
6. x = Shipping package type
   - Z = tape-and-reel
   - blank = tray

The part number contains a part modifier. Included in the modifier is a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

The PVR (Processor Version Register) and the JTAG ID register are software accessible (read-only) and contain information that uniquely identifies the part. See the *PPC405EX Embedded Processor User's Manual* for details about accessing these registers.

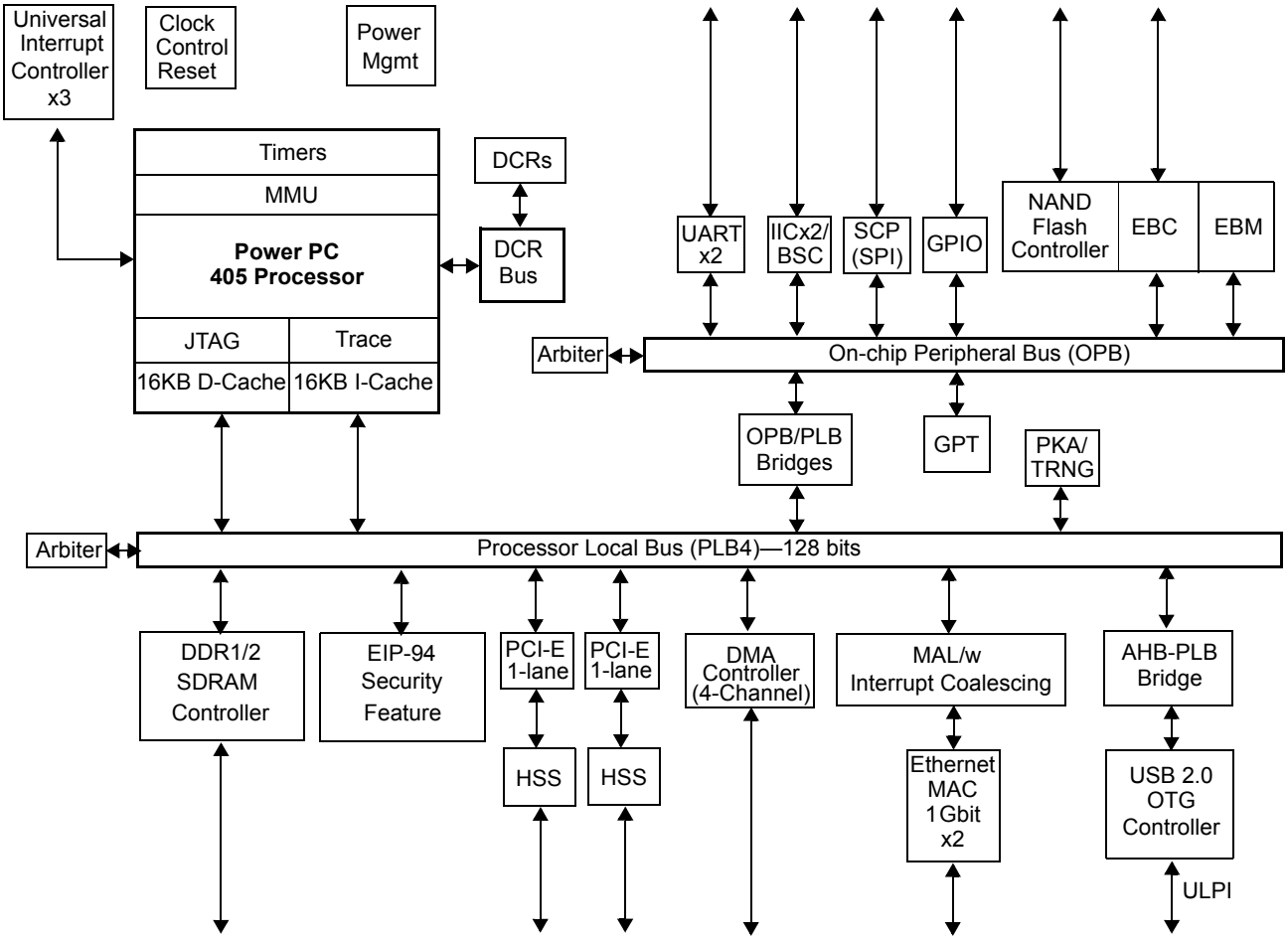
Order Part Number Key



Note: The example P/N above has the security feature, is lead-free, capable of running at 600MHz, and is shipped in tape-and-reel packaging.

Block Diagram

Figure 1. PPC405EX Embedded Controller Functional Block Diagram



The PPC405EX is designed using the IBM Microelectronics Blue Logic™ methodology in which major functional blocks are integrated together to create an ASIC (application-specific integrated circuit) product. This approach provides a consistent way to create complex ASICs using IBM CoreConnect™ Bus Architecture.

Address Maps

The PPC405EX incorporates two address maps. The first address map defines the possible use of addressable memory regions that the processor can access. The second address map defines Device Configuration Register (DCR) addresses (numbers). The DCRs are accessed by software running on the PPC405EX processor through the use of **mtdcr** and **mfdcr** instructions.

Table 1. System Memory Address Map (4 GB System Memory)

Function	Subfunction	Start Address (Hex)	End Address (Hex)	Size
Local Memory	DDR 1/2 SDRAM	0 0000 0000	0 7FFF FFFF	2GB
EBC		0 8000 0000	0 8FFF FFFF	256MB
PCI Express		0 9000 0000	0 EF5F FFFF	1.6GB
OPB Peripherals	GPT	0 EF60 0000	0 EF60 01FF	512B
	UART 0	0 EF60 0200	0 EF60 0207	8B
	Reserved	0 EF60 0208	0 EF60 02FF	248B
	UART 1	0 EF60 0300	0 EF60 0307	8B
	Reserved	0 EF60 0308	0 EF60 03FF	248B
	IIC 0	0 EF60 0400	0 EF60 041F	32B
	Reserved	0 EF60 0420	0 EF60 04FF	224B
	IIC 1	0 EF60 0500	0 EF60 051F	32B
	Reserved	0 EF60 0520	0 EF60 05FF	224B
	SCP	0 EF60 0600	0 EF60 0605	6B
	Reserved	0 EF60 0606	0 EF60 06FF	250B
	OPB Arbiter	0 EF60 0700	0 EF60 073F	64B
	Reserved	0 EF60 0740	0 EF60 07FF	192B
	GPIO	0 EF60 0800	0 EF60 087F	128B
	Reserved	0 EF60 0880	0 EF60 08FF	128B
	Ethernet 0	0 EF60 0900	0 EF60 09FF	256B
	Ethernet 1	0 EF60 0A00	0 EF60 0AFF	256B
	RGMII Bridge	0 EF60 0B00	0 EF60 0C03	260B
	Reserved	0 EF60 0C04	0 EF60 FFFF	62KB
PLB/AHB Peripherals	PKA +TRNG	0 EF61 0000	0 EF61 FFFF	64KB
	PCI Express Interrupt Handler	0 EF62 0000	0 EF62 00FF	256B
	Reserved	0 EF62 0100	0 EF6B FFFF	640KB
	USB OTG	0 EF6C 0000	0 EF6F FFFF	256KB
	Security	0 EF70 0000	0 EF77 FFFF	512KB
	Reserved	0 EF78 0000	0 EFFF FFFF	8.9MB
EBC	EBC Memory	0 F000 0000	0 FFDF FFFF	254MB
	EBC Memory—Boot ROM	0 FFE0 0000	0 FFFF FFFF	2MB

Notes:

1. If peripheral bus boot is selected, peripheral bank 0 is automatically configured at reset to the address range listed above.
2. After the boot process, software may reassign the boot memory regions for other uses.
3. PCI Express can use PLB address range 0x1 0000 0000 to 0xF FFFF FFFF even though the CPU can not access it.

Table 2. DCR Address Map

Function	Start Address (Hex)	End Address (Hex)	Size
Total DCR Address Space[1]	**0x000**	**0x3FF**	**1KW (4KB)[1]**
Reserved	000	00B	
CPR (Clocking, Power-on Reset)	00C	00D	2W
System DCRs	00E	00F	2W
DDR 1/2 SDRAM Controller	010	011	2W
External Bus Controller (EBC)	012	013	2W
External Bus Master (EBM)	014	015	2W
Reserved	016	01F	
PLB4XAHB Bridge	020	02F	16W
Reserved	030	03F	
PCI Express 0	040	05F	32W
PCI Express 1	060	07F	32W
PLB4 Arbiter	080	08F	16W
PLB-to-OPB Bridge	090	09F	16W
OPB-to-PLB Bridge	0A0	0A7	8W
Reserved	0A8	0AF	
Power Management	0B0	0B2	3W
Reserved	0B3	0BF	
UIC 0	0C0	0CF	16W
UIC 1	0D0	0DF	16W
UIC 2	0E0	0EF	16W
Reserved	0F0	0FF	
DMA	100	13F	64W
Reserved	140	17F	
Ethernet MAL	180	1FF	128W
Reserved	200	3FF	

Notes:

1. A DCR address is 10 bits (1024 or 1K unique addresses). Each unique address represents a single 32-bit (word) register, or one kiloword (KW) (which equals 4KB).

Power PC 405 Processor

The PPC405 processor is a fixed-point, 32-bit RISC unit.

Features include:
- Five-stage pipeline with single-cycle execution of most instructions, including loads and stores
- Separate, configurable 16 KB D- and I-caches, both two-way set associative
- Thirty-two 32-bit general purpose registers (GPRs)
- Unaligned load/store support
- Hardware multiply/divide
- Parity detection and reporting for the instruction cache, data cache, and translation look-aside buffer (TLB)
- Double word instruction fetch from cache
- Translation of the four GB logical address space into physical addresses
- Built-in timer and debug support
- Power management
- DCR interface is 32 bits wide
- Selectable processor vs. bus clock ratios (N:1 ratio only, where N =1, 2, 3,or 4)

Internal Buses

The PPC405EX contains four internal buses: the processor local bus (PLB), the Advanced High-Performance Bus (AHB), the on-chip peripheral bus (OPB), and the device control register (DCR) bus. High performance devices such as the processor, the DDR SDRAM memory controller, PCI Express, the Ethernet MAL, and DMA utilize the PLB. Lower bandwidth I/O interfaces such as communications and timer interfaces utilize the OPB. The daisy-chained DCR bus provides a lower bandwidth path for passing status and control information between the processor and the other on-chip peripheral functions.

PLB

The Processor Local Bus (PLB) is a high-performance on-chip bus used to connect PLB-equipped master and slave devices to the PPC405 CPU. It provides a 128-bit data path with 64-bit addressing and operates up to 200MHz. There are bridges between the PLB and the OPB.

Features include:
- Separate and simultaneous 6.4GB/s read and write data paths
- Decoupled address and data buses
- Address pipelining
- Late master request abort capability
- Hidden (overlapped) bus request/grant protocol
- Bus arbitration-locking mechanism
- Byte-enable capability allows for unaligned half word transfers and 3-B transfers
- Support for 32- and 64-B burst transfers
- Read word address capability
- Sequential burst protocol
- Guarded and unguarded memory transfers
- Simultaneous control, address, and data phases
- DMA buffered, flyby, peripheral-to-memory, memory-to-peripheral, and DMA memory-to-memory operations

AHB

The Advanced High-Performance Bus (AHB) is dedicated to the USB OTG 2.0.

Features include:
- 32-bit data path
- 32-bit address
- Synchronous to the PLB
- From 60MHz to 100MHz.

OPB

The OPB provides 32-bit address and data interfaces, and operates up to 100 MHz. There are bridges between the OPB and the PLB.

Features include:
- Pipelined read support
- Dynamic bus sizing
- Single-cycle data transfer between masters and slaves

DCR Bus

The daisy-chained DCR bus provides a path for passing status and control information between the processor core and the other on-chip cores. All DCRs are 32 bits in width with 10-bit addressing.

External Bus Controller

The external bus controller (EBC and EBM) transfers data between the PLB and external memory or peripheral devices attached to the external peripheral bus. The EBC provides direct attachment of memory devices such as ROM and SRAM, DMA device paced memory devices, and DMA peripheral devices.

Features include:
- From 60 MHz to 100 MHz speed
- Data bus is 8, 16, or 32 bits with a 27-bit address bus
- Up to four chip selects
- Arbitration and multi-master supported
- Flash ROM interface
- Boot from 8- or 16-bit NOR flash support
- Direct support for 8-,16-, or 32-bit SRAM and external peripherals
- External bus master support

NAND Flash Controller

The NAND Flash controller (NDFC) provides a simple interface between the External Bus Controller (EBC) and a variety of NAND Flash-based storage devices.

Features include:
- Attachment as internal EBC slave device
- Eight- and 16-bit NAND Flash interface
- Up to four banks of NAND Flash supported
- Device sizes:
  - 4 MB and larger supported for read/write access
  - 4 MB to 256 MB supported for boot-from-NAND flash (size supported depends on addressing mode)
- 512 B + 16 B or 2 kB + 64 B device page sizes supported
- ECC generation - hamming code, single-bit correction, double-bit detection (SEC/DED)
- Eight-bit command write, address write, and data read/write
- Interrupt on device ready (after long page write or block erase operations)
- Boot from NAND
  - Executes up to 4 KB of boot code out of first block
  - Automatic page read accesses performed based on device configuration and read address

DMA Controller

The Direct Memory Access (DMA) controller is a Processor Local Bus (PLB) master that enables faster data transfer between memory and peripherals than is possible under program control. The 4-channel DMA controller handles data transfers between memory and peripherals and from memory-to-memory. Each channel has an

independent set of registers needed for data transfer: a control register, a source address register, a destination address register, and a transfer count register.

Features include:
- Memory-to-memory transfers
- Buffered memory-to-peripheral transfers
- Buffered peripheral-to-memory transfers
- Four independent DMA channels
- Scatter/gather capability for dynamically programming multiple DMA transfers
- Programmable address increment or decrement
- Internal data buffering
- Can transfer data to/from any PLB slave, including the external bus

USB 2.0 OTG Interface

One USB 2.0 On-the-Go (OTG) controller that can be configured as either a Host or Device port.

Features include:
- Low- (Host only), Full- and High-Speed support
- Internal DMA to optimize performance and offload the CPU
- Up to two IN/OUT Endpoints in Device mode (one can be isochronous)
- Supports maximum packet size of 1024B (isochronous) and 512B (bulk)
- Support for isochronous traffic
- Three packets per microframe (24MB/s throughput)
- Eight KB buffer
- ULPI SDR interface

DDR1/2 SDRAM Controller

The Double Data Rate 1/2 (DDR1/2) SDRAM memory controller supports industry standard discrete devices that are compatible with both the DDR1 or DDR2 specifications. The correct I/O supply voltage must be provided for the two types of DDR devices: DDR1 devices require +2.5V and DDR2 devices require +1.8V.

Global memory timings, address and bank sizes, and memory addressing modes are programmable.

Features include:
- 16- or 32-bit memory interface
- Optional 8-bit error checking and correcting (ECC)
- 1.6-GB/s peak data rate
- Two memory banks of up to 1 GB each
- Maximum capacity of 2GB
- Support for one memory bank of 2GB with CAS latencies of 2, 2.5, or 3
- Clock frequencies from 133MHz (266Mbps) to 200MHz (400Mbps) supported (Faster parts may be used, but must be clocked no faster than 200MHz)
- Page mode accesses (up to 16 open pages) with configurable paging policy
- Programmable address mapping and timing
- Software initiated self-refresh
- Power management (self-refresh, suspend)
- Two regions (two chip selects, one clock driver)

PCI Express

The PCI Express single-lane interfaces include the following features:

Features include:
- Compliant with PCI Express base specification 1.1
- Each PCI Express port can be End Point or Root Complex. (Upstream & Downstream)
  - Applications compliant with MSI rules are limited to one End Point port per PPC405EX
- PCI-Express to PCI-Express opaque (Non-Transparent) bridge
- Power Management
- Supports one virtual channel (VC0) with no Traffic Class (TC) filtering
- Maximum Payload block size 256B
- Supports up to 512B maximum Read request size
- Requests supported:
  - Up to two posted outbound Write requests (memory and messages)
  - Up to two posted inbound Write requests
  - Up to two outbound Read requests outstanding on PCI Express
  - Up to two inbound Read requests outstanding on PCI Express
  - Outbound I/O request as a PCI Express Root Port
  - Inbound I/O request as a PCI Express End Point
- Buffering in each PCI Express Port for the following transaction types:
  - 1KB Replay buffer: up to eight in flight transactions
  - 512B for Outbound posted Writes
  - 512B for Outbound Reads completion
  - 512B for Inbound posted Writes
  - 512B for Inbound Reads completion
- Parity checking on each buffer
- POM Programmable Outbound Memory Regions: 3 Memory, 1 I/O, 1 Message, 1 config, 1 Internal Regs
- PIM Programmable Inbound Memory Regions: 4 Memory, 1 I/O, 1 Expansion ROM
- INTx Interrupts support (PCI legacy):
  - Up to four INTx Termination for Root Ports. A/B/C/D interrupts are wired to the UIC
  - A/B/C/D INTx types Generation for Endpoints
- MSI - Message Signaled Interrupts
  - MSI Generation for End Point
  - MSI Termination for Root Ports
  - MSI_X Termination for Root Ports

Security Function

The built-in security function is a cryptographic engine attached to the 128-bit PLB with built-in DMA and interrupt controllers.

Features include:
- Federal Information Processing Standard (FIPS) 140-2 design
- Support for an unlimited number of Security Associations (SA)
- Different SA formats for each supported protocol (IPsec, SSL/TLS/DTLS, MACSec, SGT L2/L3 and sRTP)
- Internet Protocol Security (IPSec) features
  - Full packet transforms (ESP & AH)
  - Complete header and trailer processing (IPv4 and IPv6)
  - Multi-mode automatic padding
  - "Mutable bit" handler for AH, including IPv4 option and IPv6 extension headers
- Secure Socket Layer (SSL), Transport Layer Security (TLS), and Datagram Transport Layer Security (DTLS)
  - Packet transforms
  - One-pass hash-then-encrypt or decrypt-then-hash for SSL, TLS and DTLS packet transforms using ARC4 Stream Cipher

- Secure Real-Time Protocol (sRTP) features
  - Packet transforms
  - ROC removal and TAG insertion
  - Variable bypass offset of header length per packet
- Media Access Control Security (MACSec) features
  - Cipher suite GCM-AES-128
  - Header insertion and removal
  - Integrity and confidentiality with MSDU
- SGT L2 supported features:
  - GCM-AES with 128-bit key.
  - Integrity only and with confidentiality of MSDU
- ICV generation and validation SGT L3 supported features
  - AES-GCM, AES-GMAC with 128, 192 and 256 bit key.
- IPsec/SSL security acceleration engine
- DES, 3DES, AES, ARC-4, AES-GCM, and GMAC-AES encryption/decryption
- MD-5, SHA-1, and SHA-256 hashing
- Public key acceleration for RSA, DSA and Diffie-Hellman
- Combined encryption-hash and hash-decryption with the AES-CCM algorithm.
- True or pseudo random number generators
  - Non-deterministic true random numbers
  - Pseudo random numbers with lengths of 8B or 16B
  - ANSI X9.17 Annex C compliant using a DES algorithm
- Interrupt controller
  - Fifteen programmable, maskable interrupts
  - Initiate commands via an input interrupt
  - Sixteen programmable interrupts indicating completion of certain operations
  - All interrupts mapped to one level- or edge-sensitive programmable interrupt output
- DMA controller
  - Autonomous, 4-channel
  - 1024-words (32 bits/word) per DMA transfer
  - Scatter/gather capability with byte aligned addressing
  - Byte reverse capability on SA and descriptors

UART

The Universal Asynchronous Receiver/Transmitter (UART) interface provides four configurations:
- One 8-signal port
- Two 4-signal ports.
- Two 2-signal ports
- One 4-signal port and one 2-signal port

The UART performs serial-to-parallel conversion on data received from a peripheral device or a modem, and parallel-to-serial conversion on data received from the processor.

Features include:
- Compatible with the16750
- All six software modem control functions (CTS, RTS, DSR, DTR, RI, DCD) on UART0
- Programmable auto flow (data flow controlled by RTS and CTS signals)
- Characters can be 5, 6, 7, or 8 bits
- Programmable start, stop, parity bit insertion
- Sixty-four byte FIFOs for buffering Tx and Rx data
- LIN sub-bus specification compliant - line break generation/detection and false start bit detection
- Programmable internal/external loopback capabilities
- Low Power and Sleep mode
- Register conformance (after reset) to configuration of the NS16450 register set

- Hold and shift registers (eliminate need for precise synchronization between processor and serial data in character mode)
- Complete status reporting
- Full prioritized interrupt system controls
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud generator (divides serial clock input and generates 16x clock)
- Ability to add/delete standard asynchronous communication bits such as start, stop, and parity to/from serial data
- Even, odd, or no-parity bit generation and detection
- Stop bit generation of 1, 1.5, or 2 bits
- Variable baud rate
- Internal diagnostic capability
- Loopback controls for isolating communications link faults
- Break, parity, overrun, framing error simulation
- OPB interface with optional DMA support

IIC Bus Interface

The Inter-Integrated Circuit (IIC) interface provides a Philips I^2C™ compatible interface operating up to 400 kHz either as a master, a slave, or both with a bootstrap controller (BSC) included. During chip reset, the bootstrap controller can read configuration data from an IIC compatible memory device (e.g., EEPROM). This data can be used to replace the default configuration settings provided by the chip.

Features include:

- Two IIC channels
- Compliant with *Philips Semiconductors I^2C Specification*, dated 1995
- Operation at 100 kHz or 400 kHz
- Byte (8-bit) data
- Addresses are 10 or 7 bits
- Slave Transmit and Receive
- Master Transmit and Receive
- Multiple bus masters supported
- Programmable as master, slave, or master/slave
- Boot parameters read from IIC attached memory (Port 0) with IIC bootstrap controller
- OPB slave interface is 32 bits wide

Serial Communication Port Interface (SCP/SPI)

The Serial Communication Port (SCP) (also known as the Serial Peripheral Interface or SPI) is a full-duplex, synchronous, character-oriented (byte) port that allows the exchange of data with other serial devices. The SCP is a master on the serial port supporting a three-wire interface (receive, transmit, and clock), and is a slave on the OPB.

Features include:

- One SCP channel, full duplex synchronous
- SCP master
- Up to 25 MHz
- Programmable internal loopback capabilities
- Multi-master protocol supported
- Independent masking of all interrupts (master collision, transmit FIFO overflow, transmit FIFO empty, receive FIFO full, receive FIFO underflow, receive FIFO overflow)
- Dynamic control of serial bit rate of data transfer (serial-master mode only)
- Data Item size for each data transfer under programmer control (4-to-16 bits)
- OPB slave interface is 32 bits wide

General Purpose I/O (GPIO) Controller

The GPIO controller enables multiplexing of module I/O pins with multiple functions within the chip. That is, a single package pin can be assigned to multiple I/O functions. Which function the pin is assigned to is determined by register bit settings controlled by software. This significantly reduces the number of package pins needed to support multiple I/O groups.

Features include:
- Up to 32 GPIOs available
  - GPIOs are multiplexed with alternate functions
  - If not in use for dedicated functions, I/Os are available as GPIOs
- Direct control of all functions from registers programmed by means of OPB bus master accesses
- Time multiplexing of controller outputs to module outputs
- Programmable conversion of module outputs to open-drain outputs (enables sharing of active low outputs externally)
- Time multiplexing of module inputs to controller inputs

Universal Interrupt Controller (UIC)

The Universal Interrupt Controller (UIC) provides the control, status, and communications necessary between the various sources of interrupts and the PPC405 processor.

Features include:
- Ten external interrupt sources supported
- Generate interrupt on level (high or low) or edge (rising or falling)
- Programmable as synchronous (edge-capture or level-sensitive) or asynchronous (edge- or level-sensitive triggering)
- Each interrupt source/bit programmable as critical or non critical
- DCR bus interface is 32 bits wide
- Optional interrupt handler vector generation
  - Programmable vector base address
  - Programmable vector offset size
  - Programmable interrupt priority ordering
- Programmable polarity for all interrupt types
- Interrupts of the same type do not need to be in contiguous bit positions
- Status registers provide: current state of all interrupts, current state of enabled interrupts

Gigabit Ethernet

The Ethernet support provides two Gigabit (10/100/1000 Mbps) interfaces (GMII/RGMII).

Features include:
- ANSI/IEEE Std. 802.3 and IEEE 802.3u supplement compliant
- Half-duplex and full-duplex supported
- Receive and transmit FIFOs are 16K bytes each with programmable thresholds
- FCS control for transmit/receive packets
- Multiple packet handling in transmit and receive FIFOs
- Unicast, multicast, broadcast, and promiscuous address filtering
- Two 256-bit hash filters for unicast and multicast frames
- Automatic retransmission of collided frames
- Runt frame rejection
- Programmable inter-frame gap
- IEEE 802.3x compliant for frame-based flow control mechanism, including self-assembled control frame transmitting)
- Wake-on-LAN and Power-over-Internet supported

- Programmable internal/external loopback capabilities
- OPB slave (MAC) and PLB master (MAL) interfaces are 32 bits wide
- Extensive error/status vector generation for each processed packet
- VLAN tag ID supported (according to IEEE Draft 802.3ac/D1.0 standard)
- Programmable automatic source address inclusion/replacement for transmit packets
- Programmable automatic Pad/FCS stripping for receive packets
- Programmable VLAN Tag inclusion/replacement for transmit packets
- Half- or full-duplex GMII/RGMII
- Jumbo frames support
- Memory Access Layer (MAL) provides DMA capability to Ethernet channel
- Interrupt coalescence support for two transmit and two receive channels

General Purpose Timer (GPT)

The GPT provides a time base counter and system timers in addition to those defined in the processor.

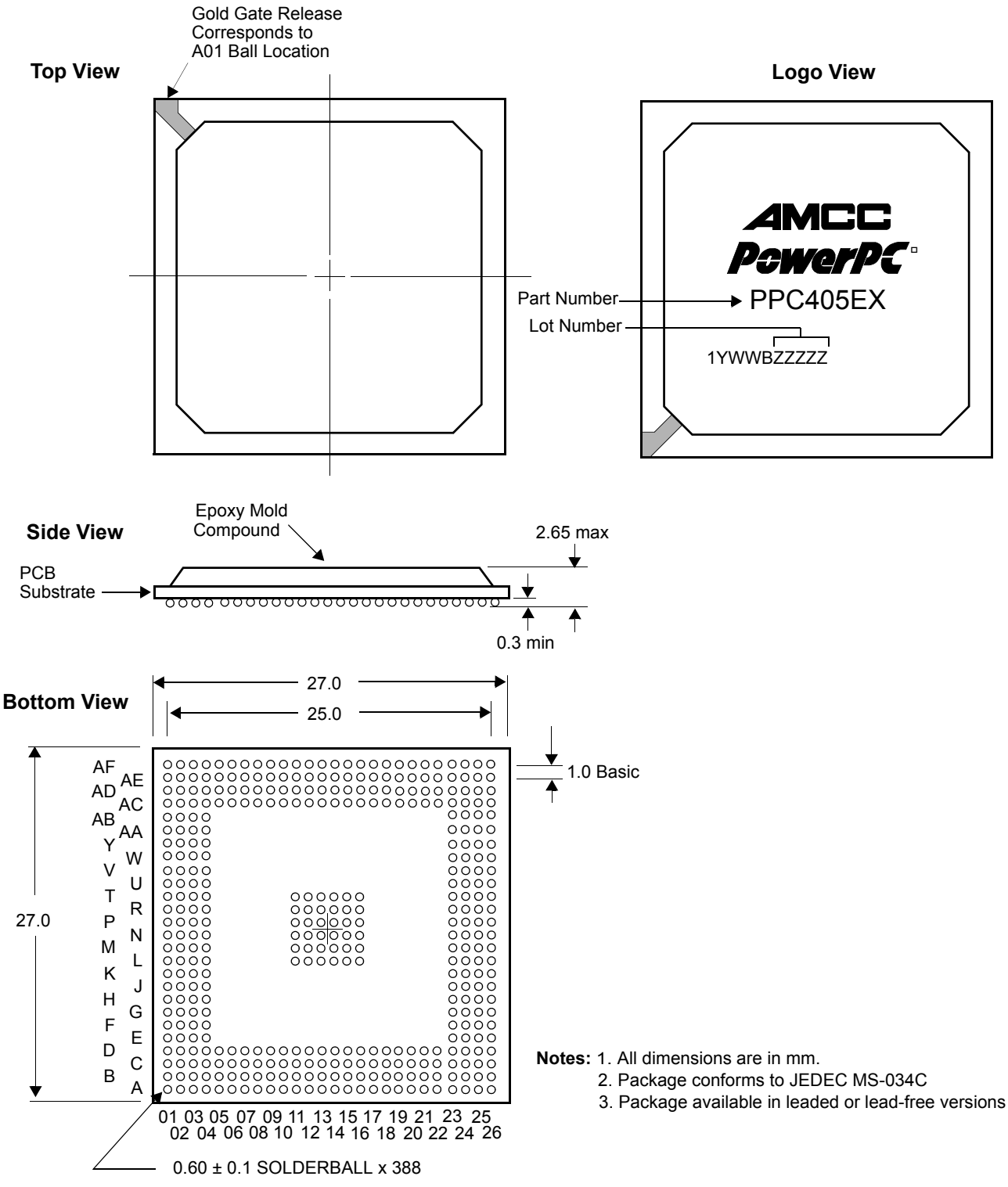
Features include:
- 32-bit time base counter driven by the OPB clock
- Seven 32-bit compare timers

JTAG

Features include:
- IEEE 1149.1 test access port
- JTAG Boundary Scan Description Language (BSDL)

Refer to **http://www.amcc.com/Embedded/Partners** for a list of AMCC partners supplying probes for use with the JTAG interface.

Figure 2. Package 27mm, 388-Ball EPBGA



Notes: 1. All dimensions are in mm.
2. Package conforms to JEDEC MS-034C
3. Package available in leaded or lead-free versions

Signal Lists

The following table lists all the external signals in alphabetical order and shows the ball (pin) number on which the signal appears. Shared signals are shown with the default signal (following reset) *not* in brackets and the alternate signal in brackets. Signals that have different functions for different modes with the same function are separated by commas.

Shared signals appear alphabetically multiple times in the list—once for each signal name on the ball. The Page column indicates the page within the table “Signal Functional Description” on page 39 on which the signals in the indicated interface group begin.

Table 3. Signals Listed Alphabetically (Sheet 1 of 13)

Signal Name	Ball	Interface Group	Page
AGND	K01	Power	45
AGND	L04		
AGND	P04		
AGND	R01		
AHV_{DD}	M04	Power	45
AHV_{DD}	R04		
AV_{DD}	J03	Power	45
AV_{DD}	K04		
AV_{DD}	M01		
AV_{DD}	N03		
AV_{DD}	N04		
AV_{DD}	P01		
AV_{DD}	T01		
BA0	AD22	DDR 1/2 SDRAM	43
BA1	AF24		
BA2	AE24		
$\overline{\text{BankSel0}}$	AF21	DDR 1/2 SDRAM	43
$\overline{\text{BankSel1}}$	AE20		
[BusReq]GPIO27[DMAEOT3][IRQ5]	B03	External Bus Master	42
$\overline{\text{CAS}}$	AF20	DDR 1/2 SDRAM	43
DM0	M25	DDR 1/2 SDRAM	43
DM1	T26		
DM2	AD16		
DM3	AD13		
DM4	Y26		
[DMAAck0]PerAddr07[TS1]	J26	DMA	42
[DMAAck1]GPIO31[IRQ0]	D01		
[DMAAck2][HoldReq]GPIO22	B05		
[DMAAck3][$\overline{\text{ExtAck}}$]GPIO25[IRQ3]	C04		
[DMAEOT0][PerAddr05]GPIO26[TS3]	K26	DMA	42
[DMAEOT1]GPIO29[IRQ2]	D03		
[DMAEOT2][$\overline{\text{ExtReq}}$]GPIO24[IRQ4]	A03		
[DMAEOT3][BusReq]GPIO27[IRQ5]	B03		
[DMAReq0]PerAddr06[TS2]	K25	DMA	42
[DMAReq1]GPIO30[IRQ1]	D02		
[DMAReq2][HoldAck]GPIO23	C05		
[DMAReq3]PerAddr08[TS0]	J25		

Table 3. Signals Listed Alphabetically (Sheet 2 of 13)

Signal Name	Ball	Interface Group	Page
DQS0	M26	DDR 1/2 SDRAM	43
DQS1	T25		
DQS2	AE16		
DQS3	AE12		
DQS4	Y25		
EAGND	AE07	Power	45
EAV_{DD}	AE08		
ECC0	V24	DDR 1/2 SDRAM	43
ECC1	W24		
ECC2	AB26		
ECC3	AB25		
ECC4	V25		
ECC5	W25		
ECC6	AA26		
ECC7	AA25		
EOV_{DD}	D12	Power	45
EOV_{DD}	T12		
EOV_{DD}	AC05		
EOV_{DD}	AB04		
EOV_{DD}	AC07		
EOV_{DD}	AC08		
[$\overline{\text{ExtAck}}$]GPIO25[DMAAck3][IRQ3]	C04	External Bus Master	42
[$\overline{\text{ExtReq}}$]GPIO24[DMAEOT2][IRQ4]	A03		
$\overline{\text{ExtReset}}$	B19		

Table 3. Signals Listed Alphabetically (Sheet 3 of 13)

Signal Name	Ball	Interface Group	Page
GMCCD, GMC1RxClk	AD04	Ethernet	39
GMCCrS, GMC1TxClk	AF04		
GMCGTxClk, GMC0TxClk	AE04		
GMCMDClk	AE03		
GMCMDIO	AF02		
GMCRefClk	AD07		
GMCRxClk, GMC0RxClk	AD09		
GMCRxD0, GMC0RxD0	AC11		
GMCRxD1, GMC0RxD1	AE10		
GMCRxD2, GMC0RxD2	AD10		
GMCRxD3, GMC0RxD3	AF09		
GMCRxD4, GMC1RxD0	AE09		
GMCRxD5, GMC1RxD1	AF07		
GMCRxD6, GMC1RxD2	AF06		
GMCRxD7, GMC1RxD3	AE06		
GMCRxDV, GMC0RxCtl	AE05		
GMCRxEr, GMC1RxCtl	AF05		
GMCTxClk	AC06		
GMCTxD0, GMC0TxD0	AE01		
GMCTxD1, GMC0TxD1	AD02		
GMCTxD2, GMC0TxD2	AD01		
GMCTxD3, GMC0TxD3	AC03		
GMCTxD4, GMC1TxD0	AC02		
GMCTxD5, GMC1TxD1	AC01		
GMCTxD6, GMC1TxD2	AB03		
GMCTxD7, GMC1TxD3	AB02		
GMCTxEn, GMC0TxCtl	AD05		
GMCTxEr, GMC1TxCtl	AF03		

Table 3. Signals Listed Alphabetically (Sheet 4 of 13)

Signal Name	Ball	Interface Group	Page
GND	A01		
GND	A08		
GND	A13		
GND	A19		
GND	A26		
GND	B01		
GND	B02		
GND	B25		
GND	C01		
GND	C02		
GND	C03		
GND	C24		
GND	D04		
GND	D09		
GND	D14		
GND	D18		
GND	D23		
GND	E01		
GND	E03		
GND	H01		
GND	H26		
GND	J04	Power	45
GND	J23		
GND	K24		
GND	L11		
GND	L13		
GND	L16		
GND	M12		
GND	M13		
GND	M14		
GND	M15		
GND	N12		
GND	N13		
GND	N14		
GND	N15		
GND	N16		
GND	N26		
GND	P11		
GND	P12		
GND	P13		
GND	P14		
GND	P15		
GND	P23		

Table 3. Signals Listed Alphabetically (Sheet 5 of 13)

Signal Name	Ball	Interface Group	Page
GND	R12	Power	45
GND	R13		
GND	R14		
GND	R15		
GND	T11		
GND	T14		
GND	T16		
GND	U01		
GND	U02		
GND	V04		
GND	V23		
GND	W01		
GND	W26		
GND	AB01		
GND	AC04		
GND	AC09		
GND	AC13		
GND	AC18		
GND	AC23		
GND	AD03		
GND	AD24		
GND	AE02		
GND	AE25		
GND	AF01		
GND	AF08		
GND	AF14		
GND	AF19		
GND	AF26		

Table 3. Signals Listed Alphabetically (Sheet 6 of 13)

Signal Name	Ball	Interface Group	Page
GPIO00[PerDataPar0]	A16	System	41
GPIO01[PerDataPar1]	B12		
GPIO02[PerDataPar2]	C09		
GPIO03[PerDataPar3]	B04		
GPIO04[PerData20][USB2Data4]	C13		
GPIO05[PerData21][USB2Data5]	B09		
GPIO06[PerData22][USB2Data6]	C12		
GPIO07[PerData23][USB2Data7]	D11		
GPIO08[$\overline{\text{PerCS1}}$][$\overline{\text{NFCE1}}$][IRQ7]	C20		
GPIO09[$\overline{\text{PerCS2}}$][$\overline{\text{NFCE2}}$][IRQ8]	A21		
GPIO10[$\overline{\text{PerCS3}}$][$\overline{\text{NFCE3}}$][IRQ9]	B20		
GPIO11[IRQ6]	H03		
GPIO12[PerData16][USB2Data0]	C11		
GPIO13[PerData17][USB2Data1]	B08		
GPIO14[PerData18][USB2Data2]	A10		
GPIO15[PerData19][USB2Data3]	B10		
GPIO16[$\overline{\text{UART0DCD}}$][$\overline{\text{UART1CTS}}$]	F04		
GPIO17[$\overline{\text{UART0DSR}}$][$\overline{\text{UART1RTS}}$]	F02		
GPIO18[$\overline{\text{UART0CTS}}$]	G02		
GPIO19[$\overline{\text{UART0RTS}}$]	G01		
GPIO20[$\overline{\text{UART0DTR}}$][UART1Tx]	F03		
GPIO21[$\overline{\text{UART0RI}}$][UART1Rx]	F01		
GPIO22[HoldReq][DMAAck2]	B05		
GPIO23[HoldAck][DMAReq2]	C05		
GPIO24[$\overline{\text{ExtReq}}$][DMAEOT2][IRQ4]	A03		
GPIO25[$\overline{\text{ExtAck}}$][DMAAck3][IRQ3]	C04		
GPIO26[PerAddr05][DMAEOT0][TS3]	K26		
GPIO27[BusReq][DMAEOT3][IRQ5]	B03		
GPIO28	U03		
GPIO29[IRQ2][DMAEOT1]	D03		
GPIO30[IRQ1][DMAReq1]	D02		
GPIO31[IRQ0][DMAAck1]	D01		
$\overline{\text{Halt}}$	A02	System	41
[HoldAck]GPIO23[DMAReq2]	C05	External Bus Master	42
[HoldReq]GPIO22[DMAAck2]	B05		
IIC0SData	AA01	IIC	39
IIC0SClk	Y03		
IIC1SData[SCPDO]	AA04		
IIC1SClk[SCPClkOut]	AA02		

Table 3. Signals Listed Alphabetically (Sheet 7 of 13)

Signal Name	Ball	Interface Group	Page
[IRQ0]GPIO31[DMAAck1]	D01	Interrupts	40
[IRQ1]GPIO30[DMAReq1]	D02		
[IRQ2]GPIO29[DMAEOT1]	D03		
[IRQ3][$\overline{\text{ExtAck}}$]GPIO25[DMAAck3]	C04		
[IRQ4][$\overline{\text{ExtReq}}$]GPIO24[DMAEOT2]	A03		
[IRQ5][BusReq]GPIO27[DMAEOT3]	B03		
[IRQ6]GPIO11	H03		
[IRQ7][$\overline{\text{PerCS1}}$][$\overline{\text{NFCE1}}$]GPIO08	C20		
[IRQ8][$\overline{\text{PerCS2}}$][$\overline{\text{NFCE2}}$]GPIO09	A21		
[IRQ9][$\overline{\text{PerCS3}}$][$\overline{\text{NFCE3}}$]GPIO10	B20		
MemAddr00	AE21	DDR1/2 SDRAM	43
MemAddr01	AD20		
MemAddr02	AF22		
MemAddr03	AE22		
MemAddr04	AF23		
MemAddr05	AD21		
MemAddr06	AC21		
MemAddr07	AE23		
MemAddr08	AE26		
MemAddr09	AD25		
MemAddr10	AD26		
MemAddr11	AC24		
MemAddr12	AB24		
MemAddr13	AC25		
MemAddr14	AC26		
MemClkEn	Y24	DDR1/2 SDRAM	43
MemClkOut0	AA23		
$\overline{\text{MemClkOut0}}$	AA24		

Table 3. Signals Listed Alphabetically (Sheet 8 of 13)

Signal Name	Ball	Interface Group	Page
MemData00	M24	DDR1/2 SDRAM	43
MemData01	N24		
MemData02	P25		
MemData03	P24		
MemData04	L25		
MemData05	L26		
MemData06	N25		
MemData07	P26		
MemData08	R24		
MemData09	T24		
MemData10	V26		
MemData11	U24		
MemData12	R25		
MemData13	R26		
MemData14	U26		
MemData15	U25		
MemData16	AE17		
MemData17	AF17		
MemData18	AE15		
MemData19	AF15		
MemData20	AF18		
MemData21	AD17		
MemData22	AF16		
MemData23	AD15		
MemData24	AE13		
MemData25	AF12		
MemData26	AF10		
MemData27	AD11		
MemData28	AE14		
MemData29	AF13		
MemData30	AF11		
MemData31	AE11		
MemFBD	AD23	DDR1/2 SDRAM	43
MemFBR	AF25		
MemODT0	AD18		
MemODT1	AE18		

Table 3. Signals Listed Alphabetically (Sheet 9 of 13)

Signal Name	Ball	Interface Group	Page
[NFALE]PerData30	C06	NAND Flash	43
[$\overline{\text{NFCE0}}$]$\overline{\text{PerCS0}}$	B21		
[$\overline{\text{NFCE1}}$][$\overline{\text{PerCS1}}$]GPIO08[IRQ7]	C20		
[$\overline{\text{NFCE2}}$][$\overline{\text{PerCS2}}$]GPIO09[IRQ8]	A21		
[$\overline{\text{NFCE3}}$][$\overline{\text{PerCS3}}$]GPIO10[IRQ9]	B20		
[NFCLE]PerData29	A06		
[NFData00]PerData00	C18		
[NFData01]PerData01	B18		
[NFData02]PerData02	C17		
[NFData03]PerData03	A18		
[NFData04]PerData04	D16		
[NFData05]PerData05	B17		
[NFData06]PerData06	C16		
[NFData07]PerData07	B16		
[NFData08]PerData08	A17		
[NFData09]PerData09	B15		
[NFData10]PerData10	C15		
[NFData11]PerData11	A15		
[NFData12]PerData12	B14		
[NFData13]PerData13	A14		
[NFData14]PerData14	C14		
[NFData15]PerData15	B13		
[$\overline{\text{NFRdyBusy}}$]PerData31	A04		
[$\overline{\text{NFREn}}$]PerData27	A05		
[$\overline{\text{NFWEn}}$]PerData28	C08		
OV_{DD}	D05	Power	45
OV_{DD}	D07		
OV_{DD}	D08		
OV_{DD}	D13		
OV_{DD}	D19		
OV_{DD}	D20		
OV_{DD}	D22		
OV_{DD}	E04		
OV_{DD}	E23		
OV_{DD}	G04		
OV_{DD}	G23		
OV_{DD}	H23		
OV_{DD}	L12		
OV_{DD}	L15		
OV_{DD}	M11		
OV_{DD}	M16		
OV_{DD}	R11		
OV_{DD}	V03		
OV_{DD}	W04		
OV_{DD}	Y04		

Table 3. Signals Listed Alphabetically (Sheet 10 of 13)

Signal Name	Ball	Interface Group	Page
PCIE0ATB	L03	PCI Express 0	40
PCIE0ClkC	L01		
PCIE0ClkT	L02		
PCIE0RExt	M03		
PCIE0RExtG	M02		
$\overline{\text{PCIE0Rx}}$	J01		
PCIE0Rx	J02		
$\overline{\text{PCIE0Tx}}$	K02		
PCIE0Tx	K03		
PCIE1ATB	R02	PCI Express 1	40
PCIE1ClkC	T02		
PCIE1ClkT	R03		
PCIE1RExt	T03		
PCIE1RExtG	T04		
$\overline{\text{PCIE1Rx}}$	N01		
PCIE1Rx	N02		
PCIE1Tx	P02		
$\overline{\text{PCIE1Tx}}$	P03		
[PerAddr05]GPIO26[TS3][DMAEOT0]	K26	External Peripheral	42
PerAddr06[TS2][DMAReq0]	K25		
PerAddr07[TS1][DMAAck0]	J26		
PerAddr08[TS0][DMAReq3]	J25		
PerAddr09[TS1E]	H25		
PerAddr10[TS0E]	J24		
PerAddr11[TS1O]	G26		
PerAddr12[TS0O]	H24		
PerAddr13	G25		
PerAddr14	F26		
PerAddr15	E26		
PerAddr16	F25		
PerAddr17	G24		
PerAddr18	E25		
PerAddr19	D26		
PerAddr20	F24		
PerAddr21	C26		
PerAddr22	D25		
PerAddr23	F23		
PerAddr24	E24		
PerAddr25	C25		
PerAddr26	D24		
PerAddr27	B26		
PerAddr28	A25		
PerAddr29	B24		
PerAddr30	C23		
PerAddr31	C22		
$\overline{\text{PerBLast}}$	D21	External Peripheral	42
PerClk	A20		

Table 3. Signals Listed Alphabetically (Sheet 11 of 13)

Signal Name	Ball	Interface Group	Page
PerCS0[NFCE0]	B21	External Peripheral	42
[PerCS1][NFCE1]GPIO08[IRQ7]	C20		
[PerCS2][NFCE2]GPIO09[IRQ8]	A21		
[PerCS3][NFCE3]GPIO10[IRQ9]	B20		
PerData00[NFData00]	C18	External Peripheral	42
PerData01[NFData01]	B18		
PerData02[NFData02]	C17		
PerData03[NFData03]	A18		
PerData04[NFData04]	D16		
PerData05[NFData05]	B17		
PerData06[NFData06]	C16		
PerData07[NFData07]	B16		
PerData08[NFData08]	A17		
PerData09[NFData09]	B15		
PerData10[NFData10]	C15		
PerData11[NFData11]	A15		
PerData12[NFData12]	B14		
PerData13[NFData13]	A14		
PerData14[NFData14]	C14		
PerData15[NFData15]	B13		
[PerData16]GPIO12[USB2Data0]	C11		
[PerData17]GPIO13[USB2Data1]	B08		
[PerData18]GPIO14[USB2Data2]	A10		
[PerData19]GPIO15[USB2Data3]	B10		
[PerData20]GPIO04[USB2Data4]	C13		
[PerData21]GPIO05[USB2Data5]	B09		
[PerData22]GPIO06[USB2Data6]	C12		
[PerData23]GPIO07[USB2Data7]	D11		
PerData24[USB2Dir]	A07		
PerData25[USB2Stop]	B07		
PerData26[USB2Next]	B06		
PerData27[NFREn]	A05		
PerData28[NFWEn]	C08		
PerData29[NFCLE]	A06		
PerData30[NFALE]	C06		
PerData31[NFRdyBusy]	A04		
[PerDataPar0]GPIO00	A16	External Peripheral	42
[PerDataPar1]GPIO01	B12		
[PerDataPar2]GPIO02	C09		
[PerDataPar3]GPIO03	B04		
PerErr	C19	External Peripheral	42
PerOE	A24		
PerReady	B11		
PerRW	B23		
PerWBE0	A23	External Peripheral	42
PerWBE1	C21		
PerWBE2	B22		
PerWBE3	A22		

Table 3. Signals Listed Alphabetically (Sheet 12 of 13)

Signal Name	Ball	Interface Group	Page
PSROUser	A09	System	41
$\overline{RAS}$	AD19	DDR 1/2 SDRAM	43
Reserved	AD12	Other	45
SAGND	A11	Power	45
SAV_{DD}	A12		
[SCPClkOut]IIC1SClk	AA02	Serial Communication Port	44
SCPDI	AA03		
[SCPDO]IIC1SData	AA04		
SV_{DD}	N23	Power	45
SV_{DD}	R16		
SV_{DD}	T15		
SV_{DD}	W23		
SV_{DD}	Y23		
SV_{DD}	AB23		
SV_{DD}	AC19		
SV_{DD}	AC20		
SV_{DD}	AC22		
SV_{DD}	AD14		
S_{VREF}1A	AC14	DDR1/2 SDRAM	43
S_{VREF}1B	T23		
S_{VREF}2A	AC16		
S_{VREF}2B	L23		
SysClk	C10	System	41
SysErr	AD06		
$\overline{SysReset}$	AD08		
TCK	V02	JTAG	40
TDI	W02		
TDO	W03		
TestEn	Y02	System	41
TmrClk	D06		
TMS	V01	JTAG	40
TrcClk	L24	Trace	41
$\overline{TRST}$	Y01	JTAG	40
[TS0]PerAddr08[DMAReq3]	J25	Trace	41
[TS1]PerAddr07[DMAAck0]	J26		
[TS2]PerAddr06[DMAReq0]	K25		
[TS3][PerAddr05]GPIO26[DMAEOT0]	K26		
[TS0E]PerAddr10	J24	Trace	41
[TS0O]PerAddr12	H24		
[TS1E]PerAddr09	H25		
[TS1O]PerAddr11	G26		

Table 3. Signals Listed Alphabetically (Sheet 13 of 13)

Signal Name	Ball	Interface Group	Page
[UART0CTS]GPIO18	G02	UART Peripheral	44
[UART0DCD][UART1CTS]GPIO16	F04		
[UART0DSR][UART1RTS]GPIO17	F02		
[UART0DTR][UART1Tx]GPIO20	F03		
[UART0RI][UART1Rx]GPIO21	F01		
[UART0RTS]GPIO19	G01		
UART0Rx	G03		
UART0Tx	H02		
[UART1CTS][UART0DCD]GPIO16	F04	UART Peripheral	44
[UART1RTS][UART0DSR]GPIO17	F02		
[UART1Rx][UART0RI]GPIO21	F01		
[UART1Tx][UART0DTR]GPIO20	F03		
UARTSerClk	E02	UART Peripheral	44
USB2Clk	C07	USB 2.0	44
[USB2Data0][PerData16]GPIO12	C11	USB 2.0	44
[USB2Data1][PerData17]GPIO13	B08		
[USB2Data2][PerData18]GPIO14	A10		
[USB2Data3][PerData19]GPIO15	B10		
[USB2Data4][PerData20]GPIO04	C13		
[USB2Data5][PerData21]GPIO05	B09		
[USB2Data6][PerData22]GPIO06	C12		
[USB2Data7][PerData23]GPIO07	D11		
[USB2Dir]PerData24	A07	USB 2.0	44
[USB2Next]PerData26	B06		
[USB2Stop]PerData25	B07		
V_{DD}	D10	Power	45
V_{DD}	D15		
V_{DD}	D17		
V_{DD}	H04		
V_{DD}	K23		
V_{DD}	L14		
V_{DD}	M23		
V_{DD}	N11		
V_{DD}	P16		
V_{DD}	R23		
V_{DD}	T13		
V_{DD}	U04		
V_{DD}	U23		
V_{DD}	AC10		
V_{DD}	AC12		
V_{DD}	AC15		
V_{DD}	AC17		
$\overline{WE}$	AE19	DDR1/2 SDRAM	43

In the following table, only the default signal name is shown for each ball. Shared balls are marked with an asterisk (*). To determine what signals or functions are shared on those balls, look up the default signal name in “Signals Listed Alphabetically” on page 18. The following table lists the signals by ball assignment.

Table 4. Signals Listed by Ball Assignment (Sheet 1 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A01	GND	B01	GND	C01	GND	D01	GPIO31 *
A02	$\overline{\text{Halt}}$	B02	GND	C02	GND	D02	GPIO30 *
A03	GPIO24 *	B03	GPIO27 *	C03	GND	D03	GPIO29 *
A04	PerData31 *	B04	GPIO03 *	C04	GPIO25 *	D04	GND
A05	PerData27 *	B05	GPIO22 *	C05	GPIO23 *	D05	OV_{DD}
A06	PerData29 *	B06	PerData26 *	C06	PerData30 *	D06	TmrClk
A07	PerData24 *	B07	PerData25 *	C07	USB2Clk	D07	OV_{DD}
A08	GND	B08	GPIO13 *	C08	PerData28 *	D08	OV_{DD}
A09	PSROUser	B09	GPIO05 *	C09	GPIO02 *	D09	GND
A10	GPIO14 *	B10	GPIO15 *	C10	SysClk	D10	V_{DD}
A11	SAGND	B11	PerReady	C11	GPIO12 *	D11	GPIO07 *
A12	SAV_{DD}	B12	GPIO01 *	C12	GPIO06 *	D12	EOV_{DD}
A13	GND	B13	PerData15 *	C13	GPIO04 *	D13	OV_{DD}
A14	PerData13 *	B14	PerData12 *	C14	PerData14 *	D14	GND
A15	PerData11 *	B15	PerData09 *	C15	PerData10 *	D15	V_{DD}
A16	GPIO00 *	B16	PerData07 *	C16	PerData06 *	D16	PerData04 *
A17	PerData08 *	B17	PerData05 *	C17	PerData02 *	D17	V_{DD}
A18	PerData03 *	B18	PerData01 *	C18	PerData00 *	D18	GND
A19	GND	B19	$\overline{\text{ExtReset}}$	C19	PerErr	D19	OV_{DD}
A20	PerClk	B20	GPIO10 *	C20	GPIO08 *	D20	OV_{DD}
A21	GPIO09 *	B21	$\overline{\text{PerCS0}}$ *	C21	$\overline{\text{PerWBE1}}$	D21	$\overline{\text{PerBLast}}$
A22	$\overline{\text{PerWBE3}}$	B22	$\overline{\text{PerWBE2}}$	C22	PerAddr31	D22	OV_{DD}
A23	$\overline{\text{PerWBE0}}$	B23	$\text{PerR}\overline{\text{W}}$	C23	PerAddr30	D23	GND
A24	$\overline{\text{PerOE}}$	B24	PerAddr29	C24	GND	D24	PerAddr26
A25	PerAddr28	B25	GND	C25	PerAddr25	D25	PerAddr22
A26	GND	B26	PerAddr27	C26	PerAddr21	D26	PerAddr19

Table 4. Signals Listed by Ball Assignment (Sheet 2 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
E01	GND	F01	GPIO21 *	G01	GPIO19 *	H01	GND
E02	UARTSerClk	F02	GPIO17 *	G02	GPIO18 *	H02	UART0Tx *
E03	GND	F03	GPIO20 *	G03	UART0Rx *	H03	GPIO11 *
E04	OV_{DD}	F04	GPIO16 *	G04	OV_{DD}	H04	V_{DD}
E05	No ball	F05	No ball	G05	No ball	H05	No ball
E06	No ball	F06	No ball	G06	No ball	H06	No ball
E07	No ball	F07	No ball	G07	No ball	H07	No ball
E08	No ball	F08	No ball	G08	No ball	H08	No ball
E09	No ball	F09	No ball	G09	No ball	H09	No ball
E10	No ball	F10	No ball	G10	No ball	H10	No ball
E11	No ball	F11	No ball	G11	No ball	H11	No ball
E12	No ball	F12	No ball	G12	No ball	H12	No ball
E13	No ball	F13	No ball	G13	No ball	H13	No ball
E14	No ball	F14	No ball	G14	No ball	H14	No ball
E15	No ball	F15	No ball	G15	No ball	H15	No ball
E16	No ball	F16	No ball	G16	No ball	H16	No ball
E17	No ball	F17	No ball	G17	No ball	H17	No ball
E18	No ball	F18	No ball	G18	No ball	H18	No ball
E19	No ball	F19	No ball	G19	No ball	H19	No ball
E20	No ball	F20	No ball	G20	No ball	H20	No ball
E21	No ball	F21	No ball	G21	No ball	H21	No ball
E22	No ball	F22	No ball	G22	No ball	H22	No ball
E23	OV_{DD}	F23	PerAddr23	G23	OV_{DD}	H23	OV_{DD}
E24	PerAddr24	F24	PerAddr20	G24	PerAddr17	H24	PerAddr12 *
E25	PerAddr18	F25	PerAddr16	G25	PerAddr13	H25	PerAddr09 *
E26	PerAddr15	F26	PerAddr14	G26	PerAddr11 *	H26	GND

Table 4. Signals Listed by Ball Assignment (Sheet 3 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
J01	$\overline{\text{PCIE0Rx}}$	K01	AGND	L01	PCIE0ClkC	M01	AV_{DD}
J02	PCIE0Rx	K02	$\overline{\text{PCIE0Tx}}$	L02	PCIE0ClkT	M02	PCIE0RExtG
J03	AV_{DD}	K03	PCIE0Tx	L03	PCIE0ATB	M03	PCIE0RExt
J04	GND	K04	AV_{DD}	L04	AGND	M04	AHV_{DD}
J05	No ball	K05	No ball	L05	No ball	M05	No ball
J06	No ball	K06	No ball	L06	No ball	M06	No ball
J07	No ball	K07	No ball	L07	No ball	M07	No ball
J08	No ball	K08	No ball	L08	No ball	M08	No ball
J09	No ball	K09	No ball	L09	No ball	M09	No ball
J10	No ball	K10	No ball	L10	No ball	M10	No ball
J11	No ball	K11	No ball	L11	GND	M11	OV_{DD}
J12	No ball	K12	No ball	L12	OV_{DD}	M12	GND
J13	No ball	K13	No ball	L13	GND	M13	GND
J14	No ball	K14	No ball	L14	V_{DD}	M14	GND
J15	No ball	K15	No ball	L15	OV_{DD}	M15	GND
J16	No ball	K16	No ball	L16	GND	M16	OV_{DD}
J17	No ball	K17	No ball	L17	No ball	M17	No ball
J18	No ball	K18	No ball	L18	No ball	M18	No ball
J19	No ball	K19	No ball	L19	No ball	M19	No ball
J20	No ball	K20	No ball	L20	No ball	M20	No ball
J21	No ball	K21	No ball	L21	No ball	M21	No ball
J22	No ball	K22	No ball	L22	No ball	M22	No ball
J23	GND	K23	V_{DD}	L23	$S_{VREF}2B$	M23	V_{DD}
J24	PerAddr10 *	K24	GND	L24	TrcClk	M24	MemData00
J25	PerAddr08 *	K25	PerAddr06 *	L25	MemData04	M25	DM0
J26	PerAddr07 *	K26	GPIO26 *	L26	MemData05	M26	DQS0

Table 4. Signals Listed by Ball Assignment (Sheet 4 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
N01	$\overline{\text{PCIE1Rx}}$	P01	AV_{DD}	R01	AGND	T01	AV_{DD}
N02	PCIE1Rx	P02	PCIE1Tx	R02	PCIE1ATB	T02	PCIE1ClkC
N03	AV_{DD}	P03	$\overline{\text{PCIE1Tx}}$	R03	PCIE1ClkT	T03	PCIE1RExt
N04	AV_{DD}	P04	AGND	R04	AHV_{DD}	T04	PCIE1RExtG
N05	No ball	P05	No ball	R05	No ball	T05	No ball
N06	No ball	P06	No ball	R06	No ball	T06	No ball
N07	No ball	P07	No ball	R07	No ball	T07	No ball
N08	No ball	P08	No ball	R08	No ball	T08	No ball
N09	No ball	P09	No ball	R09	No ball	T09	No ball
N10	No ball	P10	No ball	R10	No ball	T10	No ball
N11	V_{DD}	P11	GND	R11	OV_{DD}	T11	GND
N12	GND	P12	GND	R12	GND	T12	EOV_{DD}
N13	GND	P13	GND	R13	GND	T13	V_{DD}
N14	GND	P14	GND	R14	GND	T14	GND
N15	GND	P15	GND	R15	GND	T15	SV_{DD}
N16	GND	P16	V_{DD}	R16	SV_{DD}	T16	GND
N17	No ball	P17	No ball	R17	No ball	T17	No ball
N18	No ball	P18	No ball	R18	No ball	T18	No ball
N19	No ball	P19	No ball	R19	No ball	T19	No ball
N20	No ball	P20	No ball	R20	No ball	T20	No ball
N21	No ball	P21	No ball	R21	No ball	T21	No ball
N22	No ball	P22	No ball	R22	No ball	T22	No ball
N23	SV_{DD}	P23	GND	R23	V_{DD}	T23	S_{VREF}1B
N24	MemData01	P24	MemData03	R24	MemData08	T24	MemData09
N25	MemData06	P25	MemData02	R25	MemData12	T25	DQS1
N26	GND	P26	MemData07	R26	MemData13	T26	DM1

Table 4. Signals Listed by Ball Assignment (Sheet 5 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
U01	GND	V01	TMS	W01	GND	Y01	$\overline{TRST}$
U02	GND	V02	TCK	W02	TDI	Y02	TestEn
U03	GPIO28	V03	OV_{DD}	W03	TDO	Y03	IIC0SClk
U04	V_{DD}	V04	GND	W04	OV_{DD}	Y04	OV_{DD}
U05	No ball	V05	No ball	W05	No ball	Y05	No ball
U06	No ball	V06	No ball	W06	No ball	Y06	No ball
U07	No ball	V07	No ball	W07	No ball	Y07	No ball
U08	No ball	V08	No ball	W08	No ball	Y08	No ball
U09	No ball	V09	No ball	W09	No ball	Y09	No ball
U10	No ball	V10	No ball	W10	No ball	Y10	No ball
U11	No ball	V11	No ball	W11	No ball	Y11	No ball
U12	No ball	V12	No ball	W12	No ball	Y12	No ball
U13	No ball	V13	No ball	W13	No ball	Y13	No ball
U14	No ball	V14	No ball	W14	No ball	Y14	No ball
U15	No ball	V15	No ball	W15	No ball	Y15	No ball
U16	No ball	V16	No ball	W16	No ball	Y16	No ball
U17	No ball	V17	No ball	W17	No ball	Y17	No ball
U18	No ball	V18	No ball	W18	No ball	Y18	No ball
U19	No ball	V19	No ball	W19	No ball	Y19	No ball
U20	No ball	V20	No ball	W20	No ball	Y20	No ball
U21	No ball	V21	No ball	W21	No ball	Y21	No ball
U22	No ball	V22	No ball	W22	No ball	Y22	No ball
U23	V_{DD}	V23	GND	W23	SV_{DD}	Y23	SV_{DD}
U24	MemData11	V24	ECC0	W24	ECC1	Y24	MemClkEn
U25	MemData15	V25	ECC4	W25	ECC5	Y25	DQS4
U26	MemData14	V26	MemData10	W26	GND	Y26	DM4

Table 4. Signals Listed by Ball Assignment (Sheet 6 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AA01	IIC0SData	AB01	GND	AC01	GMCTxD5 *	AD01	GMCTxD2 *
AA02	IIC1SClk *	AB02	GMCTxD7 *	AC02	GMCTxD4 *	AD02	GMCTxD1 *
AA03	SCPDI	AB03	GMCTxD6 *	AC03	GMCTxD3 *	AD03	GND
AA04	IIC1SData *	AB04	EOV_{DD}	AC04	GND	AD04	GMCCD *
AA05	No ball	AB05	No ball	AC05	EOV_{DD}	AD05	GMCTxEn *
AA06	No ball	AB06	No ball	AC06	GMCTxClk	AD06	SysErr
AA07	No ball	AB07	No ball	AC07	EOV_{DD}	AD07	GMCRefClk
AA08	No ball	AB08	No ball	AC08	EOV_{DD}	AD08	$\overline{\text{SysReset}}$
AA09	No ball	AB09	No ball	AC09	GND	AD09	GMCRxClk *
AA10	No ball	AB10	No ball	AC10	V_{DD}	AD10	GMCRxD2 *
AA11	No ball	AB11	No ball	AC11	GMCRxD0 *	AD11	MemData27
AA12	No ball	AB12	No ball	AC12	V_{DD}	AD12	Reserved
AA13	No ball	AB13	No ball	AC13	GND	AD13	DM3
AA14	No ball	AB14	No ball	AC14	$S_{VREF}1A$	AD14	SV_{DD}
AA15	No ball	AB15	No ball	AC15	V_{DD}	AD15	MemData23
AA16	No ball	AB16	No ball	AC16	$S_{VREF}2A$	AD16	DM2
AA17	No ball	AB17	No ball	AC17	V_{DD}	AD17	MemData21
AA18	No ball	AB18	No ball	AC18	GND	AD18	MemODT0
AA19	No ball	AB19	No ball	AC19	SV_{DD}	AD19	$\overline{\text{RAS}}$
AA20	No ball	AB20	No ball	AC20	SV_{DD}	AD20	MemAddr01
AA21	No ball	AB21	No ball	AC21	MemAddr06	AD21	MemAddr05
AA22	No ball	AB22	No ball	AC22	SV_{DD}	AD22	BA0
AA23	MemClkOut0	AB23	SV_{DD}	AC23	GND	AD23	MemFBD
AA24	$\overline{\text{MemClkOut0}}$	AB24	MemAddr12	AC24	MemAddr11	AD24	GND
AA25	ECC7	AB25	ECC3	AC25	MemAddr13	AD25	MemAddr09
AA26	ECC6	AB26	ECC2	AC26	MemAddr14	AD26	MemAddr10

Table 4. Signals Listed by Ball Assignment (Sheet 7 of 7)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AE01	GMCTxD0 *	AF01	GND				
AE02	GND	AF02	GMCMDIO				
AE03	GMCMDClk	AF03	GMCTxEr *				
AE04	GMCGTxClk *	AF04	GMCCrS *				
AE05	GMCRxDV *	AF05	GMCRxEr *				
AE06	GMCRxD7 *	AF06	GMCRxD6 *				
AE07	EAGND	AF07	GMCRxD5 *				
AE08	EAV_{DD}	AF08	GND				
AE09	GMCRxD4 *	AF09	GMCRxD3 *				
AE10	GMCRxD1 *	AF10	MemData26				
AE11	MemData31	AF11	MemData30				
AE12	DQS3	AF12	MemData25				
AE13	MemData24	AF13	MemData29				
AE14	MemData28	AF14	GND				
AE15	MemData18	AF15	MemData19				
AE16	DQS2	AF16	MemData22				
AE17	MemData16	AF17	MemData17				
AE18	MemODT1	AF18	MemData20				
AE19	$\overline{WE}$	AF19	GND				
AE20	$\overline{BankSel1}$	AF20	$\overline{CAS}$				
AE21	MemAddr00	AF21	$\overline{BankSel0}$				
AE22	MemAddr03	AF22	MemAddr02				
AE23	MemAddr07	AF23	MemAddr04				
AE24	BA2	AF24	BA1				
AE25	GND	AF25	MemFBR				
AE26	MemAddr08	AF26	GND				

Pin Group List

The following table provides a summary of the number of package pins (balls) associated with each functional interface group.

Table 5. Pin Groups

Group	No. of Pins
Total Signal Pins	**246**
V_{DD}	17
OV_{DD}	20
EOV_{DD}	6
SV_{DD}	10
GND	71
AV_{DD}	7
AHV_{DD}	2
SAV_{DD}	1
SAGND	1
EAV_{DD}	1
EAGND	1
AGND	4
Total Power Pins	**141**
Reserved	1
Total Pins	**388**

In the table “Signal Functional Description” on page 39, each external signal is listed along with a short description of the signal function. Active-low signals (for example, Halt) are marked with an overline. See the preceding table, “Signals Listed Alphabetically” on page 18, for the pin (ball) number to which each signal is assigned.

Shared Pins

Some signals are shared on the same package pin so that the pin can be used for different functions. In most cases, the signal names shown in this table are not accompanied by signal names that might share the same pin. If you need to know what, if any, signals are shared with a particular signal, look up the name in “Signals Listed Alphabetically” on page 18. It is expected that in any single application a particular pin will always be programmed to serve the same function. The flexibility of sharing allows a single chip to offer a richer pin selection than would otherwise be possible.

Initialization Strapping

One group of pins is used as strapped inputs during system reset. These pins function as strapped inputs only during reset and are used for other functions during normal operation (see “Initialization” on page 69). Note that the use of these pins for strapping is not considered multiplexing since the strapping function is not programmable.

Pull-Up and Pull-Down Resistors

Pull-up and pull-down resistors are used for strapping during reset and to retain unused or undriven inputs in an appropriate state. The recommended pull-up value of 3kΩ to +3.3V and pull-down value of 1kΩ to GND, applies only to individually terminated signals. To prevent possible damage to the device, I/Os capable of becoming outputs *must never* be tied together and terminated through a common resistor.

If your system-level test methodology permits, input-only signals can be connected together and terminated through either a common resistor or directly to +3.3V or GND. When a resistor is used, its value must ensure that the grouped I/Os reach a valid logical zero or logical one state when accounting for the total input current into the PPC405EX.

Signal Functional Descriptions

The following table provides a description of the I/O signals on the PPC405EX.

Table 6. Signal Functional Description (Sheet 1 of 7)

Notes:
1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 38 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 38 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.

Signal Name	Description	I/O	Type	Notes
Ethernet Interface				
GMCCD, GMC1RxClk	GMII: Collision detect. RGMII 1: Receive clock.	I	3.3V tolerant 2.5V CMOS	1, 5
GMCCrS, GMC1TxClk	GMII: Carrier sense. RGMII 1: Transmit clock.	I/O	3.3V tolerant 2.5V CMOS	1
GMCGTxClk, GMC0TxClk	GMII: Transmit clock for GMII 1000Mbps. RGMII 0: Transmit clock.	O	3.3V tolerant 2.5V CMOS	
GMCMDClk	Management data clock.	O	3.3V tolerant 2.5V CMOS	
GMCMDIO	Management data I/O.	I/O	3.3V tolerant 2.5V CMOS	
GMCRefClk	GMII, RGMII: Reference clock for 1000Mbps.	I	3.3V tolerant 2.5V CMOS receiver	1, 5
GMCRxClk, GMC0RxClk	GMII: Receive clock. RGMII 0: Receive clock.	I	3.3V tolerant 2.5V CMOS	1, 5
GMCRxD0:3, GMC0RxD0:3	GMII: Receive data. RGMII 0: Receive data.	I	3.3V tolerant 2.5V CMOS	1
GMCRxD4:7, GMC1RxD0:3	GMII: Receive data. RGMII 1: Receive data.	I	3.3V tolerant 2.5V CMOS	1
GMCRxDV, GMC0RxCtl	GMII: Receive data valid. RGMII 0: Receive control.	I	3.3V tolerant 2.5V CMOS	1
GMCRxEr, GMC1RxCtl	GMII: Receive error. RGMII 1: Receive control.	I	3.3V tolerant 2.5V CMOS	1
GMCTxClk	GMII: Transmit clock for 10/100Mbps.	I	3.3V tolerant 2.5V CMOS	1, 5
GMCTxD0:3, GMC0TxD0:3	GMII: Transmit data. RGMII 0: Transmit data.	O	3.3V tolerant 2.5V CMOS	
GMCTxD4:7, GMC1TxD0:3	GMII: Transmit data. RGMII 1: Transmit data.	O	3.3V tolerant 2.5V CMOS	
GMCTxEn, GMC0TxCtl	GMII: Transmit enable. RGMII 0: Transmit control.	O	3.3V tolerant 2.5V CMOS	
GMCTxEr, GMC1TxCtl	GMII: Transmit error. RGMII 1: Transmit control.	O	3.3V tolerant 2.5V CMOS	
IIC Interface				
IIC0SClk	IIC Serial Clock.	I/O	3.3V LVTTL	1, 2
IIC0SData	IIC Serial Data.	I/O	3.3V LVTTL	2
IIC1SClk	IIC Serial Clock.	I/O	3.3V LVTTL	1
IIC1SData	IIC Serial Data.	I/O	3.3V LVTTL	1

Table 6. Signal Functional Description (Sheet 2 of 7)

Notes:
1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 38 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 38 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.

Signal Name	Description	I/O	Type	Notes
PCI Express Interface (n = 0 and 1)				
PCIEnATB	Analog Test Bus for manufacturing test.	O	CML	
PCIEnClkC PCIEnClkT	Differential input for external reference clock.	I	CML	5
PCIEnRExt PCIEnRExtG	External reference resistor. Attach a 1.37 kΩ , 1% resistor between RExt and RExtG to provide the reference for both the bias currents and the impedance calibration circuitry.	I/O	CML	
$\overline{\text{PCIEnRx}}$ PCIEnRx	Differential receiver for received serial data.	I	LVDS receiver	
$\overline{\text{PCIEnTx}}$ PCIEnTx	Differential driver for transmitted serial data.	O	LVDS driver	
Interrupts Interface				
IRQ0:2	External interrupt requests.	I	3.3V LVTTL	
IRQ3:5	External interrupt requests.	I	3.3V LVTTL	1
IRQ6	External interrupt requests.	I	3.3V LVTTL	
IRQ7:9	External interrupt requests.	I	3.3V LVTTL	1
JTAG Interface				
TCK	Test clock.	I	3.3V LVTTL	1
TDI	Test data in.	I	3.3V LVTTL w/pull-up	1, 4
TDO	Test data out.	O	3.3V LVTTL	
TMS	Test mode select.	I	3.3V LVTTL w/pull-up	1
$\overline{\text{TRST}}$	Test reset. Must be low at power-on to initialize the JTAG controller and for normal operation of the PPC405EX.	I	3.3V LVTTL w/pull-up	1, 5

Table 6. Signal Functional Description (Sheet 3 of 7)

Notes:
1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 38 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 38 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.

Signal Name	Description	I/O	Type	Notes
System Interface				
SysClk	System input clock.	I	3.3V tolerant 2.5V CMOS receiver	1
SysErr	Machine check exception has occurred.	O	3.3V tolerant 2.5V CMOS	
$\overline{\text{SysReset}}$	Main system reset. This signal may be driven by the PPC405EX to cause a board level reset to occur.	I/O	3.3V tolerant 2.5V CMOS	1, 2
TestEn	Test enable. Reserved for manufacturing LSSD test.	I	3.3V LVTTL receiver w/pull-down	3
$\overline{\text{Halt}}$	External request to stop the processor.	I	3.3V LVTTL receiver w/pull-up	
TmrClk	Processor timer external input.	I	3.3V LVTTL receiver w/pull-up	
GPIO00:27 GPIO29:31	General purpose I/O. Most of the GPIO signals are multiplexed with other signals. Which signal is connected to the external pin depends on the setting of bits in the GPIO registers.	I/O	3.3V LVTTL	
GPIO28	General purpose I/O. Most of the GPIO signals are multiplexed with other signals. Which signal is connected to the external pin depends on the setting of bits in the GPIO registers.	I/O	3.3V tolerant 2.5V CMOS	
PSROUser	Performance screen ring output. Use for module characterization and screening only.	O		3
Trace Interface				
TrcClk	Trace interface clock. Operates at half the CPU core frequency.	O	3.3V LVTTL	
TS0E TS1E	Even trace execution status.	I/O	3.3V LVTTL	
TS0O TS1O	Odd trace execution status.	I/O	3.3V LVTTL	
TS0:3	Trace status.	I/O	3.3V LVTTL	

Table 6. Signal Functional Description (Sheet 4 of 7)

Notes:
1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 38 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 38 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.

Signal Name	Description	I/O	Type	Notes
External Peripheral Interface				
PerAddr05:31	Address bus 5:31.	I/O	3.3V LVTTL	
PerClk	Clock output.	O	3.3V LVTTL	
$\overline{\text{PerCS0}}$	Chip selects 0.	O	3.3V LVTTL	2
$\overline{\text{PerCS1:3}}$	Chip selects 1:3.	I/O	3.3V LVTTL	1, 2
PerData00:31	Data bus 0:31.	I/O	3.3V LVTTL	
PerDataPar0:3	Data bus parity 0:3.	I/O	3.3V LVTTL	
$\overline{\text{PerOE}}$	Output enable.	O	3.3V LVTTL	2
PerReady	Slave is ready to transfer data.	I	3.3V LVTTL receiver	
$\overline{\text{PerBLast}}$	Last transfer of burst access.	I/O	3.3V LVTTL	1, 4
PerErr	External bus error.	I/O	3.3V LVTTL	1, 3
PerR$\overline{\text{W}}$	Read/Write.	I/O	3.3V LVTTL	1, 2
$\overline{\text{PerWBE0:3}}$	Write Byte enable 0:3.	I/O	3.3V LVTTL	1, 2
$\overline{\text{ExtReset}}$	External reset.	O	3.3V LVTTL	
External Bus Master Interface				
BusReq	External bus request.	O	3.3V LVTTL	1
$\overline{\text{ExtAck}}$	External data transfer complete.	O	3.3V LVTTL	1
$\overline{\text{ExtReq}}$	External data transfer request.	I	3.3V LVTTL	1
HoldReq	External request for bus access.	I	3.3V LVTTL	1
HoldAck	External request acknowledge.	O	3.3V LVTTL	1
DMA Interface				
DMAAck0:1	External peripheral DMA acknowledge.	O	3.3V LVTTL	
DMAAck2:3	External peripheral DMA acknowledge.	O	3.3V LVTTL	1
DMAReq0:1	External peripheral DMA request.	I	3.3V LVTTL	
DMAReq2	External peripheral DMA request.	I	3.3V LVTTL	1
DMAReq3	External peripheral DMA request.	I	3.3V LVTTL	
DMAEOT0:1	External DMA peripheral end-of-transmission.	I/O	3.3V LVTTL	
DMAEOT2:3	External DMA peripheral end-of-transmission.	I/O	3.3V LVTTL	1

Table 6. Signal Functional Description (Sheet 5 of 7)

Notes:
1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 38 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 38 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.

Signal Name	Description	I/O	Type	Notes
NAND Flash Interface				
NFALE	Address latch enable.	O	3.3V LVTTL	
$\overline{\text{NFCE0}}$	Chip select 0.	O	3.3V LVTTL	
$\overline{\text{NFCE1:3}}$	Chip selects 1:3.	O	3.3V LVTTL	1
NFCLE	Command latch enable.	O	3.3V LVTTL	
NFData00:15	Data Bus	I/O	3.3V LVTTL	
$\overline{\text{NFRdyBusy}}$	Read/Busy. If low, indicates that Read/Erase command is in process. If high, indicates that the command is complete.	I	3.3V LVTTL	
$\overline{\text{NFRE}}$	Read enable.	O	3.3V LVTTL	
$\overline{\text{NFWE}}$	Write enable.	O	3.3V LVTTL	
DDR1/2 SDRAM Interface				
MemData00:31	Memory data.	I/O	2.5V (1.8V) SSTL2 Dr/Rcv	
MemAddr00:14	Memory address.	O	2.5V (1.8V) SSTL2 Dr/Rcv	
$\overline{\text{RAS}}$	Row address strobe.	O	2.5V (1.8V) SSTL2 Dr/Rcv	
$\overline{\text{CAS}}$	Column address strobe.	O	2.5V (1.8V) SSTL2 Dr/Rcv	
MemClkEn	Clock enable.	O	2.5V (1.8V) SSTL2 Dr/Rcv	
MemClkOut0 $\overline{\text{MemClkOut0}}$	Differential DDR SDRAM clock output.	O	2.5V (1.8V) SSTL2 Dr/Rcv	
MemFBD	Feedback driver.	O	2.5V (1.8V) SSTL2 Dr/Rcv	
MemFBR	Feedback receiver. Connect externally to MemFBD.	I	2.5V (1.8V) SSTL2 Dr/Rcv	
MemODT0:1	On-die termination.	O	2.5V (1.8V) SSTL2 Dr/Rcv	
DM0:4	Write data byte lane mask. DM4 is the byte lane mask for the ECC byte lane.	O	2.5V (1.8V) SSTL2 Dr/Rcv	
DQS0:4	Byte lane strobe. DQS4 is the strobe for the ECC lane.	I/O	2.5V (1.8V) SSTL2 Dr/Rcv	
BA0:2	Bank address for up to eight banks.	O	2.5V (1.8V) SSTL2 Dr/Rcv	
$\overline{\text{BankSel0:1}}$	Bank select for up to two SDRAM memory banks.	O	2.5V (1.8V) SSTL2 Dr/Rcv	
ECC0:7	ECC check bit byte.	I/O	2.5V (1.8V) SSTL2 Dr/Rcv	
$\overline{\text{WE}}$	Write enable.	O	2.5V (1.8V) SSTL2 Dr/Rcv	

Table 6. Signal Functional Description (Sheet 6 of 7)

Notes:
1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 38 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 38 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.

Signal Name	Description	I/O	Type	Notes
S_{VREF}1A:B S_{VREF}2A:B	DDR 1 (DDR2) Reference voltage 1 and 2 inputs: Minimum +1.15 (+0.825)V Nomimal +1.25 (+0.9)V Maximum +1.35 (0.975)V	I	1.25V (0.9V) Volt ref receiver	
Serial Communication Port (SCP) Interface				
SCPClkOut	Output clock.	I/O	3.3V LVTTL	
SCPDI	Data input.	I	3.3V LVTTL	
SCPDO	Data output.	O	3.3V LVTTL	
UART Peripheral Interface The UART interface can be configured as follows: 1. One 8-pin 2. Two 4-pin 3. Two 2-pin (pull up DCD, DSR, CTS and RTS) 4. One 4-pin and one 2-pin				
UARTSerClk	Serial clock input.	I	3.3V LVTTL receiver w/pull-up	
$\overline{\text{UARTnCTS}}$	Clear to send.	I	3.3V LVTTL	1, 6
$\overline{\text{UARTnDCD}}$	Data carrier detect.	I	3.3V LVTTL	1, 6
$\overline{\text{UARTnDSR}}$	Data set ready.	I	3.3V LVTTL	1, 6
$\overline{\text{UARTnDTR}}$	Data terminal ready.	O	3.3V LVTTL	1
$\overline{\text{UARTnRI}}$	Ring indicator.	I	3.3V LVTTL	1
$\overline{\text{UARTnRTS}}$	Request to send.	O	3.3V LVTTL	1
UARTnRx	Receive data.	I	3.3V LVTTL receiver w/pull-down	
UARTnTx	Transmit data.	O	3.3V LVTTL	
USB 2.0 Interface				
USB2Clk	USB clock.	I	3.3V LVTTL receiver	5
USB2Data0:7	Parallel data bus.	I/O	3.3V LVTTL	
USB2Dir	Data bus direction control.	I	3.3V LVTTL	
USB2Next	Next data byte control. When data is being transferred to the PHY, the next byte should be sent. When data is being received from the PHY, the next byte is available.	I	3.3V LVTTL	
USB2Stop	Stop output control.	O	3.3V LVTTL	

Table 6. Signal Functional Description (Sheet 7 of 7)

Notes:
1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 38 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 38 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.

Signal Name	Description	I/O	Type	Notes
Power				
V_{DD}	Logic supply (+1.2V).	na	na	na
OV_{DD}	I/O supply (+3.3V).	na	na	na
SV_{DD}	DDR1/2 SDRAM supply (+2.5V or +1.8V)	na	na	na
EOV_{DD}	CMOS supply (+2.5V)	na	na	na
GND	System ground.	na	na	na
AV_{DD}	Logic Analog supply (+1.2V)	na	na	na
SAV_{DD}	System analog supply (+2.5V).	na	na	na
SAGND	System analog ground.	na	na	na
EAV_{DD}	Ethernet analog supply (+2.5V).	na	na	na
EAGND	Ethernet analog ground.	na	na	na
AHV_{DD}	SerDes analog supply (+2.5V).	na	na	na
AGND	Analog ground.	na	na	na
Other				
Reserved	Do not connect voltages, grounds, or signals to these pins.	na	na	na

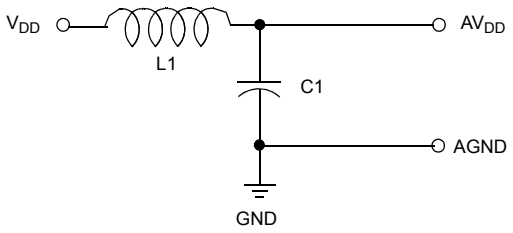
Ratings and Specifications

Table 7. Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. *Operation at or beyond these maximum ratings can cause permanent damage to the device. None of the performance specification contained in this document are guaranteed when operating at these maximum ratings.*

Characteristic	Symbol	Value	Unit	Notes
Supply Voltage (Internal Logic)	V_{DD}	0 to +1.6	V	
Core SerDes Analog Supply Voltage	AV_{DD}	0 to +1.6	V	1
PLL SerDes Analog Supply Voltage	AHV_{DD}	0 to +2.6	V	1
I/O Supply Voltage	OV_{DD}	0 to +3.6	V	
SDRAM DDR1(2) Supply Voltage	SV_{DD}	0 to +2.6 (+1.9)	V	
CMOS Supply Voltage	EOV_{DD}	0 to +2.6	V	
System PLL Analog Supply Voltage	SAV_{DD}	0 to +2.6	V	1
Ethernet PLL Analog Supply Voltage	EAV_{DD}	0 to +2.6	V	1
Input Voltage (3.3V LVTTL receivers)	V_{IN}	0 to +3.6	V	
Storage Temperature Range	T_{STG}	−55 to +150	°C	
Case Temperature Range under bias	T_C	−40 to +120	°C	
Junction Temperature Range	T_{JMax}	−40 to +125	°C	

1. The analog voltages can be derived from the +1.2V and +2.5V supplies, but must be filtered as shown below before entering the PPC405EX. Use a separate filter for each voltage. This circuit can be used for AV_{DD}, AHV_{DD} , SAV_{DD}, and EAV_{DD}. Use AGND with AV_{DD} and $AHV_{DD.}$ Use SAGND with SAV_{DD}. Use EAGND with EAV_{DD}. These analog grounds must be brought out and connected to the digital ground plane at the filter capacitor. Keep all wire lengths as short as possible.



L1 – Murata BLM18AG121SN1D

C1 – 0.1 µF ceramic

Thermal Management

Table 8. Package Thermal Specifications

The PPC405EX is designed to operate within a case temperature range T_C defined in "Recommended DC Operating Conditions" on page 48. Thermal resistance values for the EPBGA packages in a convection environment are as follows:

Parameter	Symbol	Airflow ft/min (m/sec)							Unit
		0 (0)	100 (0.51)	200 (1.02)	300 (1.52)	400 (2.02)	500 (2.53)	600 (3.03)	
Junction-to-ambient thermal resistance *without* heat sink	θ_{JA}	18.9	16.6	15.8	15.4	15.0	14.7	14.4	°C/W
Junction-to-ambient thermal resistance *with* heat sink	θ_{JA}	15.5	12.5	11.4	10.9	10.7	10.5	10.3	°C/W
		Resistance Value							
Junction-to-case thermal resistance	θ_{JC}	8.96							°C/W
Junction-to-board thermal resistance	θ_{JB}	13.74							°C/W

Notes:

1. Values in the table are achieved with the following JEDEC standard board: 114.5mm x 101.6mm x 1.6mm, 4 layers.
2. For a chip mounted on a card with at least one signal and two power planes, the following relationships exist:
   a. Case temperature, T_C, is measured at top center of case surface with device soldered to circuit board.
   b. $T_A = T_C - P x \theta_{CA}$, where T_A is ambient temperature and P is power consumption.
   c. $T_{CMax} = T_{JMax} - P x \theta_{JC}$, where T_{JMax} is maximum junction temperature and P is power consumption.

The following heat sink was used in the above thermal analysis:

26.92mm x 27mm x 11.43mm

The heat sink is manufactured by:

Aavid Thermalloy, P/N 62925

Table 9. Recommended DC Operating Conditions (Sheet 1 of 2)

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Logic Supply Voltage	V_{DD}	+1.1	+1.2	+1.3	V	
I/O Supply Voltage	OV_{DD}	+3.15	+3.3	+3.45	V	
SDRAM DDR1(2) Supply Voltage	SV_{DD}	+2.4 (+1.7)	+2.5 (+1.8)	+2.6 (+1.9)	V	
CMOS Supply Voltage	EOV_{DD}	+2.4	+2.5	+2.6	V	
PLL Analog Supply Voltage	AHV_{DD} SAV_{DD} EAV_{DD}	+2.4	+2.5	+2.6	V	
Analog Supply Voltage	AV_{DD}	+1.1	+1.2	+1.3	V	
I/O Input Low (3.3V LVTTL)	V_{IL}	0		+0.8	V	
I/O Input High (3.3V LVTTL)	V_{IH}	+2.0		+3.6	V	
I/O Output Low (3.3V LVTTL)	V_{OL}	0		+0.4	V	
I/O Output High (3.3V LVTTL)	V_{OH}	+2.4		+3.6	V	
I/O Input Low (3.3V tol, 2.5V CMOS)	V_{IL}	0		+0.7	V	
I/O Input High (3.3V tol, 2.5V CMOS)	V_{IH}	+1.7		+3.6	V	
I/O Output Low (3.3V tol, 2.5V CMOS)	V_{OL}	0		+0.4	V	
I/O Output High (3.3V tol, 2.5V CMOS)	V_{OH}	+2.0		+2.7	V	
I/O Input Low DDR1 (DDR2) (SSTL2)	V_{IL}	– 0.3		S_{VREF} – 0.18 (0.125)	V	
I/O Input High DDR1 (DDR2) (SSTL2)	V_{IH}	S_{VREF} + 0.18 (0.125)		SV_{DD} + 0.3	V	
I/O Output Low DDR1 (DDR2) (SSTL2)	V_{OL}	See JESD8-9 (JESD8-15A) standard.			V	
I/O Output High DDR1 (DDR2) (SSTL2)	V_{OH}	See JESD8-9 (JESD8-15A) standard.			V	
I/O Input Common-Mode	V_{ICM}	0		V_{DD}	V	
I/O Input Low (LVDS)	V_{IL}	– 0.3		V_{ICM} – 0.05	V	
I/O Input High (LVDS)	V_{IH}	V_{ICM} + 0.05		+1.9	V	
I/O Output Low (LVDS)	V_{OL}	+0.832	+1.01	+1.197	V	
I/O Output High (LVDS)	V_{OH}	+1.243	+1.377	+1.509	V	
Input Leakage Current (no pull-up or pull-down)	I_{IL1}	0		1	µA	
Input Leakage Current (with internal pull-down)	I_{IL2}	0 (LPDL)		200 (MPUL)	µA	1
Input Leakage Current (with internal pull-up)	I_{IL3}	–150 (LPDL)		0 (MPUL)	µA	1

Table 9. Recommended DC Operating Conditions (Sheet 2 of 2)

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
I/O Maximum Allowable Overshoot (3.3V LVTTL)	V_{MAO}			+3.9	V	
I/O Maximum Allowable Undershoot (3.3V LVTTL)	V_{MAU}	−0.6		0	V	
Case Temperature	T_C	−40		+85	℃	

Notes:

1. LPDL is least positive down level; MPUL is most positive up level.

Table 10. I/O Input Capacitance

Parameter	Symbol	Maximum	Unit	Notes
3.3V LVTTL	C_{IN1}	2.3	pF	
2.5V CMOS	C_{IN2}	2.1	pF	
2.5/1.8V SSTL2	C_{IN3}	3.2	pF	
PCI Express differential data receiver	C_{IN4}	1.59	pF	
PCI Express differential data transmitter	C_{IN5}	1.16	pF	
PCI Express differential clock receiver	C_{IN6}	0.188	pF	

Table 11. Typical DC Power Supply Requirements with DDR1 SDRAM

Frequency (MHz)	+1.2V	+1.8V	+2.5V	+3.3V	Total	Unit	Notes
333	1.15	0	0.54	0.10	1.79	W	1, 2
400	1.25	0	0.60	0.14	1.99	W	1, 3
533	1.25	0	0.58	0.12	1.95	W	1, 4
600	1.27	0	0.54	0.10	1.91	W	1,5

Notes:

1. Values are estimates and subject to change.
2. DDR1 running at 333MHz., PLB running at 166MHz.
3. DDR1 running at 400MHz., PLB running at 200MHz.
4. DDR1 running at 355MHz., PLB running at 177MHz.
5. DDR1 running at 400MHz., PLB running at 200MHz.

Table 12. Typical DC Power Supply Requirements with DDR2 SDRAM

Frequency (MHz)	+1.2V	+1.8V	+2.5V	+3.3V	Total	Unit	Notes
333	1.15	0.26	0.17	0.10	1.689	W	1, 2
400	1.25	0.28	0.17	0.14	1.84	W	1, 3
533	1.25	0.27	0.20	0.12	1.84	W	1, 4
600	1.27	0.26	0.17	0.10	1.80	W	1, 5

Notes:

1. Values are estimates and subject to change.
2. DDR2 running at 333MHz., PLB running at 166MHz.
3. DDR2 running at 400MHz., PLB running at 200MHz.
4. DDR2 running at 355MHz., PLB running at 177MHz.
5. DDR2 running at 400MHz., PLB running at 200MHz.

Table 13. DC Power Supply Loads with DDR1 SDRAM

Parameter	Symbol	Typical	Maximum	Unit	Notes
V_{DD} (+1.2V) active operating current	$I_{DD1.2}$	920	1390	mA	1
AV_{DD} (+1.2V) active operating current	I_{ADD}	40	50	mA	1
AHV_{DD} (+2.5V) active operating current	I_{AHDD}	100	120	mA	1
OV_{DD} (+3.3V) active operating current	I_{ODD}	40	50	mA	1
SV_{DD} + EOV_{DD} (+2.5V) active operating current	I_{DD}	200	240	mA	1
SAV_{DD} (+2.5V) active operating current	I_{SADD}	100	120	mA	1
EAV_{DD} (+2.5V) active operating current	I_{EADD}	100	120	mA	1

Notes:

1. Typical and Maximum values are estimates and subject to change.

Table 14. DC Power Supply Loads with DDR2 SDRAM

Parameter	Symbol	Typical	Maximum	Unit	Notes
V_{DD} (+1.2V) active operating current	I_{DD}	920	1390	mA	1
AV_{DD} (+1.2V) active operating current	I_{ADD}	40	50	mA	1
AHV_{DD} (+2.5V) active operating current	I_{AHDD}	100	120	mA	1
OV_{DD} (+3.3V) active operating current	I_{ODD}	40	50	mA	1
SV_{DD} (+1.8V) active operating current	I_{SDD}	180	210	mA	1
EOV_{DD} (+2.5V) active operating current	I_{EODD}	20	30	mA	1
SAV_{DD} (+2.5V) active operating current	I_{SADD}	100	120	mA	1
EAV_{DD} (+2.5V) active operating current	I_{EADD}	100	120	mA	1

Notes:

1. Typical and Maximum values are estimates and subject to change.

Test Conditions

Clock timing and switching characteristics are specified in accordance with *minimum* operating conditions shown in the table “Recommended DC Operating Conditions” on page 48. For all signals, AC specifications are characterized at T_C = 85°C with the test load shown in the figure to the right.

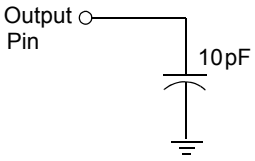
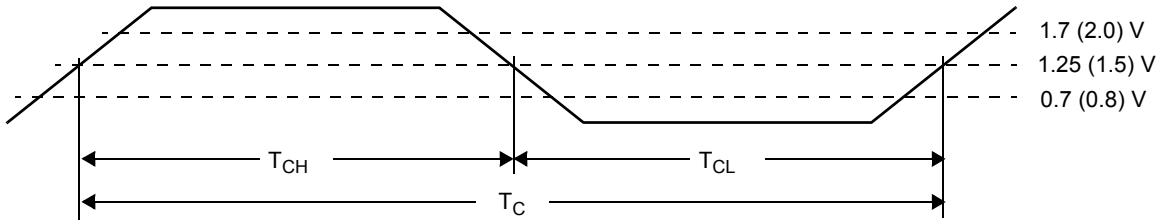


Table 15. System Clocking Specifications

Symbol	Parameter	Minimum	Maximum	Units
CPU				
PF_C	Processor clock frequency (must be ≥ SCF_C)	333.33	666.66	MHz
SysClk Input				
SCF_C	Frequency	33.33	100	MHz
SCT_{CS}	Edge stability (phase jitter, cycle-to-cycle)	na	± 0.1	ns
SCT_{CH}	High time (% of nominal period)	40	60	%
SCT_{CL}	Low time (% of nominal period)	40	60	%
SC_{RT}	Rise time	na	0.4	ns
Other Clocks				
$VCOF_C$	VCO frequency	600	1800	MHz
$PLBF_C$	PLB frequency	133	200	MHz
$OPBF_C$	OPB frequency	66	100	MHz

Figure 3. Clocking Waveform

Note: SysClk and GMCRefClk are 2.5V (3.3V tolerant) signals. Rise time should be measured between 0.7V and 1.7V.



Spread Spectrum Clocking

Care must be taken if using a spread spectrum clock generator (SSCG) with the PPC405EX. This controller uses a PLL for clock generation inside the chip. The accuracy with which the PLL follows the SSCG is called tracking skew. The PLL bandwidth and phase angle determine how much tracking skew exists between the SSCG and the PLL for a given frequency deviation and modulation frequency. If using an SSCG with the PPC405EX the following conditions must be met:

- The frequency deviation must not violate the minimum clock cycle time. Therefore, when operating the PPC405EX with one or more internal clocks at their maximum supported frequency, the SSCG can only lower the frequency.
- The maximum frequency deviation must not exceed −3%, and the modulation frequency must not exceed 40 kHz. In some cases, on-board PPC405EX peripherals impose more stringent requirements (see Note 1).
- Use the peripheral bus clock for logic that is synchronous to the peripheral bus because this clock tracks the modulation.

Notes:

1. The serial port baud rates are synchronous to the modulated clock. The serial port has a tolerance of approximately 1.5% on baud rate before framing errors begin to occur, assuming that the connected device is running at precise baud rates. If an external serial clock is used, baud rate ~~is unaffect~~ed by the modulation.
2. Ethernet operation is unaffected.
3. IIC operation is unaffected.

Caution: The system designer must ensure that any SSCG used with the PPC405EX meets these requirements and does not adversely affect other aspects of the system.

Table 16. Peripheral Interface I/O Clock Timings (not SDRAM or PCI-E)

Clock	Minimum	Maximum	Units	Notes
GMCTxClk frequency	125	125	MHz	
GMCTxClk high time	45% of nominal	–	ns	
GMCTxClk low time	55% of nominal	–	ns	
GMCRxClk frequency	125	125	MHz	
GMCRxClk high time	45% of nominal	–	ns	
GMCRxClk low time	55% of nominal	–	ns	
GMCGTxClk	125	125	MHz	
GMCMDClk	2.5	25	MHz	
GMCRefClk	125	125	MHz	
GMCRefClk edge stability (phase jitter, cycle-to-cycle)	na	± 0.1	ns	
GMCRefClk rise time	na	0.4	ns	
GMCRefClk high time	40% of nominal	–	ns	
GMCRefClk low time	60% of nominal	–	ns	
GMCnRxClk	125	125	MHz	
GMCnTxClk	125	125	MHz	
UARTSerClk		1000 $2T_{OPB1}$ + 2ns	MHz	1
TmrClk	na	100	MHz	
PerClk	33	100	MHz	
TCK	na	20	MHz	
USB2Clk (60MHz ± 0.05%)	57.97	60.03	MHz	
TrcClk	66	200	MHz	2

Notes:

1. T_{OPB} is the period in ns of the OPB clock. The internal OPB clock runs at an integral divisor ratio of the frequency of the PLB clock. The maximum OPB clock frequency is 100MHz.
2. TrcClk is 1/2 CPU Clk. The maximum CPU Clk supported for instruction trace is 400 MHz.

Figure 4. Input Setup and Hold Timing Waveform

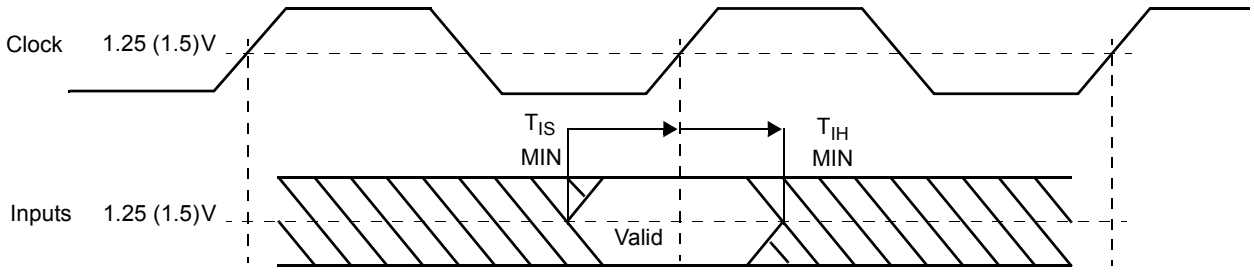


Figure 5. Output Delay and Float Timing Waveform

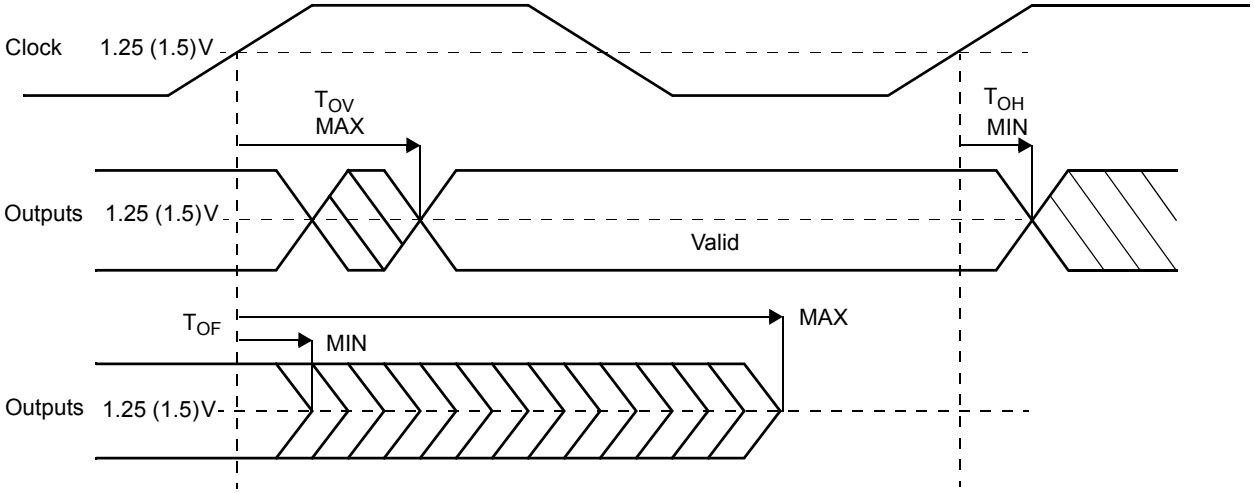
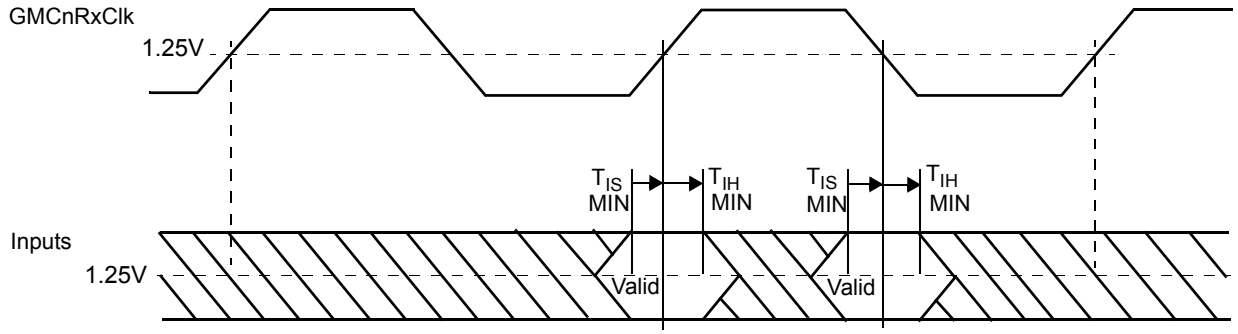
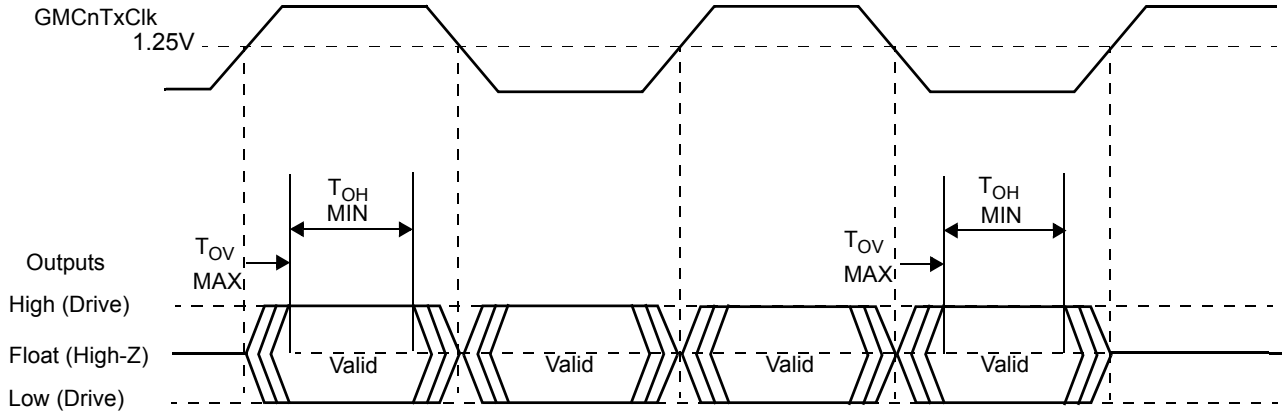


Figure 6. Input Setup and Hold Timing Waveform for RGMII Signals



RGMII 1000Mb timing is with reference to the raising and falling edge of GMCnRxClk.
RGMII 10/100Mb timing is with reference only to the raising edge of GMCnRxClk.

Figure 7. Output Delay and Hold Timing Waveform for RGMII Signals



RGMII 1000Mb timing is with reference to the raising and falling edge of GMCnTxClk.
RGMII 10/100Mb timing is with reference only to the raising edge of GMCnTxClk.

Table 17. I/O Specifications—All CPU Speeds (Sheet 1 of 2)

Notes:
1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I_{OH} (min)	I_{OL} (min)		
Ethernet GMII Interface								
GMCMDIO	2	0	2.5	2	5.51	7.23	Async	1
GMCCD	2	0			na	na	Async	1
GMCCrS	2	0			na	na	Async	1
GMCRxD0:7	1.85	0			na	na	GMCRxClk	1
GMCRxDV	1.95	0			na	na	GMCRxClk	1
GMCRxEr	1.95	0			na	na	GMCRxClk	1
GMCTxD0:7			2.3	2.0	5.51	7.23	GMCTxClk	1
GMCTxEr			2.4	2.0	5.51	7.23	GMCTxClk	1
GMCTxEn			2.4	2.0	5.51	7.23	GMCTxClk	1
Ethernet RGMII Interface (n = 0 or 1)								
GMCnRxD0:3	0.7	1			na	na	GMCnRxClk	1
GMCnRxCtl	0.8	1			na	na	GMCnRxClk	1
GMCnTxD0:3			0.5	2.7	5.51	7.23	GMCnTxClk	1
GMCnTxCtl			0.5	2.7	5.51	7.23	GMCnTxClk	1
Internal Peripheral Interfaces (not SDRAM or PCI-E)								
IICnSData					na	10.46		
$\overline{\text{UARTnCTS}}$			na	na	15.75	10.46		
$\overline{\text{UARTnRTS}}$	na	na			15.75	10.46		
$\overline{\text{UARTnDSR}}$			na	na	15.75	10.46		
$\overline{\text{UARTnDCD}}$			na	na	15.75	10.46		
$\overline{\text{UARTnDTR}}$	na	na			15.75	10.46		
$\overline{\text{UARTnRI}}$	na	na			15.75	10.46		
UARTnRx	na	na			na	na		
UARTnTx			na	na	15.75	10.46		
SCPDI					na	na		
SCPDO					na	10.46		
USB2Data0:7	3.9	0	6.3	2	15.75	10.46	USB2Clk	
USB2Dir	3.7	0	6.4	2	na	na	USB2Clk	
USB2Next	3.5	0			na	na	USB2Clk	
USB2Stop			6.4	2	15.75	10.46	USB2Clk	
DMA Interface								
DMAAck0:3			5.2	1.0	15.75	10.46	PerClk	
DMAReq0:3	2.4	1			na	na	PerClk	
DMAEOT0:3	2	1	5.3	1.0	15.75	10.46	PerClk	
Interrupts Interface								
IRQ0:9					15.75	10.46		
JTAG Interface								
TDI					na	na		
TDO					15.75	10.46		
TMS					na	na		
$\overline{\text{TRST}}$					na	na		

Table 17. I/O Specifications—All CPU Speeds (Sheet 2 of 2)

Notes:
1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I_{OH} (min)	I_{OL} (min)		
System Interface								
GPIO00:10	na	na	na	na	11.08	7.37		
GPIO11:15	na	na	na	na	5.51	7.23		
GPIO16:27	na	na	na	na	11.08	7.37		
GPIO28	na	na	na	na	15.75	10.46		
GPIO29:31	na	na	na	na	11.08	7.37		
$\overline{\text{Halt}}$	na	na	na	na	na	na		
SysErr	na	na	na	na	5.51	7.23		
$\overline{\text{SysReset}}$	na	na	na	na	5.51	7.23		

Table 18. I/O Specifications—333 MHz to 600 MHz CPU

Notes:
1. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I_{OH} (minimum)	I_{OL} (minimum)		
External Peripheral Interface (not SDRAM or PCI-E)								
PerAddr05:31	1.8	1	5.3	1	11.08	7.37	PerClk	
$\overline{\text{PerCS0:3}}$			5.2	1	11.08	7.37	PerClk	
PerData00:31	2.7	1	5.3	1	11.08	7.37	PerClk	
PerDataPar0:3	1.9	1	5.3	1	11.08	7.37	PerClk	
$\overline{\text{PerOE}}$			5.2	1	11.08	7.37	PerClk	
PerReady	2	1			na	na	PerClk	
PerR$\overline{\text{W}}$	1.8	1	5.3	1	11.08	7.37	PerClk	
$\overline{\text{PerWBE0:3}}$	1.7	1	5.1	1	11.08	7.37	PerClk	
$\overline{\text{PerBLast}}$	2	1	5	1	11.08	7.37	PerClk	
PerErr	1.9	1	5.3	1	11.08	7.37	PerClk	
$\overline{\text{ExtReset}}$			5.3	1	11.08	7.37	PerClk	
BusReq	2.3	1	5.1	1	11.08	7.37	PerClk	
HoldReq	2	1	5.2	1	na	na	PerClk	
HoldAck			5.2	1	11.08	7.37	PerClk	
$\overline{\text{ExtAck}}$	2.3	1	5	1	11.08	7.37	PerClk	
$\overline{\text{ExtReq}}$	2	1	5.3		na	na	PerClk	
NFALE			5.3	1	11.08	7.37	PerClk	
$\overline{\text{NFCE0:3}}$			5.3	1	11.08	7.37	PerClk	
NFCLE			5.3	1	11.08	7.37	PerClk	
NFData0:15	2.3	1	5.3	1	11.08	7.37	PerClk	
$\overline{\text{NFRdyBusy}}$	1.7	1			na	na	PerClk	
$\overline{\text{NFREn}}$			5.3	1	11.08	7.37	PerClk	
$\overline{\text{NFWEn}}$			5.3	1	11.08	7.37	PerClk	

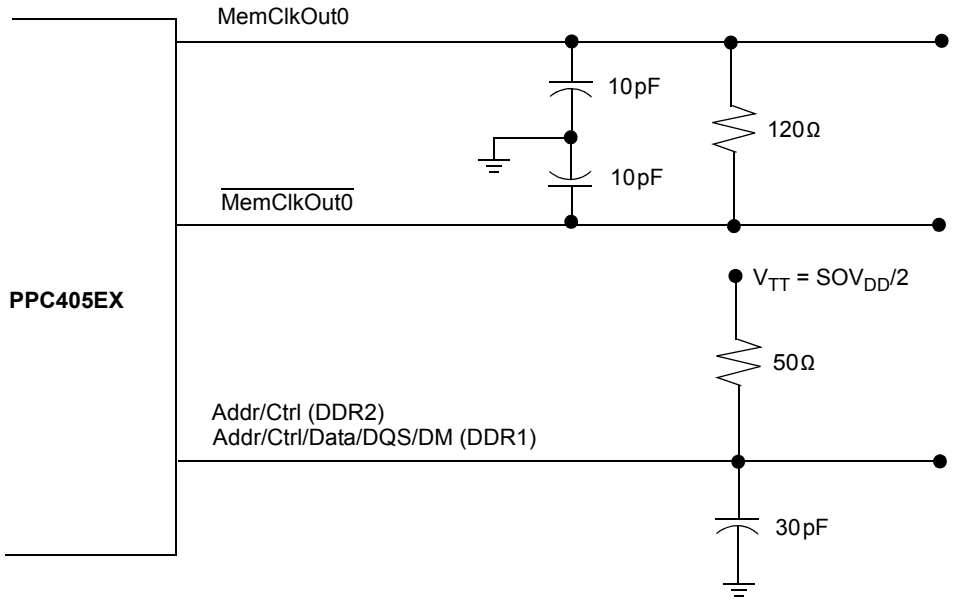
DDR 1/2 SDRAM I/O Specifications

The DDR SDRAM controller times its operation using the internal PLB clock signal and generates MemClkOut from the PLB clock. The PLB clock is an internal signal that cannot be directly observed. However MemClkOut is the same frequency as the PLB clock signal and is in phase with the PLB clock signal.

Note: MemClkOut can be advanced with respect to the PLB clock by means of the SDRAM0_CLKTR programming register. In a typical system, users advance MemClkOut by 90°. This depends on the specific application and requires a thorough understanding of the memory system in general (refer to the DDR SDRAM Controller chapter in the *PPC405EX Embedded Processor User's Manual*).

The signals are terminated as indicated in *Figure 8* for the DDR timing data and output currents in the following sections.

Figure 8. DDR SDRAM Simulation Signal Termination Model



Note: This diagram illustrates the model of the DDR SDRAM interface used when generating simulation timing data. It is *not* a recommended physical circuit design for this interface. An actual interface design depends on many factors, including the type of memory used and the board layout.

DDR2 SDRAM On-Die Termination Impedance Setting

For all DDR2 applications, the On-Die Termination (ODT) impedance value *must* be set to 75 ohms in the DIMM Extended Mode Register (EMR) in order to optimize the data transmission during memory write operations.

Table 19. DDR SDRAM Output Driver Specifications

Signal Path	Output Current (mA)	
	I/O H (maximum)	I/O L (maximum)
Write Data		
MemData00:31	10	10
ECC0:7	10	10
DM0:4	10	10
MemClkOut0	10	10
MemAddr00:14	10	10
BA0:2	10	10
$\overline{RAS}$	10	10
$\overline{CAS}$	10	10
$\overline{WE}$	10	10
$\overline{BankSel0:1}$	10	10
MemClkEn	10	10
DQS0:4	10	10
MemODT0:1	10	10

DDR SDRAM Write Operation

The rising edge of MemClkOut aligns with the first rising edge of the DQS signal on writes as indicated in *Figure 9*. DQS rising and falling edges are centered on valid data for writes.

The data in *Table 20* is generated by means of simulation and includes logic, driver, package RLC, and lengths. Values are calculated over best case and worst case processes with speed, junction temperature, and voltage as follows:

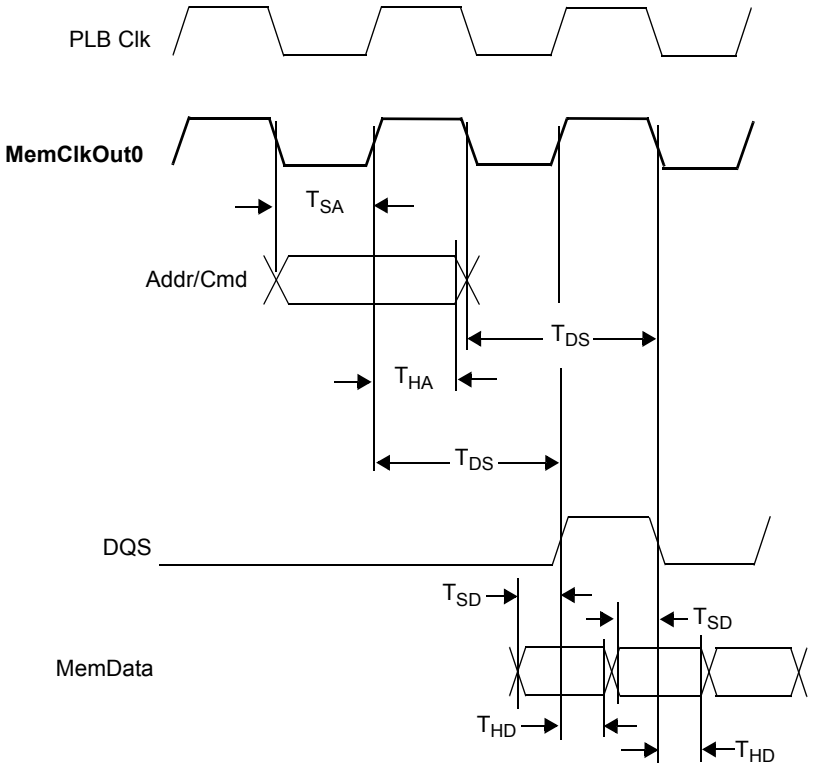
Table 20. DDR SDRAM Write Operation Conditions

Case	Process Speed	Junction Temperature (°C)	Voltage (V)
Best	Fast	−40	+1.3
Worst	Slow	+125	+1.1

Note: In the following tables and timing diagrams, minimum values are measured under best case conditions and maximum values are measured under worst case conditions. The timing numbers in the following sections are obtained using a simulation that assumes a model as shown in *Figure 8*.

The following diagram illustrates the relationship among the signals involved with a DDR write operation.

Figure 9. DDR SDRAM Write Cycle Timing



T_{SA} = Setup time for address and command signals to MemClkOut0
T_{HA} = Hold time for address and command signals from MemClkOut0
T_{SD} = Setup time for data signals (minimum time data is valid *before* rising/falling edge of DSQ)
T_{HD} = Hold time for data signals (minimum time data is valid *after* rising/falling edge of DSQ)
T_{DS} = Delay from rising/falling edge of clock to the rising/falling edge of DQS

Note: The timing data in the following tables is based on simulation runs using Einstimer.

Table 21. I/O Timing—DDR SDRAM T_{DS}

Notes:
1. All of the DQS signals are referenced to MemClkOut0 with the DQS delay line programmed to 1 cycle.
2. Clock speed is 200MHz.

Signal Name	T_{DS} (ns)	
	Minimum	Maximum
DQS0	4	6
DQS1	4	6
DQS2	4	6
DQS3	4	6
DQS4	4	6

Table 22. I/O Timing—DDR SDRAM T_{SA} and T_{HA}

Signal Name	T_{SA} (ns) Minimum	T_{HA} (ns) Minimum
MemAddr00:14	1.08	1.12
BA0:2	1.12	1.15
$\overline{\text{BankSel0:1}}$	1.09	1.13
MemClkEn	1.10	1.16
$\overline{\text{CAS}}$	1.10	1.13
$\overline{\text{RAS}}$	1.09	1.12
$\overline{\text{WE}}$	1.08	1.16

Table 23. I/O Timing—DDR SDRAM Write Timing T_{SD} and T_{HD}

Notes:
1. T_{SD} and T_{HD} are measured under worst case conditions.
2. Clock speed for the values in the table is 200MHz.
3. The time values in the table include 1/4 of a cycle at 200MHz (5ns x 0.25 = 1.25 ns).
4. To obtain adjusted T_{SD} and T_{HD} values for lower clock frequencies, subtract 1.5 ns from the values in the table and add 1/4 of the cycle time for the lower clock frequency (for example, $T_{SD} - 1.25 + 0.25T_{CYC}$).

Signal Names	Reference Signal	T_{SD} (ns)	T_{HD} (ns)
MemData00:07, DM0	DQS0	1.067	0.973
MemData08:15, DM1	DQS1	1.074	0.973
MemData16:23, DM2	DQS2	1.082	0.973
MemData24:31, DM3	DQS3	1.088	0.973
ECC0:7, DM4	DQS4	1.012	0.973

DDR SDRAM Read Operation

Data on a read is edge aligned with DQS. To capture the incoming data on the rising and falling edges, DQS is delayed by the DDR controller in order to center a DQS edge on valid data. Programmable registers control the delay.

DDR SDRAM MemClkOut0 and Read Clock Delay

In order to accommodate timing variations introduced by memory layout and process, a three-stage data path is used to eliminate metastability and allow data sampling to be adjusted for minimum latency.

Figure 10 shows the data read path of a single data bit. Data entering on the left is captured in the Stage 1 Flip Flops. Four Flip Flops are needed to capture an entire four beat burst on the DDR interface. The DDR controller only supports burst of four. Data captured on the rising edge of DQS is stored in the even numbered Flip Flops. Like wise, data captured on the falling edge of DQS is stored in the odd numbered Flips Flops.

To latch the data in Stage 1, a delayed version of DQS is used. Initialization software is responsible for tuning the DQS delay timing so that DQS is centered on valid data. Since there is process variation between parts and possible voltage variations on boards, read tuning is required. Fixed DQS delay values should not be used on production systems.

The Feedback Data Capture Window selects which Flip Flop is used to store the data sampled by DQS. Each output of this block generates a pulse to an input multiplexor. The series of four pulses selecting the input multiplexor is initiated by a feedback signal pulse on the input of the Feedback Data Capture Window. The DDR controller calculates when to assert the feedback signal based on when the data should be present after a read command.

The width of the feedback pulse is the same as DDR 1X clock. The internal DDR 1X clock is the same frequency as MemClkOut0. MemClkOut0 is slightly delayed relative to DDR 1X clock due to the insertion delay of the drivers.

The feedback signal to the Feedback Data Capture Window is adjusted for propagation delay by the fine/coarse delays and is automatically adjusted for variations in the DDR I/O due to supply voltage and temperature. Compensation for driver/receiver variations is accomplished by driving and receiving the feedback signal on the external MemFBD and MemFBR pins. Tuning the fine/coarse delays adjust for propagation delay. When properly tuned, the feedback pulse is aligned to the first DQS in a four beat burst such that the rising edge of DQS is nominally centered on the feedback pulse.

Software can adjust the pulse using the fine/coarse delays. Connection of MemFBD directly to MemFBR with the minimum trace length is recommended.

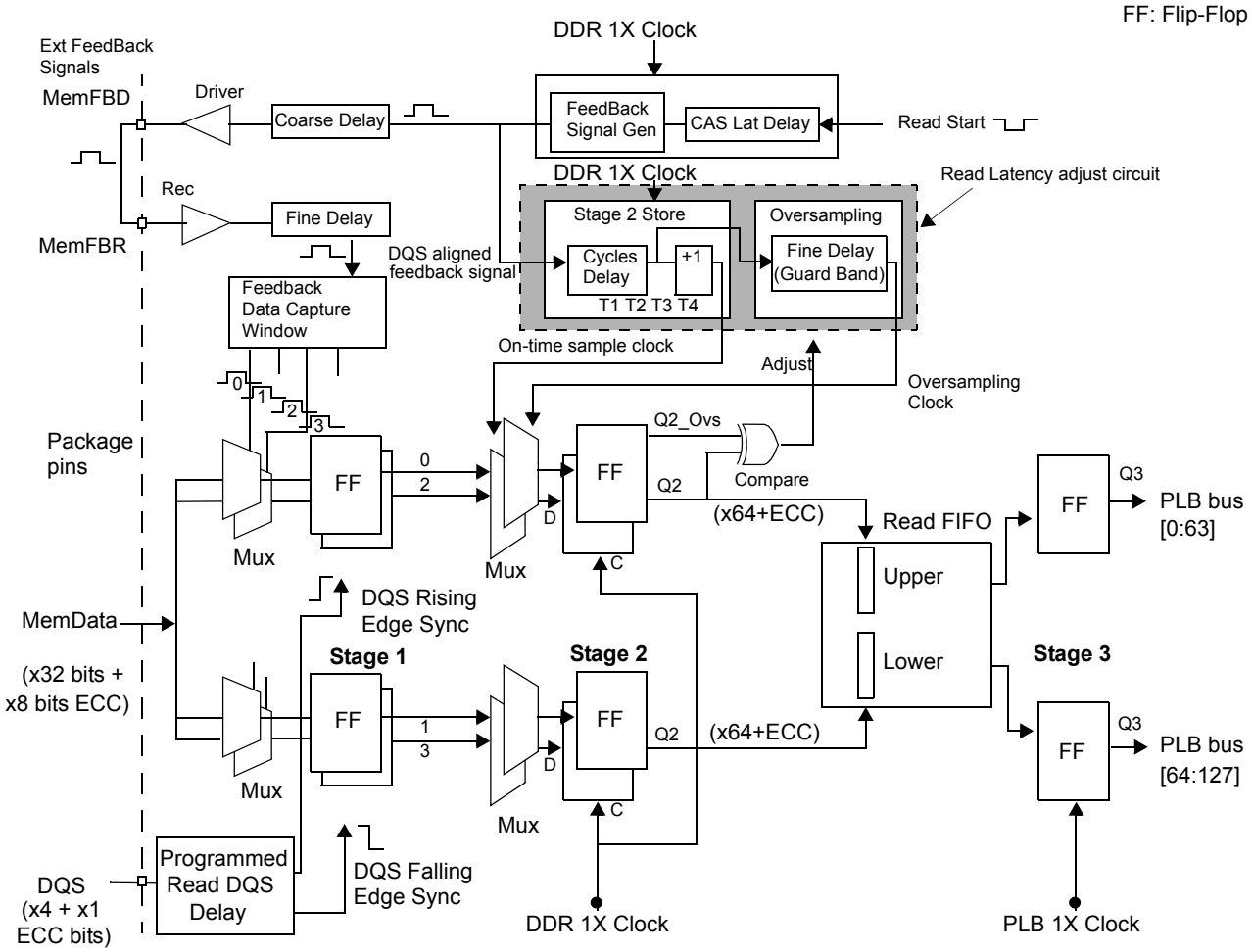
The data captured in Stage 1 is relative to the DQS timing domain and is held for two DDR 1X cycles. Stage 2 samples the data in Stage 1 attempting to capture the first and/or second cycle of data in the DDR 1X domain. The on-time-sample clock from the Stage 2 Store block samples the Stage 1 data at sample cycle T1, T2, T3 or T4. The sample cycle is either selected by initialization software or can be automatically selected and adjusted by the DDR controller. The Stage 1 data is sampled a second time by the over sample clock at a delayed sample point. The delay between the on-time-sample and over sample clocks is the Over-Sampling-Guard-Band.

The feedback pulse is sampled with the data captured by the first DQS in the four beat burst. A match of one or both of the sample clocks with the feedback pulse is a hit. The DDR controller based on hits or misses by the on-time sample and over sample clocks adjust the sample cycle in order to track variations in DQS. Burst data from a sample hit is passed to Stage 3.

In Stage 3 the data is synchronized to the PLB clock domain and eventually driven onto the PLB bus. The data captured on the rising and falling DQS edges is unpacked into the correct bit locations on the upper (0:63) and lower (64:127) PLB bus. When ECC is enable, ECC checking and corrections is done after Stage 3.

Figure 12 illustrates how the three Stage read logic captures the data in the DQS timing domain and synchronizes it to the PLB clock domain. The first DQS of four beat burst is roughly centered on feedback signal pulse.

Figure 10. DDR SDRAM Read Data Path for a Single Data Bit



ECC detection and correction if enabled occurs after Stage 3 before completing the read on the PLB.

DDR SDRAM Read Cycle Timing

The following diagram illustrates the relationship of the signals involved with a DDR read operation.

Figure 11. DDR SDRAM Memory Data and DQS

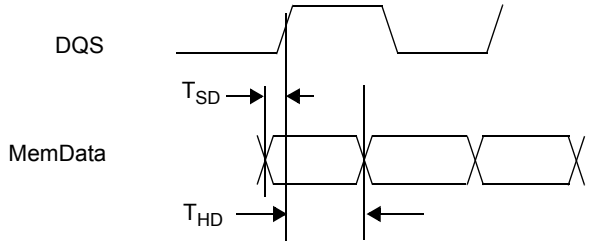


Table 24. I/O Timing—DDR SDRAM Read Timing T_{SD} and T_{HD}

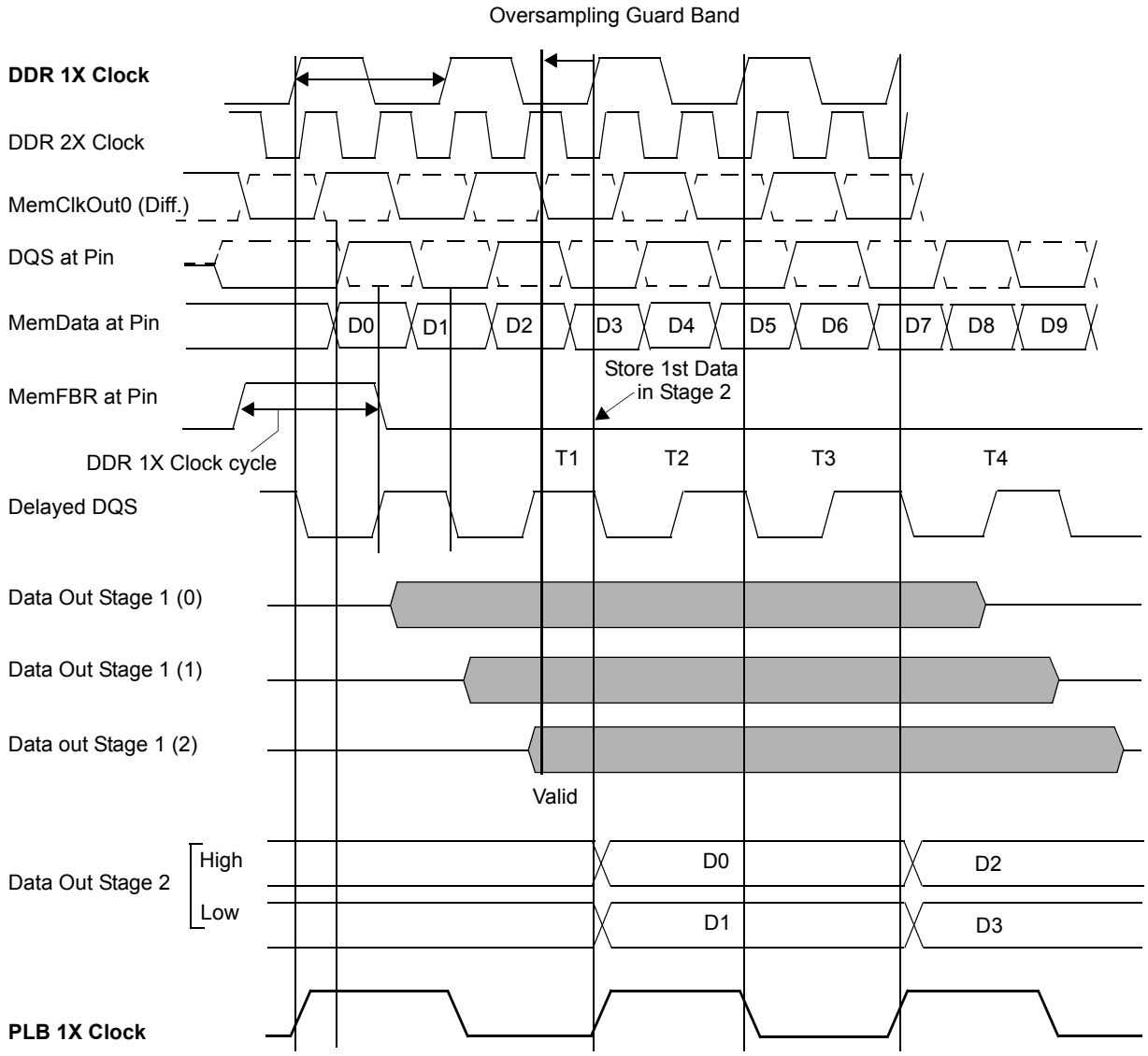
1. T_{SD} and T_{HD} are measured under worst case conditions.
2. Clock speed for the values in the table is 200MHz.
3. The time values in the table include 1/4 of a cycle at 200MHz (5ns x 0.25 = 1.25 ns).
4. To obtain adjusted T_{SD} and T_{HD} values for lower clock frequencies, subtract 0.75 ns from the values in the table and add 1/4 of the cycle time for the lower clock frequency (e.g., T_{SD} - 1.25 + 0.25T_{CYC}).

Signal Names	Reference Signal	Read Data vs DQS Set up T_{SD} (ns)	Read Data vs DQS Hold T_{HD} (ns)
MemData00:07	DQS0	0.27	0.45
MemData08:15	DQS1	0.27	0.45
MemData16:23	DQS2	0.27	0.45
MemData24:31	DQS3	0.27	0.45
ECC0:7	DQS4	0.27	0.45

In the following example, the data strobes (DQS) and the data are shown to be coincident. There is actually a slight skew as specified by the SDRAM specifications, and there can be additional skew due to loading and signal routing. It is recommended that the signal length for all of the DQS signals be matched.

The following example shows the timing relationship between SDRAM DDR Data at the input pin and storing the data in Stage 1.

Figure 12. DDR SDRAM Read Cycle Timing—Example



PCI Express (PCI-E) I/O Specifications

The following tables provide the required I/O timing information regarding the use of the PCI Express interface on this chip.

Table 25. PCI-E Receiver I/O Specifications

Parameter	Minimum	Maximum	Units	Notes
Unit Interval (UI)	399.88	400.12	ps	
Differential Rx peak-peak voltage	175	1200	mV	
Receiver eye time opening	0.4	-	UI	
Maximum time delta between median and deviation from median	-	0.3	UI	
Rx package plus Si differential return loss	10	-	dB	
Common mode Rx return loss	6	-	dB	
Receiver DC common mode impedance	40	60	Ω	
DC differential impedance	80	120	Ω	
Rx AC common mode voltage	-	150	mV	
DC Input CM input impedance during reset or power down	200	-	kΩ	
Electrical idle detect threshold	65	125	ns	

Table 26. PCI-E Reference Clock I/O Specifications

Parameter	Minimum	Maximum	Units	Notes
PCI_E reference clock frequency (PCIEnClkC and PCIEnClkT)	100	100	MHz	1
Accuracy	-300	+300	ppm	
Duty cycle	45	55	%	
1kHz to 1000kHz peak-to peak jitter	-	100	ps	2
1MHz to 6MHz peak-to peak jitter	-	40	ps	2
6MHz to 20MHz peak-to peak jitter	-	100	ps	2
Spread Spectrum Clock (SSC) frequency	30	33	kHz	3
Rise time	TBD	TBD	ns	
Common mode voltage	0	1600	mV	
Differential signal amplitude	200	-	mV	

Notes:

1. The PCI-E reference clock frequency specification does not include +/- 300ppm accuracy specification.
2. To convert to ps peak-to-peak jitter to ps RMS jitter, divide the peak-to-peak jitter by 13.9.
3. The data rate can be modulated from +0.5% to −0.5% of the nominal data rate frequency, at a modulation rate in the range not exceeding 30kHz–33kHz. The +/- 600ppm requirement remains which requires the two communcicating ports to be modulated so that they never exceed a total of 600ppm difference. For most implementations, this requires that both ports have the same bit rate clock source when the data is modulated with an SSC.

Table 27. PCI-E Transmitter I/O Specifications

Parameter	Minimum	Maximum	Units	Notes
Unit Interval (UI)	399.88	400.12	ps	
Differential p-p TX voltage swing	800	-	mV ppd	
Low power differential p-p TX voltage swing	400	-	mV ppd	
TX de-emphasis level ratio	-3.0	-4.0	dB	
Minimum TX eye width	0.75	-	UI	
Maximum time between the jitter median and maximum deviation from the median	-	0.125	UI	
Transmitter rise and fall time	0.125	-	UI	
Maximum Tx PLL bandwidth	-	22	MHz	
Minimum TX PLL BW for 3dB peaking	1.5	-	MHz	
TX AC common mode voltage	-	20	mV	
Absolute Delta of DC Common Mode Voltage during L0 and Electrical Idle.	0	100	mV	
Absolute Delta of DC Common Mode Voltage between PCIEnTX and $\overline{\text{PCIEnTX}}$	0	25	mV	
Electrical Idle Differential Peak Output Voltage	0	20	mV	
The amount of voltage change allowed during Receiver Detection	-	600	mV	
Transmitter DC common-mode voltage	0	3.6	V	
Transmitter short-circuit current limit	-	90	mA	
Minimum time spent in Electrical Idle	20	-	ns	
Maximum time to transition to a valid Electrical Idle after sending an EIOS	-	8	ns	
Maximum time to transition to valid differential signaling after leaving Electrical Idle	-	8	ns	
Differential return loss	10	-	dB	
Common mode return loss	6	-	dB	
DC differential TX impedance	80	120	Ω	

Initialization

The following describes the method by which initial chip settings are established when a system reset occurs.

Strapping

When the $\overline{\text{SysReset}}$ input is driven low (system reset), the state of certain I/O pins is read in order to enable default initial conditions before PPC405EX start-up. The actual instant of capture is the nearest system clock edge before the deassertion of reset. These pins must be strapped using external pull-up (logical 1) or pull-down (logical 0) resistors to select the desired default conditions. The recommended pull-up is 3kΩ to +3.3V, or 10kΩ to +5V. The recommended pull-down is 1kΩ to GND. These pins are only used for strap functions during reset. They are used for other signals during normal operation. The following table lists the strapping pins along with their functions and strapping options. The signal names assigned to the pins for normal operation appear below the pin number.

Table 28. Strapping Pin Assignments

		Pin Strapping		
Initialization Source	**Option**	**$\overline{\text{F04}}$** (UART0DCD)	**$\overline{\text{F02}}$** (UART0DSR)	**$\overline{\text{G02}}$** (UART0CTS)
EBC 8-bit wide ROM	A	0	0	0
EBC 16-bit wide ROM	B	0	0	1
EBC 16-bit wide ROM	C	0	1	0
EBC 8-bit wide NAND Flash	D	0	1	1
EBC 8-bit wide NAND Flash	E	1	0	0
IIC ROM at address 0xA8	G	1	0	1
EBC 8-bit wide ROM	F	1	1	0
IIC ROM at address 0xA4	H	1	1	1

Note: See the *PPC405EX Embedded Processor User's Manual* for option descriptions and other details regarding the boot process.

Revision Log

Date	Version	Contents of Modification
02/27/2007	1.00	Initial creation of document.
03/01/2007	1.01	Updates following review of initial document.
03/22/2007	1.02	Change package drawing to eliminate confusion. Expand system memory map. Define FSource0 signal as Reserved. Add Recommended Operating Conditions data. Add thermal data. Misc. updates and additions.
04/24/2007	1.03	Misc. updates and additions including some limited timing data.
05/24/2007	1.04	Correct one of three ball numbers assigned to PerData28. Swap four balls between V_{DD} and GND. Swap one ball between OV_{DD} and SV_{DD}. Correct typographical errors in Table 3. Add missing alphabetical entries for PerAddr05, NAND Flash, and IIC1. Add output current values to Tables 15 and 16.
06/04/2007	1.05	Input various review comments. Update Table 6 Notes column. Update Block Diagram. Swap SAV_{DD} an EAV_{DD} signal name assignments on package balls. Add two UART configurations. Add DDR SDRAM section extracted from 460EX with changes appropriate for 405EX. Update timing information for all interfaces. Add power values. Update I/O capacitance values.
06/07/2007	1.06	Remove Confidential status. Input various review comments.
06/28/2007	1.07	Input review comments and corrections. Change default signals for GPIO balls to GPIO00–GPIO27 signals. Eliminate confusing terminology in initialization section.
07/12/2007	1.08	Change voltage names so that SDRAM voltage is always SV_{DD} for both DDR1 and DDR2 types. Six voltage pins originally labeled SV_{DD} changed to EOV_{DD}.
08/21/2007	1.09	Update GMCRefClk specifications (rise time, jitter, etc.)
10/25/2007	1.11	Add I/O timing figures for RGMII signals. Correct AMCC telephone numbers. Change PerErr to always pull down. Implement doc issue 374. Change chip revision level from A to B (Doc issue 380). Implement doc issue 381. Revise I/O timing figures for RGMII signals. Major updates to DDR SDRAM section (and other parts of the DS) (Doc issue 392). Add PCI-E I/O specifications. I/O timing values updates. Change boot-from-EBC support (Doc Issue 383).
11/20/2007	1.12	Misc. updates. Change all 667 MHz specs to 600 MHz.

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