Raytheon

29000 Series Field Programmable Read-Only Memories

Features

- Low power Schottky technology
- Highly reliable nichrome fuses
- Three-state outputs
- PROM and SPROM versions of all configurations
- Typical SPROM "OFF" power is 25% of standard power
- SPROMs feature guaranteed access times and full V_{CC} tolerance under power-switched conditions
- All devices use same programming techniques (generic)
- All devices available in both commercial (0°C to +75°C) and military (-55°C to +125°C) versions
- All devices are industry standard pin-out
- All devices available in flat packages
- 16K and 32K devices available in 0.3" wide 24-pin dual in-line packages
- 8K and 32K devices available in leadless chip carriers

Applications

- Prototyping/volume production
- Non-volatile fixed instructions
- Microprogram control storage
- Complex LSI logic simulation
- Custom look-up tables
- Security encoding/decoding
- Error correction
- Code conversion
- Character generation

Description

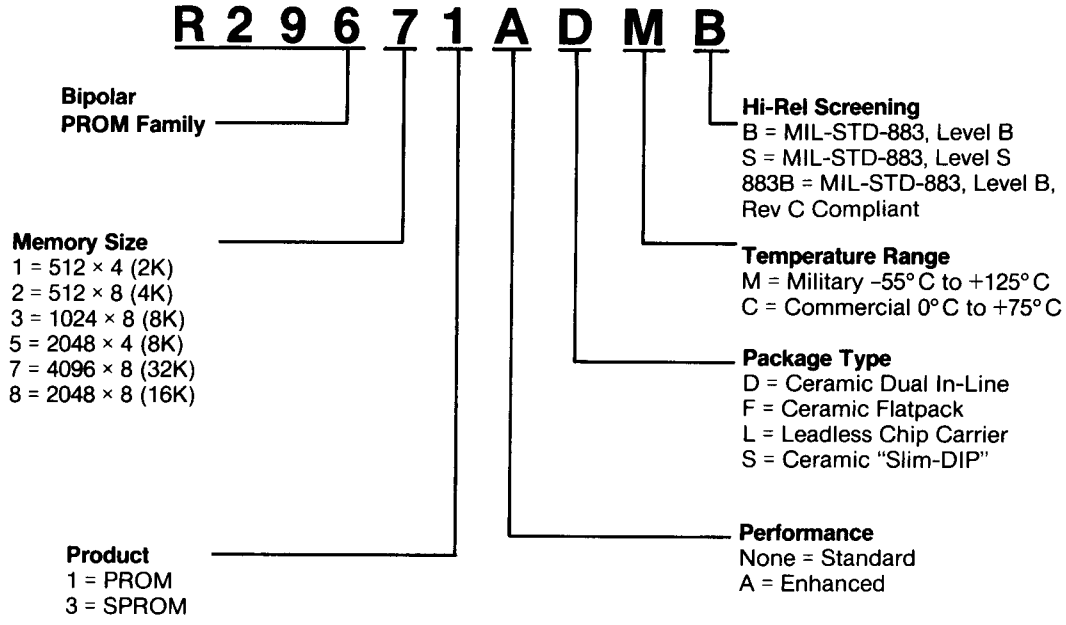
Raytheon's 29000 Series of Bipolar Field Programmable Read-Only Memories includes most of the popular PROM configurations in both standard and power-switched versions. The power-switched devices (SPROMs) were originated by Raytheon to reduce overall power dissipation in large PROM arrays. This technique takes advantage of the non-volatile nature of PROMs by removing power when a particular device is not being used in the system. Unlike previous power-switching schemes, which employed external transistors and resistors, the SPROM includes all power-switching circuitry on the same chip as the memory. Moreover, the power switch is activated by the same Chip Select (CS) input that is used to address a standard PROM; thus, in most cases, SPROMs can be directly substituted for standard devices without system redesign.

All Raytheon 29000 Series PROMs and SPROMs are manufactured with nichrome fuses and low power Schottky technology. The devices are shipped with all bits in the HIGH (logical ONE) state. To achieve a LOW state in a given bit position, the nichrome link is fused open by passing a short, high-current pulse through the link. All 29000 Series devices are programmed using the same programming technique.

Contents

Raytheon Company
Semiconductor Division
350 Ellis Street
Mountain View, CA 94039-7016
(415) 968-9211
TWX: 910-379-6484

Ordering Information



Country of Origin
R = U.S.A.
T = Mexico
M = Phillippines

Thermal Characteristics

Package	16, 18, 20-Lead Ceramic DIP	16, 18, 20-Lead Size Brazed DIP	24-Lead 600 Mil Ceramic DIP	24-Lead 600 Mil Size Brazed DIP	24-Lead 300 Mil Size Brazed DIP	16, 18, 20-Lead Ceramic Flat Package	24-Lead Ceramic Flat Package	Ceramic Leadless Chip Carrier
Max. Junction Temp.	175°C	175°C	175°C	175°C	175°C	175°C	175°C	175°C
Max. P_D $T_A < 50°C$	1388mW	1562mW	2083mW	2083mW	1666mW	1042mW	1388mW	1250mW
Therm. Res. θ_{JC}	25°C/W	25°C/W	20°C/W	15°C/W	15°C/W	25°C/W	20°C/W	20°C/W
Therm. Res. θ_{JA} (Note 1)	90°C/W	80°C/W	60°C/W	60°C/W	75°C/W	120°C/W	90°C/W	100°C/W
For $T_A < 50°C$ Derate at	11.1mW per °C	12.5mW per °C	16.7mW per °C	16.7mW per °C	13.3mW per °C	8.34mW per °C	11.1mW per °C	10.0mW per °C

Note: 1. In still air.

Absolute Maximum Ratings (Above which the useful life may be impaired).

Junction Temperature ..... -65°C to +175°C
Storage Temperature ..... -65°C to +150°C
Temperature
Under Bias ..... -55°C to +125°C
Supply Voltage to Ground
Potential (Continuous) .... -0.5V to +7.0V
DC Voltage Applied to
Outputs (Except During
Programming) ..... -0.5V to +V_{CC} Max
DC Input Voltage
(Address Inputs) ..... -0.5V to +5.5V
DC Voltage Applied to Outputs
During Programming 26V
Output Current into Outputs
During Programming 250mA
DC Input Voltage
(Chip Select Input-Pin) ..... -0.5V to +33V
DC Input Current ..... -30mA to +5.0mA

Operating Range

29000XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%	Commercial
29000XM	T_C = -55°C to +125°C	V_{CC} = 5.0V ±10%	Military

X denotes package type. Refer to the ordering information for complete details.

Common Electrical Characteristics Over Operating Range (unless otherwise noted)

Parameter	Description	Test Conditions		Min	Typ[1]	Max	Units
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -2.0mA V_{IN} = V_{IH} or V_{IL}		2.4	3.6		V
V_{OL}[3]	Output Low Voltage	V_{CC} = Min	I_{OL} = 8.0mA		0.30	0.4	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA		0.35	0.5	
V_{IH}	Input High Level	Guaranteed Input Logical High Voltage for All Inputs		2.0		5.5	V
V_{IL}	Input Low Level	Guaranteed Input Logical Low Voltage for All Inputs		0.0		0.8	V
I_{IL}	Input Low Current	V_{CC} = Max, V_{IN} = 0.4V			-10	-250	μA
I_{IH}	Input High Current	V_{CC} = Max, V_{IN} = 2.7V				10	μA
		V_{CC} = Max, V_{IN} = 5.5V				0.1	mA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_{OUT} = 0.2V (Note 2)		-12	-35	-85	mA
V_I	Input Clamp Voltage	V_{CC} = Min, I_{IN} = -18mA				-1.5	V
I_{CEX}	Output Leakage Current	V_{CC} = Max	V_O = 4.5V			+100	μA
		Chip Disabled	V_O = 0.45V			-100	

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = +25°C
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. This characteristic cannot be tested prior to programming; it is guaranteed by factory testing.

AC Test Conditions

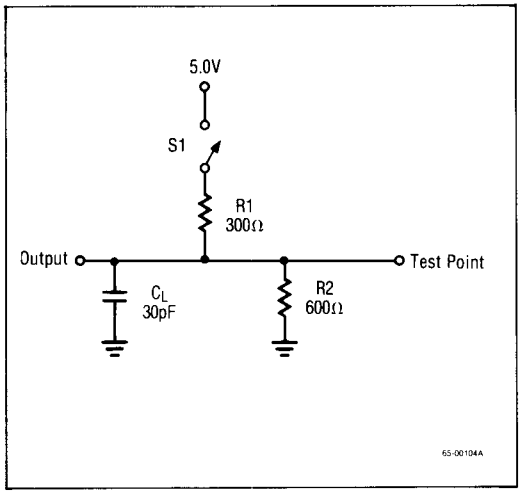


Figure 1. AC Test Circuit

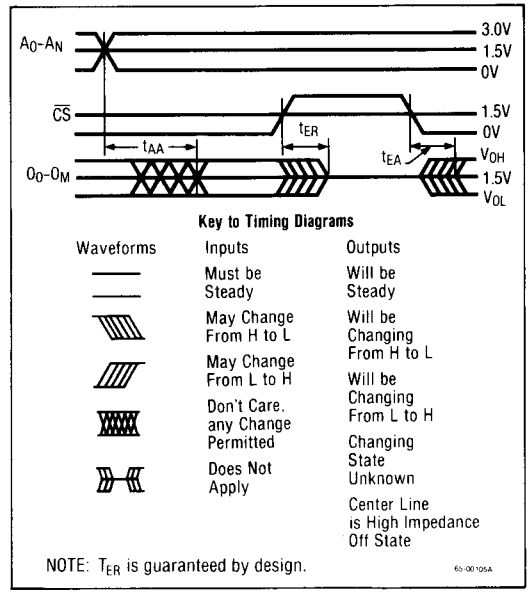


Figure 2. Switching Waveforms

Programming Instructions

General

The device is manufactured with all outputs high in all storage locations. To make an output low at a particular word, a nichrome fusible link must be opened. This procedure is called programming.

Programming Description

To select a particular link for programming, the word address is presented with TTL levels on A_O through A_N, a V_{CC} of 5.50V is applied or left applied. The program pin and the output to be programmed are taken to an elevated voltage to supply the required current to the fuse. The outputs must be programmed one at a time, since internal decoding circuitry is capable of sinking only one unit of programming current.

Other Chip Select Inputs

On some devices, additional Chip Select Inputs are present. These may be high, low or open during programming. When checking that an output is programmed (which is called verification) these inputs must be enabled to activate the device. Since they must be enabled during verification and the state is irrelevant during programming, the simplest procedure is to activate them during the entire procedure.

Timing

The programming procedure involves the use of the program pin (a chip select) and the output pin. In order to guarantee that the output transistor is off before increasing the voltage on the output pin, the program pin's voltage pulse must come before the output pin's programming pulse and leave after the output pin's programming pulse. The programming pulse applied to the output pin and program pin must have a 0.4V/μS rise time (see Figure 3).

It is recommended that only one programming pulse be applied for each bit to be programmed. To maximize programming yield, this pulse should be applied with V_{PP} = 33V and V_{OUT} = 26V. Any other conditions are not recommended.

Verification

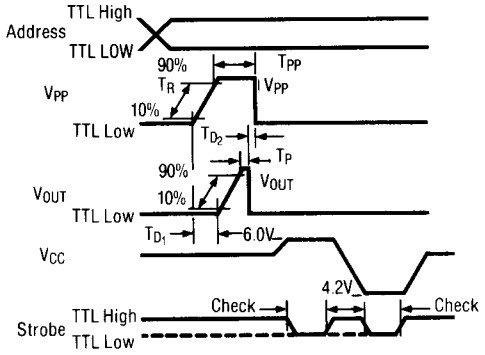
After programming a device, it can be checked for desired output logic states by enabling the device. To guarantee operation at minimum and maximum V_{CC}, current and temperature, the device must sink 12mA at a V_{CC} of 4.20V when low and 0.2mA at a V_{CC} of 6.2V when high at room temperature.

Board Programming

Units may be programmed at the board level by bringing the program pin of each package to the card connector. To program a particular package "A", the program pin of package A and one output pin of package A, which may or may not be "OR" tied to other packages, are taken to the required programming voltage. An alternate procedure is to tie the enable and outputs together as required by the system function and only apply V_{CC} to the device to be programmed. The number of units soldered on a board should be consistent with expected programming yields to avoid rework.

Unprogrammable Units

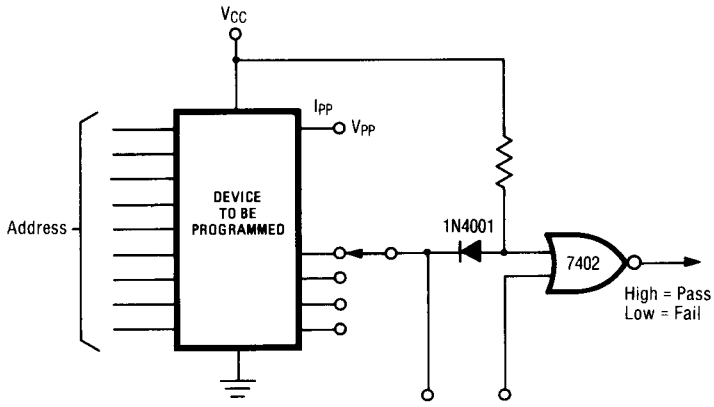
Visual inspection at 200X prior to encapsulation, test fuses and decoding circuitry tests are used to guarantee a high programming yield of the device in the field. However, because of random defects, it is impossible to guarantee that any given bit will program correctly. **Units returned to Raytheon as unprogrammable must be accompanied by a complete description of the programming method used and a contact phone number for clarification of any engineering or purchasing questions.**



$T_R = 0.4V/\mu \pm 15\%$
$T_{PP} = 95 \pm 15\mu S$
$T_P = 1\mu S$ min, $40\mu S$ max
$T_{D_1} = 80 \pm 10\mu S$
$T_{D_2} = 100nS$ min
$V_{PP} = 33V$
$V_{OUT} = 26V$

Note: Output Load = 0.2mA During 6.0V Check
Output Load = 12mA During 4.2V Check

Figure 3. Programming Timing



For proper threshold adjustment, insert a 2N404 germanium transistor with collector and emitter shorted so that it looks like a diode in series with pin 7 of the 7402 to ground.

Note: The 1N4001 diode protects the input of the 7402 from the high programming voltages.

Figure 4. Typical Programming Circuit

Programming Parameters (Do not test these limits or you may program the device)

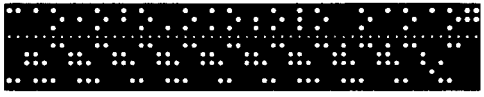
Parameter	Description	Test Conditions	Min	Typ	Max	Units
I_{PP}	Current Program Pin During Programming, Before and After Fuse has Blown	V_{CC} = 5.50V V_{OUT} = 5.0V to 25V V_{PP} = 4.50V		0		mA
		V_{PP} = 27V		30		mA
I_{OUT}	Current into Output During Programming Before the Fuse has Programmed	V_{PP} = 27V, V_{CC} =5.50V V_{OUT} = 4.5V		0.1		mA
		V_{OUT} = 20V		70		mA
I_{OUT}	Current into Output During Programming After the Fuse has Programmed	V_{PP} = 27V V_{OUT} = 20V V_{CC} = 5.50V		50		mA
T_R	Rise Time of Program Pulse Applied to the Data Out or Program Pin		0.34	0.4	0.46	V/μS
V_{CCP}	V_{CC} Required During Programming		5.40	5.50	5.60	V
I_{OLV_1}	Output Current Required During Verification	Both Chip Enables Low T_A = 25° C, V_{CC} = 4.2V	11	12	13	mA
I_{OLV_2}	Output Current Required During Verification	Both Chip Enables Low	0.1	0.2	0.3	mA
MDC	Maximum Duty Cycle During Automatic Programming of Program Pin	$\frac{T_{PP}}{T}$			50	%
V_{PP}	Required Programming Voltage on Program Pin		27		33	V
V_{OUT}	Required Programming Voltage on Output Pin		20		26	V
I_L	Required Current Limit of the Power Supply Feeding the Program Pin and the Output During Programming	V_{PP} = 33V V_{OUT} = 26V V_{CC} = 5.50V	250			mA
T_P	Required Coincidence Among the Program Pin, Output, Address and V_{CC} for Programming		1.0		40	μS
T_{D_1}	Required Time Delay Between Disabling the Memory Output and Application of the Output Programming Pulse	Measure at 10% Levels	70	80	90	μS
T_{D_2}	Required Time Delay Between Removal of Programming Pulse and Enabling the Memory Output	Measure at 10% Levels	100			nS

Master PROM

Raytheon can program devices at our facility if the customer supplies a master PROM which contains the desired program.

Transferring programs via Master PROMs is considered the preferred method.

Paper Tape Format



The PROM program tape in hexadecimal code is sequentially formatted as follows:

1. Approximately 12 inches of unpunched leader section.
2. The applicable program tape number with any note or comment.
3. A data start mark consisting of 25 "control A" characters.
4. The data in hexadecimal characters (0-9 and A-F) which represent the output data of word Ø; a space and the output data of word 1; a space . . . etc.
5. The character "control C" is used to end the data string.

NOTE: "Carraige Return" and "Line Feed" characters may be included to make data more legible when printed out.

Truth tables can also be sent to Raytheon in an ASCII tape format. Information can be sent to us by air mail or TWX 910-379-6481. The tape reading equipment at Raytheon recognizes ASCII characters S, B, P, N, F, and E and interprets them as:

S Start
B Begin a word
P High data
N Low data
F Finish a word
E End of tape

All other characters such as carriage returns, line feeds, etc. are ignored so that comments and spaces may be sent in the data field to improve readability. Comments, however, should not use the characters S, B, P, N, F, and E. Word addresses must begin with zero and count sequentially to the highest address.

In order to assist the machine operator in determining where the heading information stops and the data field begins, 25 bell characters or rubout characters should precede the start of the truth table. Any type of 8 level tape (paper, mylar, fanfold, etc.) is acceptable. Channel 1 is the most significant bit and channel 8 (parity) is ignored. Sprocket holes are located between channels 3 and 4. Note that the order of the outputs between characters B and F is:

$O_8, O_7, O_6, O_5, O_4, O_3, O_2, O_1$

not

$O_1, O_2, O_3, O_4, O_5, O_6, O_7, O_8$

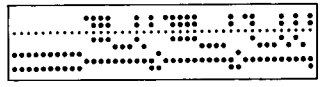
The required heading information at the beginning of the tape is as follows:

Customer name and phone _____
Customer TWX number _____
Purchase order number _____
Raytheon part number _____
Customer symbolized part number _____
Truth table number _____
Number of truth tables _____
Total number of parts _____
Number of parts of each truth table _____
25 bell or rubout characters _____

Example For X4 Devices

Blarney Electronics 408-735-8140
TWX 911-338-9225
P0142
29653
0431
12
1 8 level
3 TWX
3

BNNNPF BNNNNF BNPNPF BNPPPF
BNNNNF BNPNPF BNNPPF BPPPNF



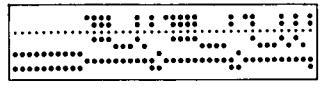
Begin Data Field
Data Field (P = High Voltage, N = Low Voltage)
Finished Data Field

B P P N P F BPPPPF BPNNPF etc. BPNNNF
0_4 0_3 0_2 0_1
Word 0 Word 1 Word 2 Word N

Example For X8 Devices

Blarney Electronics 408-735-8140
TWX 911-338-9225
P0142
29633 8 Level
etc. TWX

BNNNPPPNPF BNNNNPPPPF BNPPPNPNF BNNNNNNNF
BNNNNNNNF BNNNPPPNPF BPPPPPPPPF BNPPNPNNNF



Begin Data Field
Data Field (P = High Voltage, N = Low Voltage)
Finished Data Field

B P P P N P P N P F BPPPPPPPPF BPNPPPNNPF etc. BPPNPPNNNF
0_8 0_7 0_6 0_5 0_4 0_3 0_2 0_1
Word 0 Word 1 Word 2 Word N

Commercial Programmers

All Raytheon PROMs are designed and tested to give an average programming yield in excess of 90%. This average yield should be achieved using the programming procedure described previously or with any of the commercial PROM programmers listed below when they are properly calibrated and in good operating condition. Raytheon maintains a close relationship with programmer manufacturers to assure that their systems provide the proper programming environment for all Raytheon PROMs and SPROMs.

Programmer Manufacturing			Data I/O			Digilec	
Model/Series			Mod V	Mod IX, XIX, XXIX		Up 803	
Raytheon Part No.	Org.	Pins	Program Card Set 909-1226-1 Socket Adaptor	Unipak		Personality Module FAM12	
				Rev	Code	Device Adaptor	Device Code
29611 29613	512 x 4	16	715-1035-2	D	11 03	DA 1	4-12
29621 29623	512 x 8	20	715-1064	D	11 09	DA 4	4-15
29631 29633	1024 x 8	24	715-1033-3	D	11 16	DA 7	4-10
29651 29653	2084 x 8	18	715-1039	D	11 06	DA 3	4-12
29671 29673	4096 x 8	24		K	11 63	DA 68	4-2
29681 29683	2048 x 8	24	715-1033	D	11 21	DA 7	4-6

Return Policy for Field Programmable Devices

Raytheon guarantees 95% field programming yields. Reject parts from lots that yield better than 95% will be accepted for replacement.

Reject lots and or rejects originating from lots yielding less than 95% will be analyzed and properly dispositioned for credit or replacement, at (Raytheon's Option), provided the conditions as stated herein are strictly followed.

Programming failures can be correctly evaluated and will be considered for credit or replacement only when **All** of the information requested below is supplied.

The units that are returned will be carefully examined and a programmability attempt (based on the availability of the master ROM) will be made before a credit or replacement order will be approved by Raytheon, except where it is found that failures where caused by:

a) Misuse
b) Incorrect Electrical Connections
c) Incorrect Programming Techniques
d) Physical Damage Caused by Poor Packaging Methods
e) Non-Random Array Content Verification

Units that are found to be programmable will be returned to the customer fully programmed as per master ROM supplied.

Units that are found to be unprogrammable will be destroyed and credit or replacement order at Raytheon's option, will be issued.

Units which are found to be unprogrammable because of damage or misuse by the customer will not be credited, but the devices will be marked and returned to the customer.

1. Customer _____

   Location _____

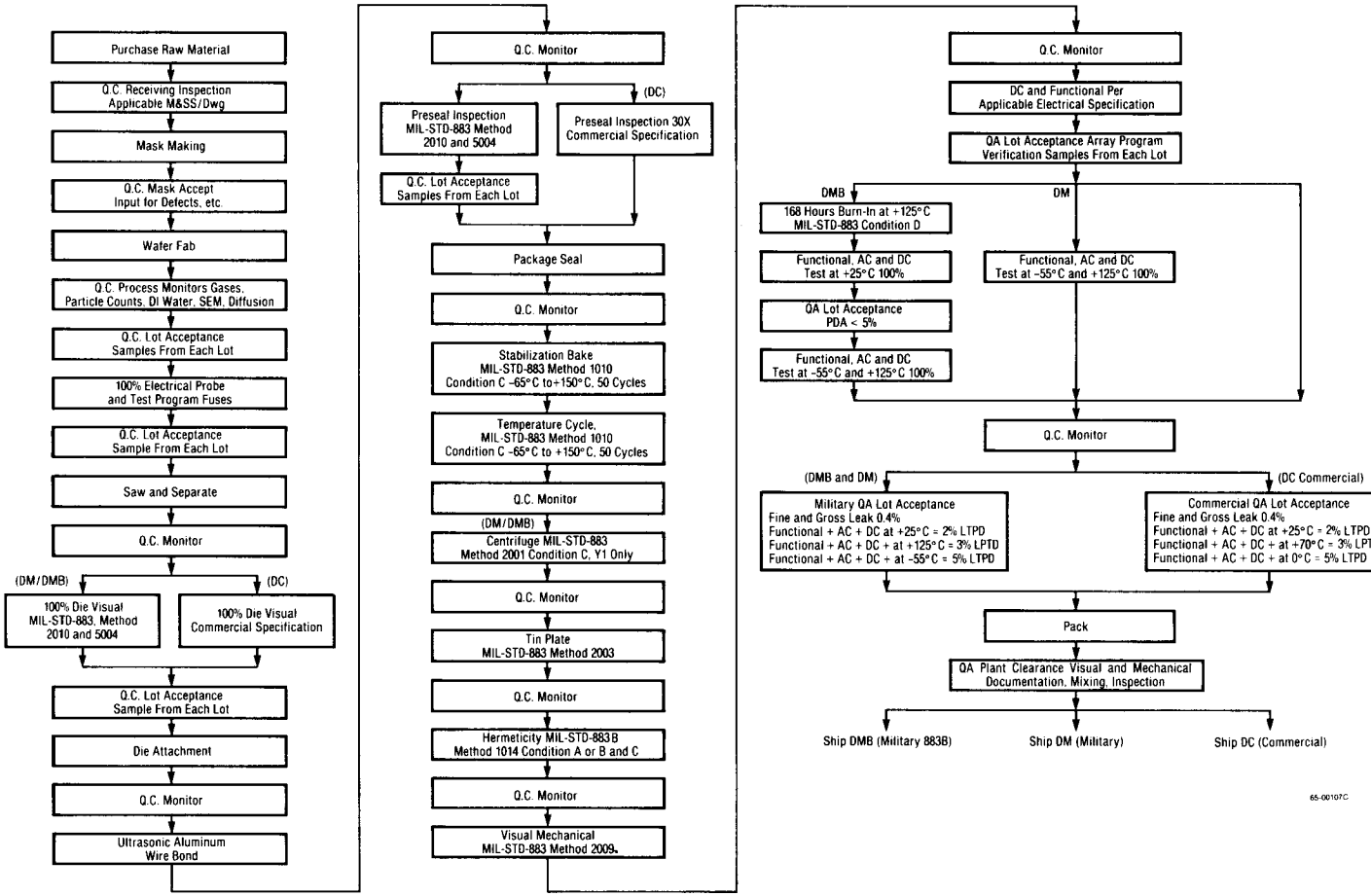
2. Purchase Order Number _____ Part Type _____

3. Quantity Programmed _____ Quantity Rejected _____

4. Programmer Type _____
   (Make, Model, Cardset, Etc)

5. Master ROM **Must Be** included with return.

Quality and Reliability Product Flow



Bipolar PROM/SPROM Cross Reference Guide

All Raytheon PROMs available as full military specification compliant.

No. of Bits	Org	Pkg	Output	Raytheon Part No.		Other Manufacturers												
				PROM	SPROM	AMD	Fairchild	Fujitsu	Harris	Hitachi	Intel	Intersil	MMI	National	NEC	Signetics	Supertex	T.I.
2K	512 x 4	16	TS			27S13	93446	MBM7053	7621			5624	5/6306	54S571		82S131		
					29613													
4K	512 x 8	20	TS	29621		27S29			7649				5/6349	54S472		82S147		TBP28S42
					29623													TBP28P42
8K	1024 x 8	24[1]	TS	29631		27S181	93451	MB7122/32	7681	HN20589	3628A		5/6381[1]	87S181		82S181	82S181	TBP28S86
				29631A[2]			93451									82HS181		
					29633											82PS181		TBP28P86
					29633A[2]													
8K	2048 x 4	18	TS	29651		27S185		MB7128	7685				5/6389	87S185		82S185		TBP24S81
				29651A[2]		27S185A							53/63S841			82S185		TBP24S81
					29653	27PS185												
					29653A[2]													
16K	2048 x 8	24[1]	TS	29681		27S191	93511	MB7138	76161	HN25169	3636		53/63S1681	87S191	μBP429	82S191	82S191	TBP28S166
				29681A[2]		27S191A	93511				3636B							
					29683	27PS191							53/63PS1681					TBP28P166
					29683A[2]													
					29683E[3]	27PS291												
32K	4096 x 8	24[1]	TS	29671		27S43		MB7142	76321		3632		53/63S3281	87S421		82S321		
				29671A[2]		27S43A								87S421				
					29673	27PS43												

Notes: 1. Available in 0.3 inch wide Slim-DIP package.
2. Speed Select.
3. Source Agreement with AMD.

512 × 4 SPROM — 29613/29613A

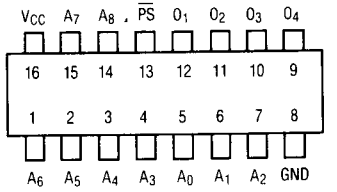
Power and AC Characteristics Over Operating Range (unless otherwise noted)

Parameter	Description	Test Conditions	Typical 5V +25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power Supply Current	(Disabled)	30	45	45	mA
		(Enabled)	90	130	130	
t_{AA}	Address Access Time	C_L = 30pF R_L = 300Ω to V_{CC}	35 (30)	60 (45)	75 (60)	nS
t_{EA}	Enable Access Time	and 600Ω to GND	40 (35)	60 (50)	75 (65)	nS
t_{ER}	Enable Recovery Time	(16mA Load) Note 1	15	30	40	nS

Notes: 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.
2. Numbers in parenthesis are for 29613A only.

Pin Out Information

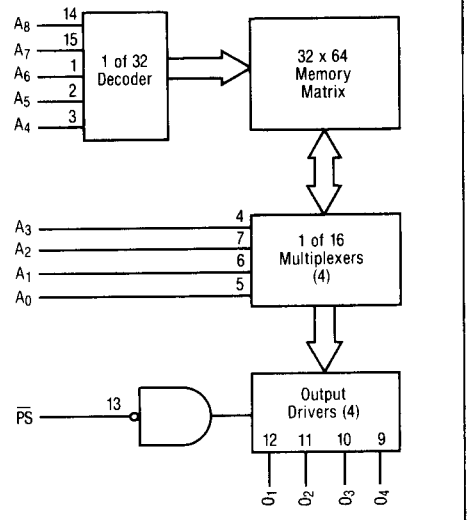
Dual-in-Line and Flat Packages



Pin 13 is also the programming pin (pp).

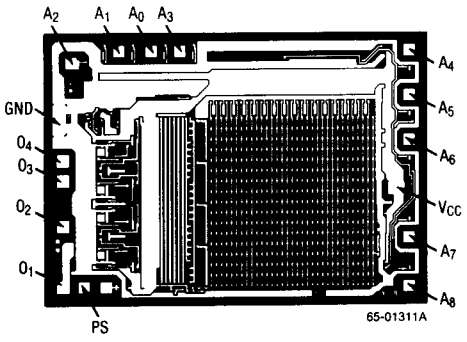
65-01312A

Block Diagram



65-00111A

Mask Pattern



65-01311A

Die Size: 87 x 122 mils
Min. Pad Dimensions: 4 x 4 mils

512 × 8 PROM — 29621/29621A

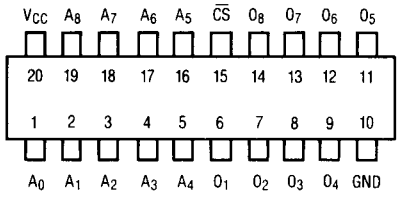
Power and AC Characteristics Over Operating Range (unless otherwise noted)

Parameter	Description	Test Conditions	Typical 5V +25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power Supply Current		90	155	155	mA
t_{AA}	Address Access Time	C_L = 30pF R_L = 300Ω to V_{CC}	50 (40)	65 (50)	80 (60)	nS
t_{EA}	Enable Access Time	and 600Ω to GND	20	30	40	nS
t_{ER}	Enable Recovery Time	(16mA Load) Note 1	20	30	40	nS

Notes: 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.
2. Numbers in parenthesis are for 29621A only.

Pin Out Information

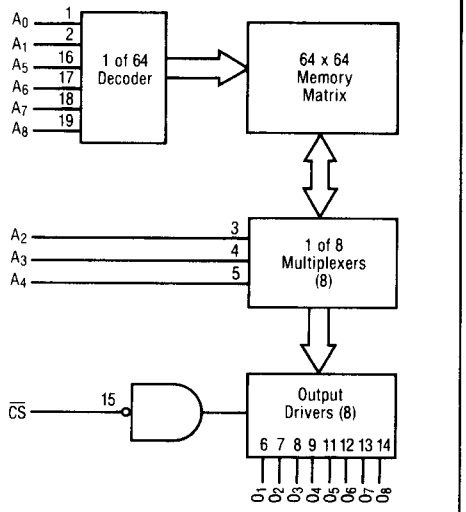
Dual-In-Line and Flat Packages



Pin 15 is also the programming pin (pp).

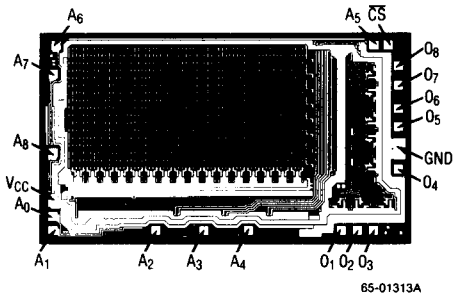
65-01314A

Block Diagram



65-00112A

Mask Pattern



65-01313A

Die Size: 93 x 163 mils
Min. Pad Dimensions: 4 x 4 mils

512 × 8 SPROM — 29623/29623A

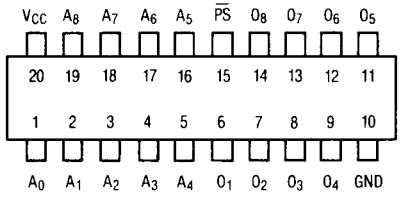
Power and AC Characteristics Over Operating Range (unless otherwise noted)

Parameter	Description	Test Conditions	Typical 5V +25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power Supply Current	(Disabled)	30	45	45	mA
		(Enabled)	90	155	155	
t_{AA}	Address Access Time	C_L = 30pF R_L = 300Ω to V_{CC}	55 (40)	70 (50)	85 (60)	nS
t_{EA}	Enable Access Time	and 600Ω to GND	55 (45)	70 (55)	85 (65)	nS
t_{ER}	Enable Recovery Time	(16mA Load) Note 1	20	30	40	nS

Notes: 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.
2. Numbers in parenthesis are for 29623A only.

Pin Out Information

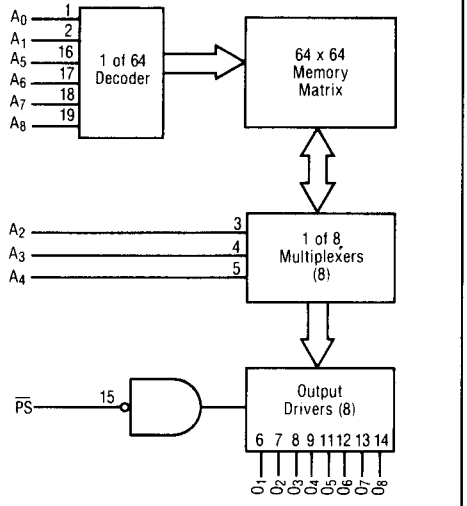
Dual-in-Line and Flat Packages



Pin 15 is also the programming pin (pp).

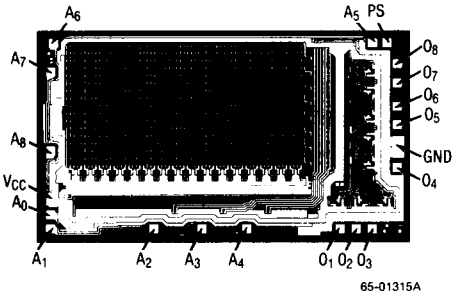
65-01316A

Block Diagram



65-00113A

Mask Pattern



65-01315A

Die Size: 93 x 163 mils
Min. Pad Dimensions: 4 x 4 mils

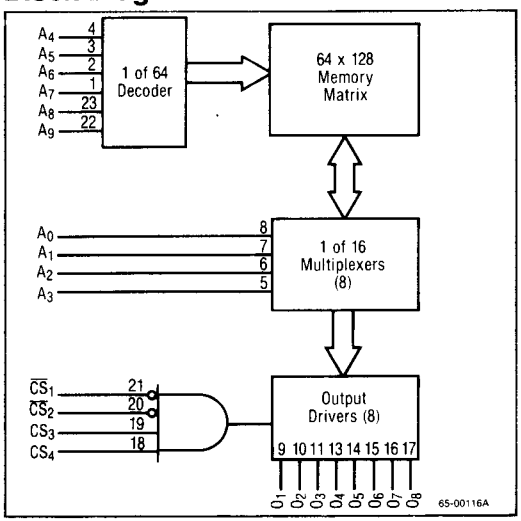
1024 × 8 PROM — 29631/29631A

Power and AC Characteristics Over Operating Range (unless otherwise noted)

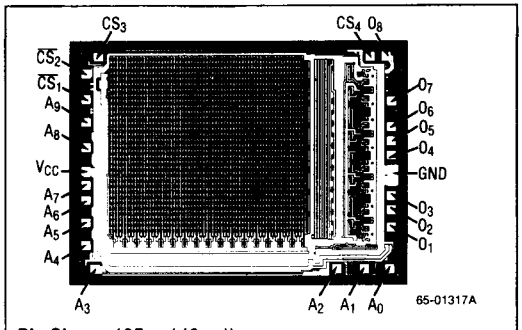
Parameter	Description	Test Conditions	Typical 5V +25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power Supply Current		120	170	170	mA
t_{AA}	Address Access Time	C_L = 30pF R_L = 300Ω to V_{CC}	45 (40)	70 (50)	90 (60)	nS
t_{EA}	Enable Access Time	and 600Ω to GND	20 (20)	30 (35)	40 (40)	nS
t_{ER}	Enable Recovery Time	(16mA Load) Note 1	15	30	40	nS

Notes: 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.
2. Numbers in parenthesis are for 29631A only.

Block Diagram



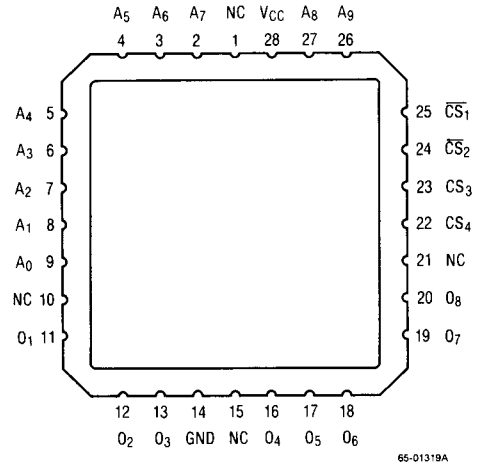
Mask Pattern



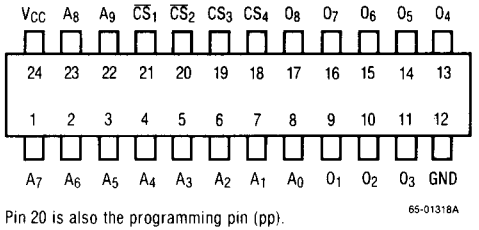
Die Size: 105 x 146 mils
Min. Pad Dimensions: 4 x 4 mils

Pin Out Information

Leadless Chip Carrier (28 Pin)



Dual-in-Line and Flat Packages



Pin 20 is also the programming pin (pp).

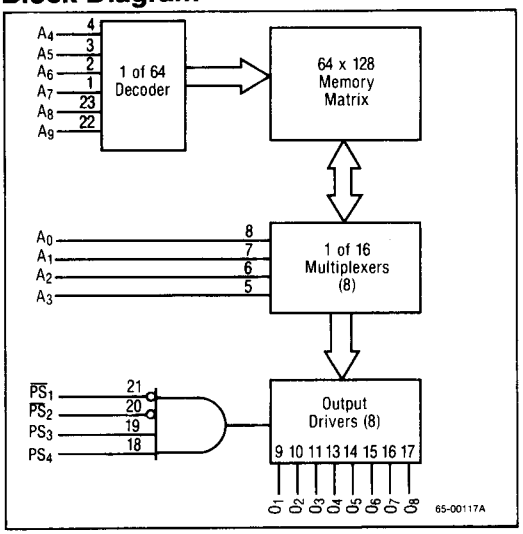
1024 × 8 PROM — 29633/29633A

Power and AC Characteristics Over Operating Range (unless otherwise noted)

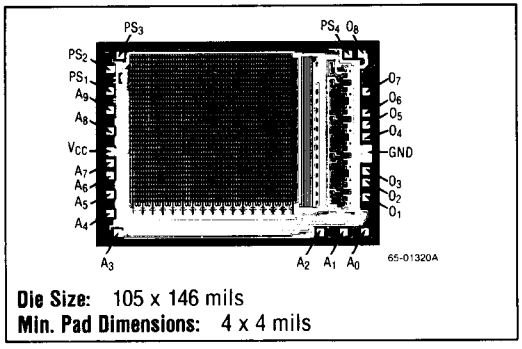
Parameter	Description	Test Conditions	Typical 5V +25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power Supply Current	Disabled	30	45	45	mA
		Enabled	110	170	170	
t_{AA}	Address Access Time	C_L = 30pF R_L = 300Ω to V_{CC}	50 (40)	70 (50)	90 (70)	nS
t_{EA}	Enable Access Time	and 600Ω to GND	50 (50)	75 (50)	115 (70)	nS
t_{ER}	Enable Recovery Time	(16mA Load) Note 1	15	30	40	nS

Notes: 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.
2. Numbers in parenthesis are for 29633A only.

Block Diagram



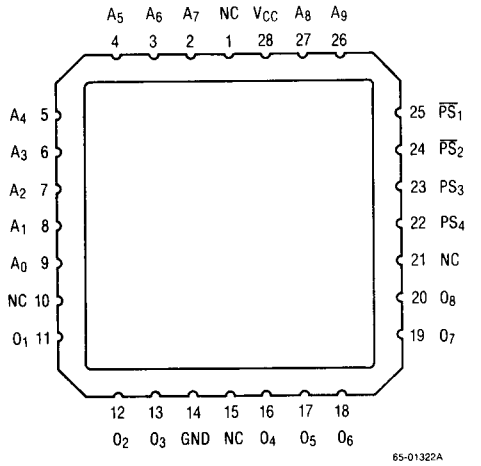
Mask Pattern



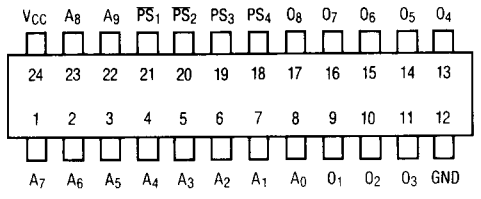
Die Size: 105 x 146 mils
Min. Pad Dimensions: 4 x 4 mils

Pin Out Information

Leadless Chip Carrier (28 Pin)



Dual-in-Line and Flat Packages



Pin 20 is also the programming pin (pp).

65-01321A

2048 × 4 PROM — 29651/29651A
Power and AC Characteristics Over Operating Range (unless otherwise noted)

Parameter	Description	Test Conditions	Typical 5V +25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power Supply Current		120	170	170	mA
t_{AA}	Address Access Time	C_L = 30pF R_L = 300Ω to V_{CC}	45 (35)	70 (60)	90 (70)	nS
t_{EA}	Enable Access Time	and 600Ω to GND	20 (15)	40 (35)	50 (45)	nS
t_{ER}	Enable Recovery Time	(16mA Load) Note 1	15	35	45	nS

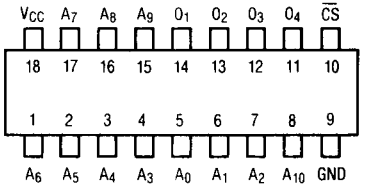
Notes: 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.
2. Numbers in parenthesis are for 29651A only.

Pin Out Information

Leadless Chip Carrier (28 Pin)

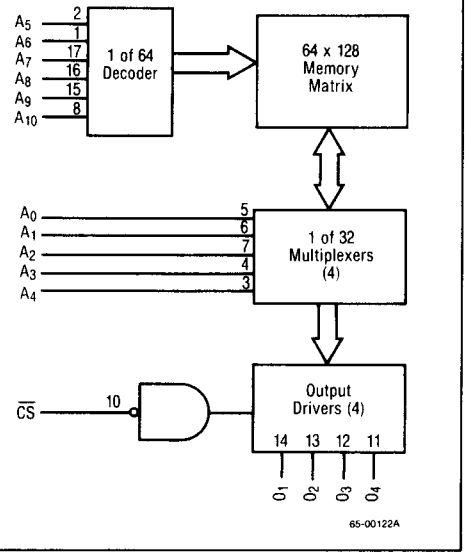
Contact Factory for Pin Out.

Dual-in-Line and Flat Packages

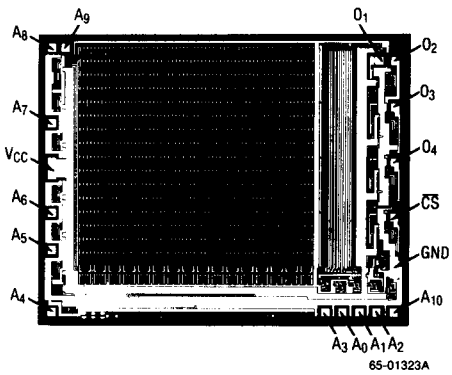


Pin 10 is also the programming pin (pp). 65-01324A

Block Diagram



Mask Pattern



Die Size: 127 x 161 mils
Min. Pad Dimensions: 4 x 4 mils

2048 × 4 SPROM — 29653/29653A
Power and AC Characteristics Over Operating Range (unless otherwise noted)

Parameter	Description	Test Conditions	Typical 5V +25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power Supply Current	Disabled	30	45	45	mA
		Enabled	110	170	170	
t_{AA}	Address Access Time	C_L = 30pF R_L = 300Ω to V_{CC} and 600Ω to GND (16mA Load) Note 1	50 (40)	75 (65)	90 (75)	nS
t_{EA}	Enable Access Time		50 (38)	80 (70)	95 (80)	nS
t_{ER}	Enable Recovery Time		15	35	45	nS

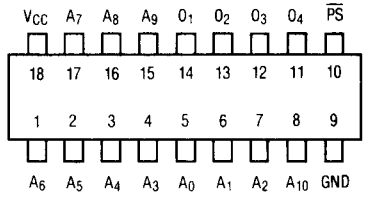
Notes: 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.
2. Numbers in parenthesis are for 29653A only.

Pin Out Information

Leadless Chip Carrier (28 Pin)

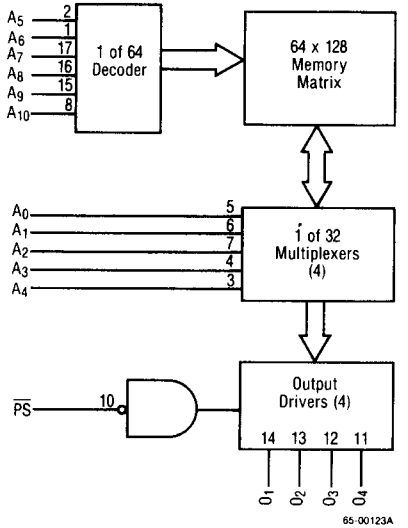
Contact Factory for Pin Out.

Dual-in-Line and Flat Packages

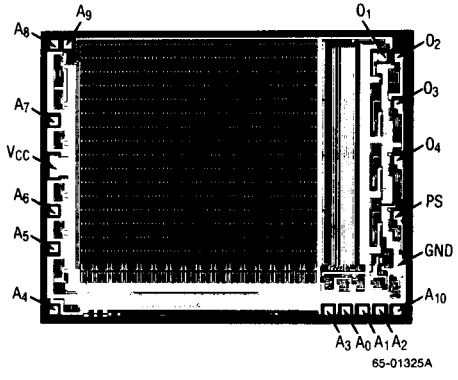


Pin 10 is also the programming pin (pp). 65-01326A

Block Diagram



Mask Pattern



Die Size: 127 x 161 mils
Min. Pad Dimensions: 4 x 4 mils

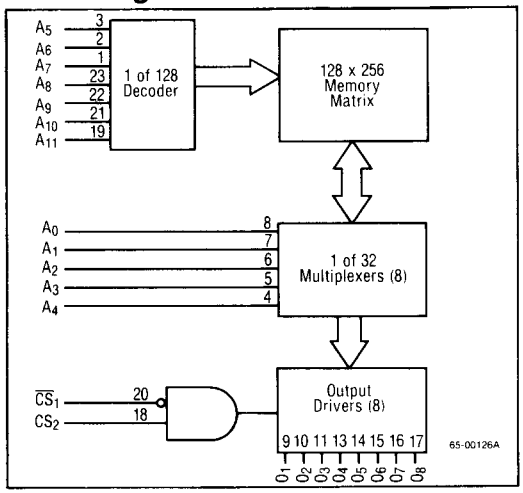
4096 × 8 PROM — 29671/29671A

Power and AC Characteristics Over Operating Range (unless otherwise noted)

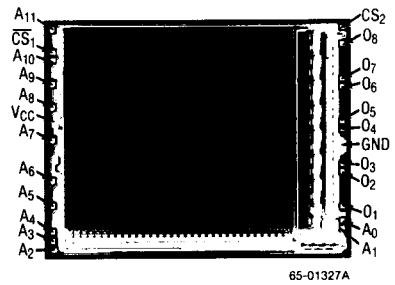
Parameter	Description	Test Conditions	Typical 5V +25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power Supply Current		150	195	195	mA
t_{AA}	Address Access Time	C_L = 30pF R_L = 300Ω to V_{CC}	50 (40)	80 (70)	100 (80)	nS
t_{EA}	Enable Access Time	and 600Ω to GND	30 (25)	40	50 (45)	nS
t_{ER}	Enable Recovery Time	(16mA Load) Note 1	25 (15)	40	45 (35)	nS

Notes: 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.
2. Numbers in parenthesis are for 29671A only.

Block Diagram



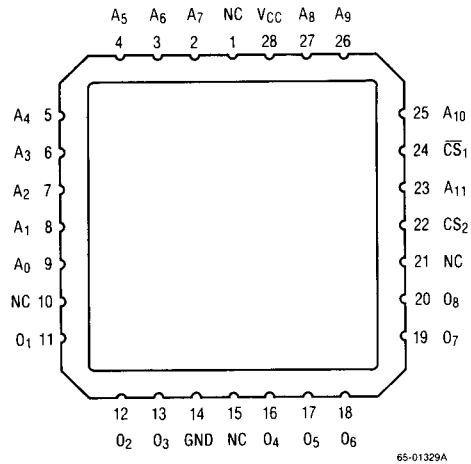
Mask Pattern



Die Size: 178 x 228 mils
Min. Pad Dimensions: 4 x 4 mils

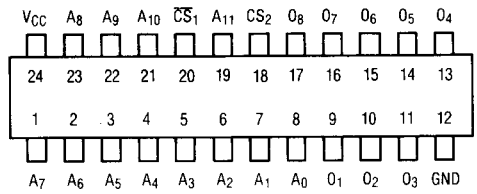
Pin Out Information

Leadless Chip Carrier (28 Pin)



Pin 24 is also the programming pin (pp).

0.6, 0.3 wide, Dual-in-Line and Flat Packages



Pin 20 is also the programming pin (pp).

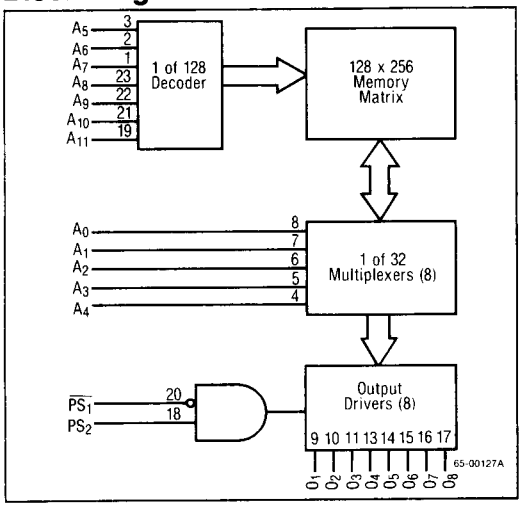
4096 × 8 SPROM — 29673

Power and AC Characteristics Over Operating Range (unless otherwise noted)

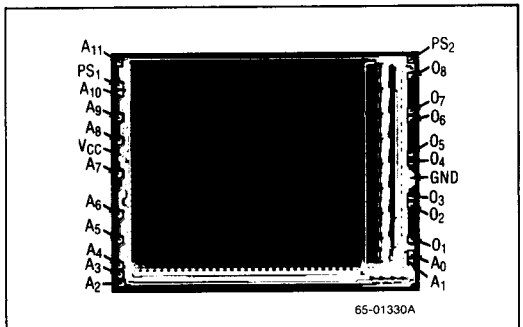
Parameter	Description	Test Conditions	Typical 5V +25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power Supply Current	Disabled	40	55	55	mA
		Enabled	150	195	195	
t_{AA}	Address Access Time	C_L = 30pF R_L = 300Ω to V_{CC} and 600Ω to GND (16mA Load) Note 1	55	85	105	nS
t_{EA}	Enable Access Time		55	95	125	nS
t_{ER}	Enable Recovery Time		35	45	50	nS

Notes: 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.

Block Diagram



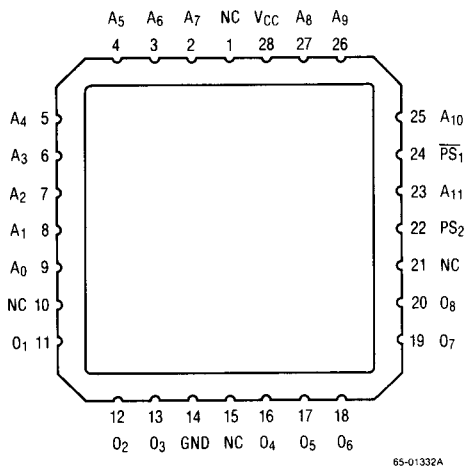
Mask Pattern



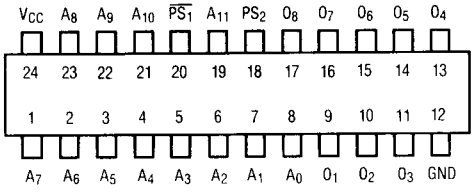
Die Size: 178 x 228 mils
Min. Pad Dimensions: 4 x 4 mils

Pin Out Information

Leadless Chip Carrier (28 Pin)



0.6, 0.3 wide, Dual-In-Line and Flat Packages



Pin 20 is also the programming pin (pp).

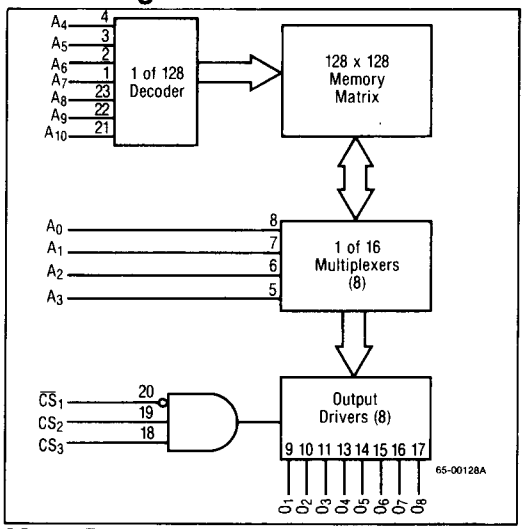
2048 × 8 PROM — 29681/29681A

Power and AC Characteristics Over Operating Range (unless otherwise noted)

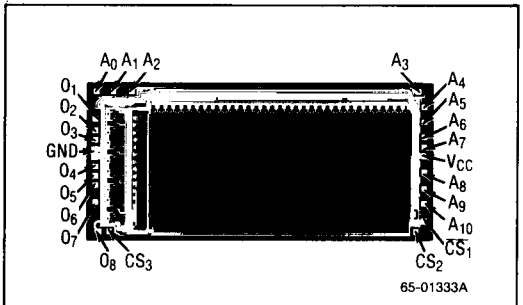
Parameter	Description	Test Conditions	Typical 5V +25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power Supply Current		125	180	180	mA
t_{AA}	Address Access Time	C_L = 30pF R_L = 300Ω to V_{CC}	50 (35)	80 (50	100 (70))	nS
t_{EA}	Enable Access Time	and 600Ω to GND	30 (25)	40 (35)	50 (45)	nS
t_{ER}	Enable Recovery Time	(16mA Load) Note 1	25 (15)	40 (30)	45 (35)	nS

Notes: 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.
2. Numbers in parenthesis are for 29681A only.

Block Diagram



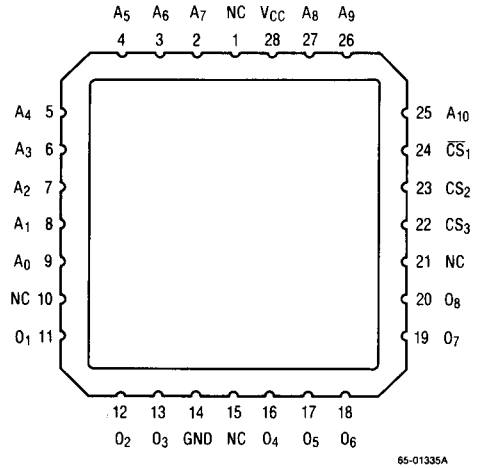
Mask Pattern



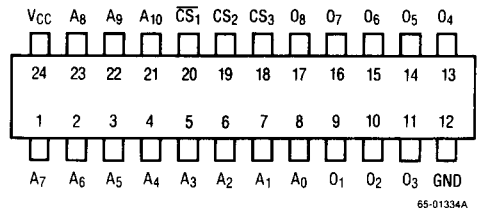
Die Size: 105 x 230 mils
Min. Pad Dimensions: 4 x 4 mils

Pin Out Information

Leadless Chip Carrier (28 Pin)



0.6, 0.3 wide, Dual-in-Line and Flat Packages



Pin 20 is also the programming pin (pp).

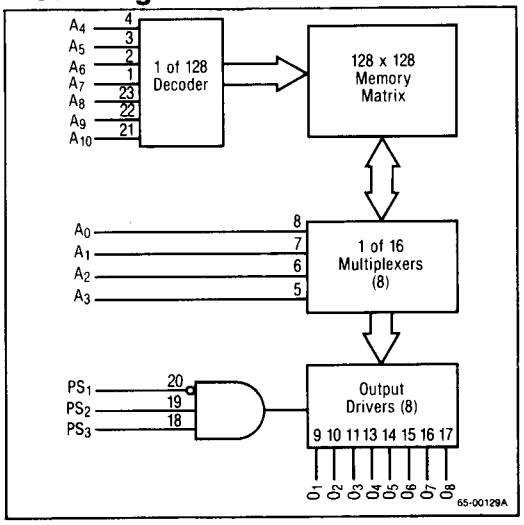
2048 × 8 SPROM — 29683/29683A

Power and AC Characteristics Over Operating Range (unless otherwise noted)

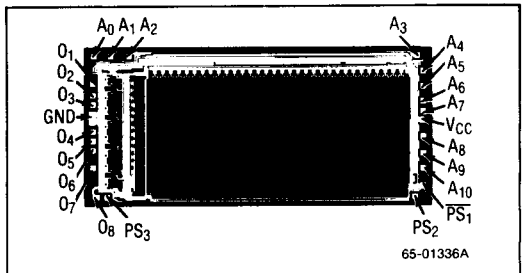
Parameter	Description	Test Conditions	Typical 5V +25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power Supply Current	Disabled	30	50	50	mA
		Enabled	125	180	180	
t_{AA}	Address Access Time	C_L = 30pF R_L = 300Ω to V_{CC}	55 (38)	85 (50)	105 (70)	nS
t_{EA}	Enable Access Time	and 600Ω to GND	55 (40)	85 (65)	105 (85)	nS
t_{ER}	Enable Recovery Time	(16mA Load) Note 1	35 (20)	45 (35)	50 (45)	nS

Notes: 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.
2. Numbers in parentheses are for the 29683A device only.

Block Diagram



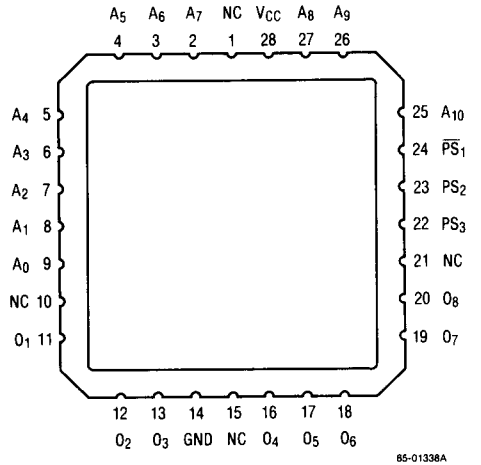
Mask Pattern



Die Size: 105 x 230
Min. Pad Dimensions: 4 x 4 mils

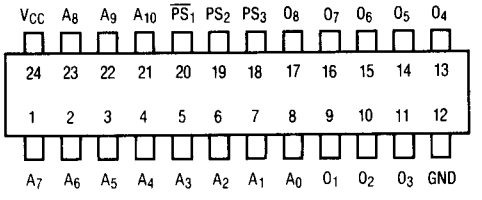
Pin Out Information

Leadless Chip Carrier (28 Pin)



Pin 24 is also the programming pin (pp).

0.6, 0.3 wide, Dual-In-Line and Flat Packages

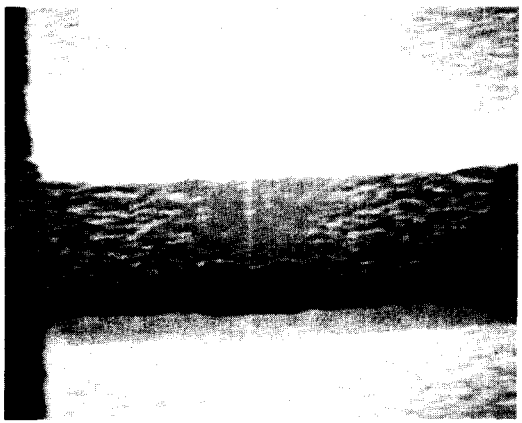


Pin 20 is also the programming pin (pp).

85-01337A

Operating Life Test Data

Device	Device Operating Hours	Number of Failures	Observed Failure Rate at %/1000 Hours $T_A = +125°C$	60% Confidence Failure Rate at %/1000 Hours $T_A = +125°C$	Estimated Failure Rate at %/1000 Hours $T_A = +70°C$
PROMs					
2K	860,000	0	0	0	0
4K	177,000	1	0.56%	0.7%	0.52%
8K	889,000	1	0.11%	0.14%	0.0011%
16K	674,000	1	0.14%	0.17%	0.0012%
32K	48,000	0	0	0	0
Fuses Reliability Data					
2K	1,761,280,000	0	$< 10^{-7}$	$< 10^{-7}$	$< 10^{-7}$
4K	724,992,000	0	$< 10^{-7}$	$< 10^{-7}$	$< 10^{-7}$
8K	7,282,688,000	0	$< 10^{-7}$	$< 10^{-7}$	$< 10^{-7}$
16K	11,370,496,000	0	$< 10^{-7}$	$< 10^{-7}$	$< 10^{-7}$
32K	1,502,864,000	0	$< 10^{-7}$	$< 10^{-7}$	$< 10^{-7}$



Programmed Fuse

Intact Fuse

High Speed, Low Power ROM Arrays Using Power Switched PROMs

Applications

These applications describe high speed PROM arrays that achieve significant power reduction through the use of a Raytheon chip select power switched PROM (SPROM).

1 Watt 55nS 8K × 8 PROM Array

Figure 5 shows a high speed low power 8K × 8 PROM array using two 4K × 8 SPROMs (29673).

The unique feature of this application is the use of the internal chip select logic to eliminate any extra decoders or gates in expanding the 4K word 29673 (12-bit address) into the 8K word array (13-bit address). As the power enabling chip select speed is comparable to the address delay there is no speed loss using this technique. In fact it is considerably faster than using an extra decoder and power supply switching transistor.

1 Watt 50nS 4K × 8 SPROM Array

Figure 6 shows a high speed low power 4K × 8 PROM array using four 1K × 8 SPROMs (29633).

The unique feature of this application is the use of the internal chip select logic to eliminate any extra decoders or gates in expanding the 1K word 29633 (10-bit address) into the 4K word array (12-bit address). As the power enabling chip select speed is comparable to the address delay there is no speed loss using this technique. In fact it is considerably faster than using an extra decoder and power supply switching transistor.

An additional benefit of this method of word expansion with SPROMs is the automatic "power off" of the de-selected PROMs without using any extra Power transistors or their decoder drivers and the elimination of any power required to drive them.

All 12 address lines are balanced with 4 loads each. To achieve the proper decoding using the chip select inputs the proper unused chip select inputs must be connected either to ground or to V_{CC} as required by their logical inputs.

The power savings of this structure over standard PROMs is significant. A SPROM when de-selected typically consumes ~25% of the power of a standard PROM or selected SPROM. The power consumed by this SPROM array is the power of one enabled or selected SPROM (typically 700mW) plus the power of three disabled or de-selected SPROMs (150mW each) for a total of 1150mW. This compares with 4 full power PROMs (typically 700mW each) for 2.8 Watts or guaranteed power savings of 75% (maximum ratings reflect a greater power savings).

2.8 Watts 65nS 8K × 16 PROM Array

Figure 7 shows an 8K × 16 PROM array that achieves a significant power savings by two methods.

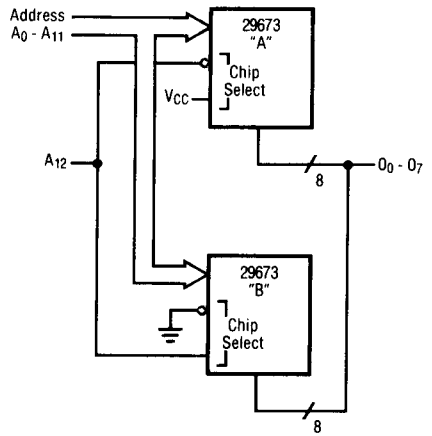
First, the expansion of the 2K word 29653 SPROM (2K × 4) to 8K words is accomplished by use of a 2-line to 4-line decoder. This device enables or selects only one fourth of the SPROMs at a time resulting in a power savings of about 50 to 60%. Expansion of the array to 16K words can be accomplished using only a 3-line to 8-line decoder in place of the 2 to 4 with a total power savings greater than 65%.

Second, the system clock or processor read enable is connected to the decoder chip "enable" or "data" input. This permits the entire PROM array to be disabled when not required.

The speed of the expansion address inputs is slightly slower than the direct address inputs as the additional delay of the decoder chip/IC is added to the delay of the SPROM power switched chip select. Use of the very high speed version of the 2K × 4 SPROMs can achieve a better than 90nS address or array enable to output delay over full military power supply and temperature variations. The system power is 4 enabled devices (typically 550mW) for 2.2 watts plus 12 disabled devices (typically 150mW) for a total selected power of 2.2W + 1.8 = 4 watts. Totally disabled the array power is typically 2.4 watts.

By use of the systems clock or memory select enable the typical operating system power can be reduced to 3.2 watts for a 50% duty cycle and 2.8 watts for a 25% duty cycle.

These two SPROM arrays point out the power saving capability of the internally power switched PROM. They achieve lower array power than obtainable with low power devices while maintaining the speed performance of the standard power units. Both of these arrays can be expanded to further improve power savings over conventional PROMs.

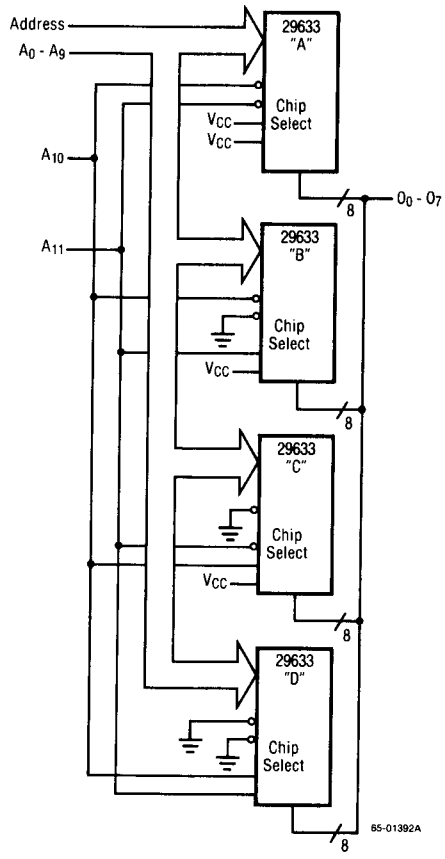


A_{12}	29673 Activated
Low	"A"
High	"B"

Typical Access Time = 55nS

Typical Power Dissipation, Without Power Switching
2 devices x 750mW/device = 1.5 Watts
Typical Power Dissipation, With Power Switching
1 device x 750mW/device + 1 device x 200mW/device = 0.95 Watts
power savings ~ 37%

Figure 5. High Speed, Low Power 8K × 8 PROM Array Using 4K × 8 SPROMs (Raytheon 29673)

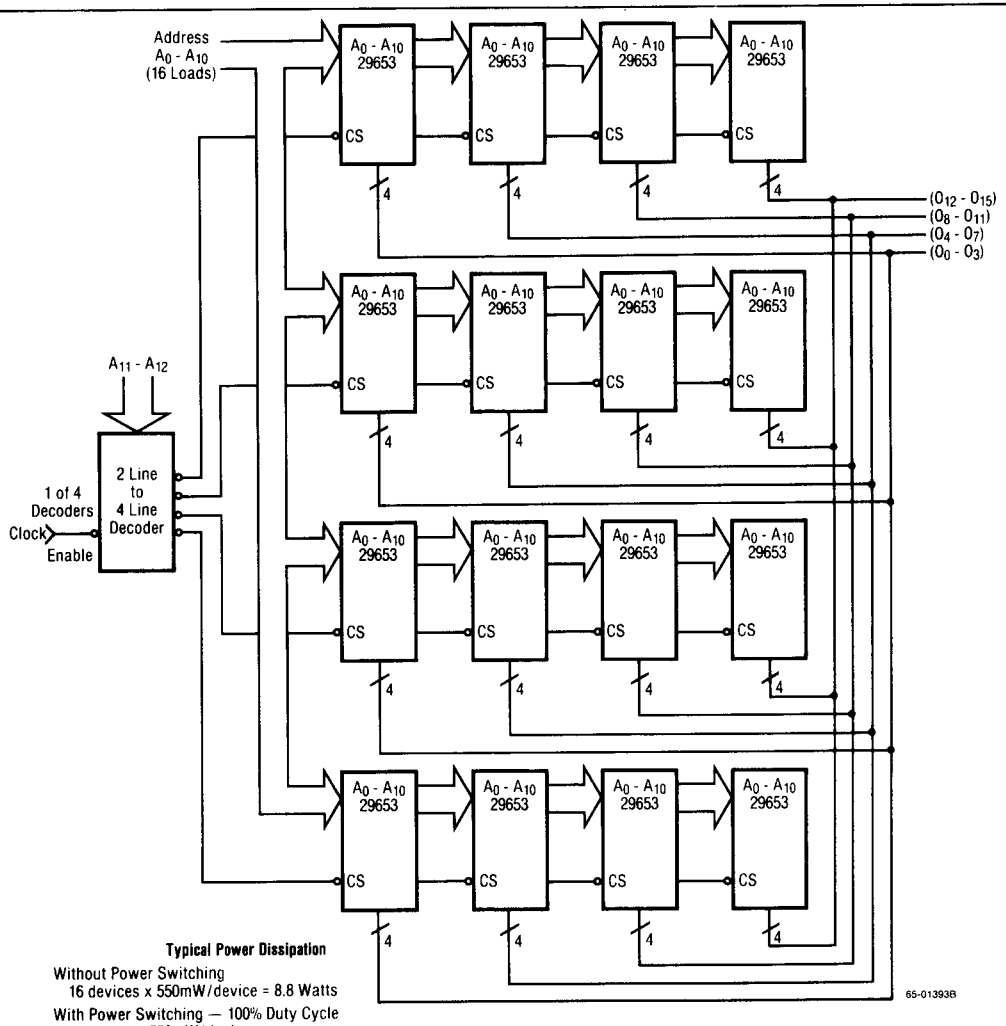


A_{10}	A_{11}	29633 Activated
Low	Low	"A"
Low	High	"B"
High	Low	"C"
High	High	"D"

Typical Access Time = 50nS

Typical Power Dissipation, Without Power Switching
4 devices x 700mW/device = 2.8 Watts
Typical Power Dissipation, With Power Switching
1 device x 700mW/device + 3 devices x 150mW/device = 1.150 Watts
power savings ~ 75%

Figure 6. High Speed, Low Power 4K × 8 PROM Array Example Using 1K × 8 SPROMs (Raytheon 29633)



Typical Power Dissipation

Without Power Switching
16 devices x 550mW/device = 8.8 Watts

With Power Switching — 100% Duty Cycle
4 devices x 550mW/device
+ 12 devices x 550mW/device
= 4 Watts

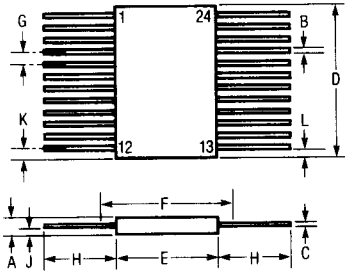
50% Clock with Power Switching — 50% Clock Duty Cycle
4 devices x 550mW/device x 50%
+ 4 devices x 150mW/device x 50%
+ 12 devices x 150mW/device
= 3.2 Watts

25% with Power Switching — 25% Clock Duty Cycle
4 devices x 550mW/device x 25%
+ 4 devices x 150mW/device x 25%
+ 12 devices x 150mW/device
= 2.8 Watts

Figure 7. 8K × 16 Low Power, High Speed, Clocked PROM Array Using 2K × 4 SPROMs (Raytheon 29653)

Packaging Information

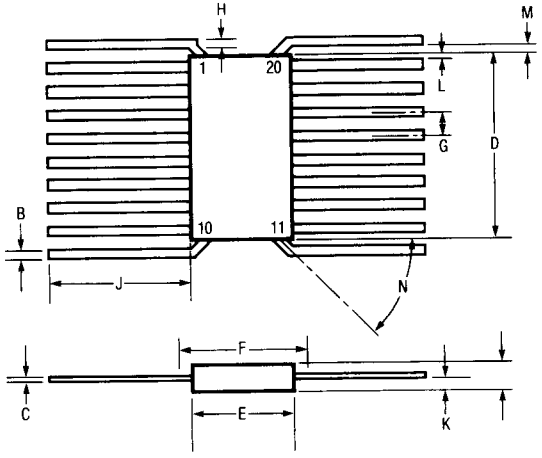
24-Lead Ceramic Flat Package



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	.045	.090	1.14	2.29
B	.015	.019	.38	.48
C	.003	.006	.08	.15
D		.640		16.26
E	.360	.420	9.14	10.67
F		.440		11.18
G	.050 BSC		1.27 BSC	
H	.250	.370	6.35	9.40
J	.010	.040	.25	1.02
K		.045		1.14
L	.005		0.13	

65-01221B

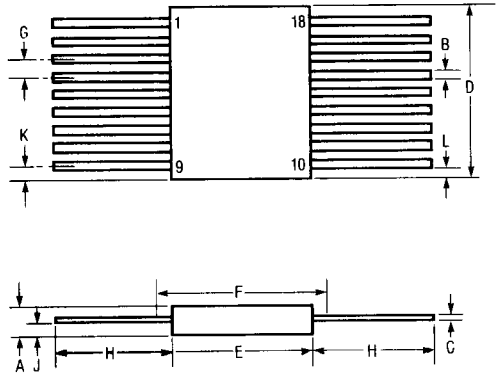
20-Lead Ceramic Flat Package



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	.045	.085	1.14	2.16
B	.015	.019	.38	.48
C	.003	.006	.08	.15
D		.440		11.18
E	.245	.285	6.22	7.24
F		.305		7.75
G	.050 BSC		1.27 BSC	
H	.008	.015	.20	.38
J	.250	.370	6.35	9.40
K	.010	.040	.25	1.02
L	.005		.13	
M	.004		.10	
N	30°	90°	30°	90°

65-01216B

18-Lead Ceramic Flat Package

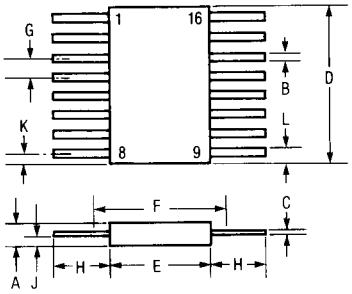


Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	.050	.085	1.27	2.16
B	.015	.019	.38	.48
C	.003	.006	.08	.15
D	.590	.625	14.41	15.88
E	.220	.310	5.95	7.87
F		.320		8.13
G	.050 BSC		1.27 BSC	
H	.330	.370	8.38	9.40
J	.020	.040	0.52	1.02
K	.060	.080	1.52	2.03
L		.060		1.52

65-01213B

Packaging Information (Continued)

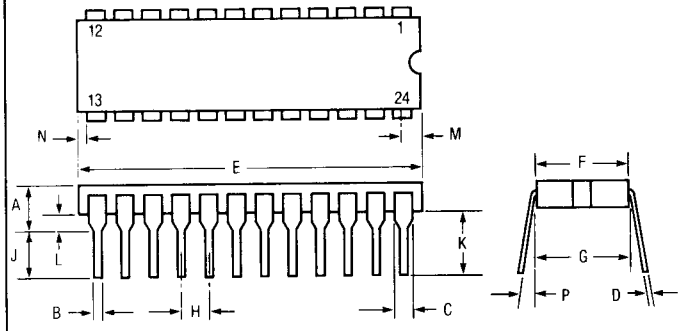
16-Lead
Ceramic Flat Package



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	.045	.085	1.14	2.16
B	.015	.019	.38	.48
C	.003	.006	.08	.15
D		.440		11.18
E	.245	.285	6.22	7.24
F		.305		7.75
G	.050 BSC		1.27 BSC	
H	.250	.370	6.35	9.40
J	.010	.040	.25	1.02
K		.045		1.14
L	.005		.13	

65-01210B

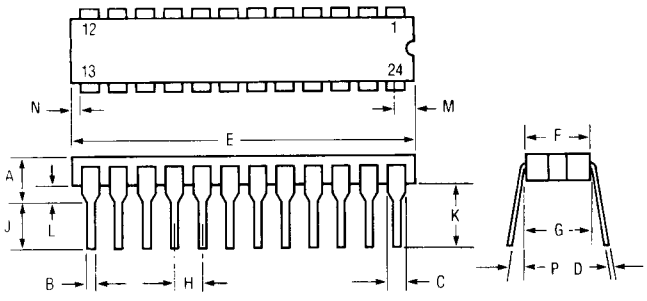
24-Lead
Ceramic Dual In-Line Package



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A		.225		5.72
B	.014	.023	.36	.58
C	.030	.070	.76	1.78
D	.008	.015	.20	.38
E		1.290		32.77
F	.500	.610	12.70	15.49
G	.590	.620	14.99	15.75
H	.100BSC		2.54BSC	
J	.120	.200	3.05	5.08
K	.150		3.81	
L	.015	.075	.38	1.91
M		.098		2.49
N	.005		.13	
P	0°	15°	0°	15°

65-01217B

24-Lead
Ceramic Dual In-Line Narrow Package

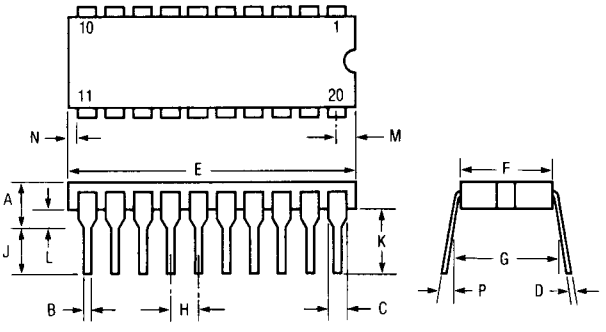


Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A		.225		5.72
B	.014	.023	.36	.58
C	.030	.070	.76	1.78
D	.008	.015	.20	.38
E		1.290		32.77
F		.302		7.67
G	.290	.320	7.37	8.13
H	.100BSC		2.54BSC	
J	.120	.200	3.05	5.08
K	.150		3.81	
L	.015	.075	.38	1.91
M		.098		2.49
N	.005		.13	
P	0°	15°	0°	15°

65-01219B

Packaging Information (Continued)

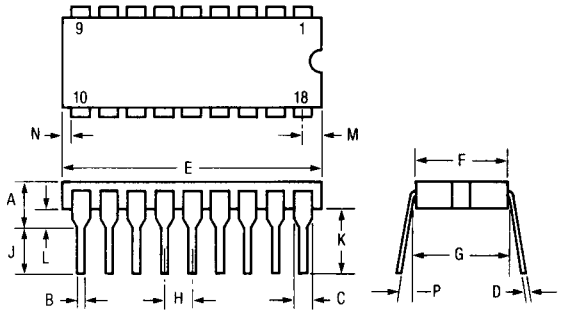
20-Lead
Ceramic Dual In-Line Package



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A		.200		5.08
B	.014	.023	.36	.58
C	.030	.070	.76	1.78
D	.008	.015	.20	.38
E	.930	.975	23.60	24.80
F	.220	.310	5.59	7.87
G	.290	.320	7.37	8.13
H	.100BSC		2.54BSC	
J	.120	.200	3.05	5.08
K	.150		3.81	
L	.015	.060	.38	1.52
M		.098	.38	2.49
N	.005		.13	2.49
P	0°	15°	0°	15°

65-01214B

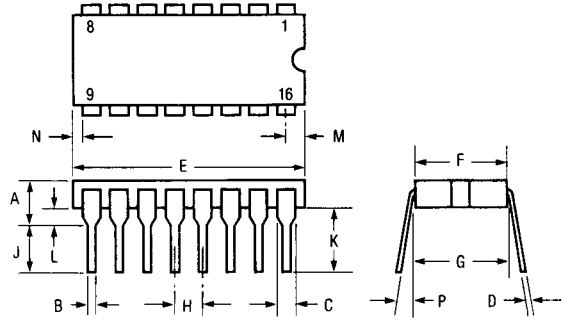
18-Lead
Ceramic Dual In-Line Package



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A		.200		5.08
B	.014	.023	.36	.58
C	.030	.070	.76	1.78
D	.008	.015	.20	.38
E		.940	23.90	23.90
F		.310		7.87
G	.290	.320	7.37	8.13
H	.100BSC		2.54BSC	
J	.120	.200	3.05	5.08
K	.150		3.81	
L	.015	.060	.38	1.52
M		.080	.38	2.03
N	.005		.13	
P	0°	15°	0°	15°

65-01211B

16-Lead
Ceramic Dual In-Line Package

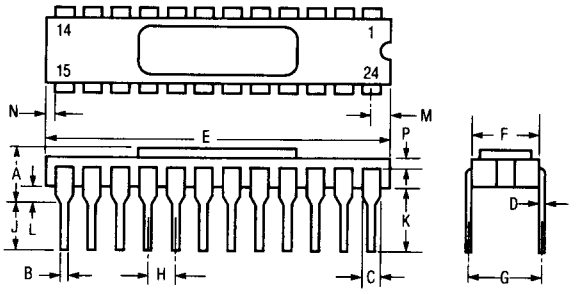


Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A		.200		5.08
B	.014	.023	.36	.58
C	.030	.070	.76	1.78
D	.008	.015	.20	.38
E		.840		21.34
F	.220	.310	5.59	7.87
G	.290	.320	7.37	8.13
H	.100BSC		2.54BSC	
J	.125	.200	3.18	5.08
K	.150		3.81	
L	.015	.060	.38	1.52
M		.080		2.03
N	.005		.13	
P	0°	15°	0°	15°

65-01208B

Packaging Information (Continued)

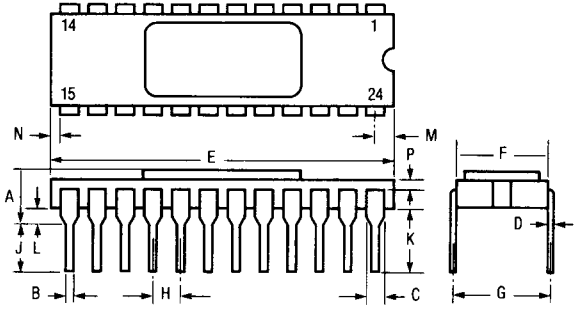
24-Lead
Ceramic Side-Brazed Dual In-Line Narrow Package



Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		0.200		5.08
B	0.015	0.021	0.38	0.53
C	0.045	0.060	1.14	1.52
D	0.008	0.012	0.20	0.31
E	1.180	1.220	29.97	31.01
F	0.290	0.320	14.73	15.49
G	0.280	0.310	14.73	15.75
H	0.100BSC		2.54BSC	
J	0.125		3.18	
K	0.150		3.05	5.08
L	0.030	0.070	0.76	1.78
M	0.030	0.065	0.76	1.65
N	0.005		0.13	
P	0.005		0.13	

65-01220B

24-Lead
Ceramic Side-Brazed Dual In-Line Package

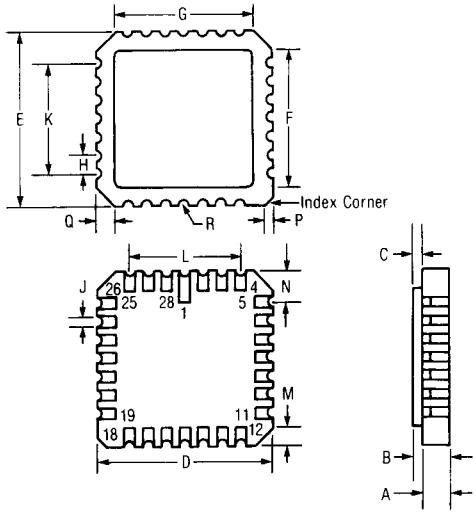


Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		0.200		5.08
B	0.015	0.023	0.38	0.58
C	0.045	0.060	1.14	1.52
D	0.008	0.012	0.20	0.31
E	1.150	1.220	29.20	31.01
F	0.580	0.610	7.11	7.87
G	0.580	0.620	7.37	8.13
H	0.100BSC		2.54BSC	
J	0.125		3.18	
K	0.150		3.05	5.08
L	0.015	0.060	0.38	1.52
M	0.030	0.065	0.76	1.65
N	0.005		0.13	
P	0.005		0.13	

65-01218B

Packaging Information (Continued)

LW 28-Pin
Leadless Chip Carrier Square



Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	0.017	0.066	0.43	1.68
B	0.064	0.100	1.62	2.54
C	0.007	0.075	0.18	1.91
D	0.442	0.458	11.23	11.63
E	0.442	0.458	11.23	11.63
F	0.370	0.400	9.40	10.16
G	0.370	0.400	9.40	10.16
H	0.050 BSC		1.27 BSC	
J	0.022	0.028	0.59	0.71
K	0.300		7.62	
L	0.300		7.62	
M	0.045	0.055	1.14	1.40
N	0.077	0.093	1.96	2.36
P	0.015	0.025	0.38	0.64
Q	0.040 BSC		1.02 BSC	
R	0.007	0.011	0.18	0.28

65-01231B

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6583