

## ILC5062

SOT-23 Power Supply reset Monitor  
With Complementary CMOS Output



### General Description

All-CMOS voltage monitoring circuit in a 3-lead SOT-23 package offers the best performance in power consumption and accuracy.

The ILC5062 is available in a series of  $\pm 1\%$  (A-grade) or 2% (standard grade) accurate trip voltages to fit most micro-processor applications. Even though its output can sink over 2mA, the device draws only 1 $\mu$ A in normal operation.

Additionally, a built-in hysteresis of 5% of detect voltage simplifies system design.

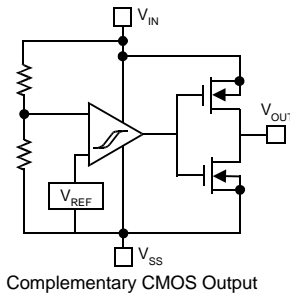
### Features

- All-CMOS design in SOT-23 package
- A grade  $\pm 1\%$  precision in Reset Detection
- Standard grade :  $\pm 2\%$  precision in Reset Detection
- Only 1 $\mu$ A of Iq
- Over 2mA of sink current capability
- Built-in hysteresis of 5% of detection voltage
- Voltage options of 2.6, 2.7, 2.8, 2.9, 3.1, 4.4, and 4.6V fit most supervisory applications

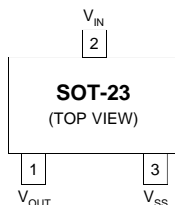
### Applications

- Microprocessor reset circuits
- Memory battery back-up circuitry
- Power-on reset circuits
- Portable and battery powered electronics

### Block Diagram



### Pin-Package Configurations



### Ordering Information

Ordering Information	
ILC5062AM-26	2.6V $\pm 1\%$ Monitor in SOT-23
ILC5062AM-27	2.7V $\pm 1\%$ Monitor in SOT-23
ILC5062AM-28	2.8V $\pm 1\%$ Monitor in SOT-23
ILC5062AM-29	2.9V $\pm 1\%$ Monitor in SOT-23
ILC5062AM-31	3.1V $\pm 1\%$ Monitor in SOT-23
ILC5062AM-44	4.4V $\pm 1\%$ Monitor in SOT-23
ILC5062AM-46	4.6V $\pm 1\%$ Monitor in SOT-23
ILC5062M-26	2.6V $\pm 2\%$ Monitor in SOT-23
ILC5062M-27	2.7V $\pm 2\%$ Monitor in SOT-23
ILC5062M-28	2.8V $\pm 2\%$ Monitor in SOT-23
ILC5062M-29	2.9V $\pm 2\%$ Monitor in SOT-23
ILC5062M-31	3.1V $\pm 2\%$ Monitor in SOT-23
ILC5062M-44	4.4V $\pm 2\%$ Monitor in SOT-23
ILC5062M-46	4.6V $\pm 2\%$ Monitor in SOT-23

\* Standard product offering comes in tape & reel, quantity 3000 per reel, orientation right

**Absolute Maximum Ratings ( $T_A=25^{\circ}\text{C}$ )**

Parameter	Symbol	Ratings	Units
Input Voltage	$V_{IN}$	12	V
Output Current	$I_{OUT}$	50	mA
Output Voltage	$V_{OUT}$	$V_{SS}-0.3\sim V_{IN}+0.3$	V
Continuous Total Power Dissipation (SOT-23)	$P_d$	150	mW
Operating Ambient Temperature	$T_{opr}$	-30~+80	$^{\circ}\text{C}$
Storage Temperature	$T_{stg}$	-40~+125	$^{\circ}\text{C}$

**Electrical Characteristics ILC5062 ( $T_A=25^{\circ}\text{C}$ )**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Detect Fail Voltage	$V_{DF}$	A grade	$V_{DF} \times 0.99$	$V_{DF}$	$V_{DF} \times 1.01$	V
Detect Fail Voltage	$V_{DF}$	Standard grade	$V_{DF} \times 0.98$	$V_{DF}$	$V_{DF} \times 1.02$	V
Hysteresis Range	$V_{HYS}$		$V_{DF} \times 0.02$	$V_{DF} \times 0.05$	$V_{DF} \times 0.08$	V
Supply Current	$I_{SS}$	$V_{IN} = 1.5\text{V}$ $V_{IN} = 2.0\text{V}$ $V_{IN} = 3.0\text{V}$ $V_{IN} = 4.0\text{V}$ $V_{IN} = 5.0\text{V}$		0.9 1.0 1.3 1.6 2.0	2.6 3.0 3.4 3.8 4.2	$\mu\text{A}$
Operating Voltage	$V_{IN}$	$V_{DF} = 2.1 \sim 6.0\text{V}$	1.5		10.0	V
Output Current	$I_{OUT}$	N-ch $V_{DS} = 0.5\text{V}$ $V_{IN} = 1.0\text{V}$ $V_{IN} = 2.0\text{V}$ $V_{IN} = 3.0\text{V}$ $V_{IN} = 4.0\text{V}$ $V_{IN} = 5.0\text{V}$  P-Ch $V_{DS} = 2.1\text{V}$ $V_{IN} = 8\text{V}$		2.2 7.7 10.1 11.5 13.0  -10		mA
Temperature Characteristics	$\Delta V_{DF}/(\Delta T_{opr} \cdot V_{DF})$	$-30^{\circ}\text{C} \leq T_{opr} \leq 80^{\circ}\text{C}$		$\pm 100$		ppm/ $^{\circ}\text{C}$
Delay Time (Release Voltage $\rightarrow$ Output Inversion)	$t_{DLY}$ ( $V_{DR} \rightarrow V_{OUT}$ Inversion)				0.2	ms

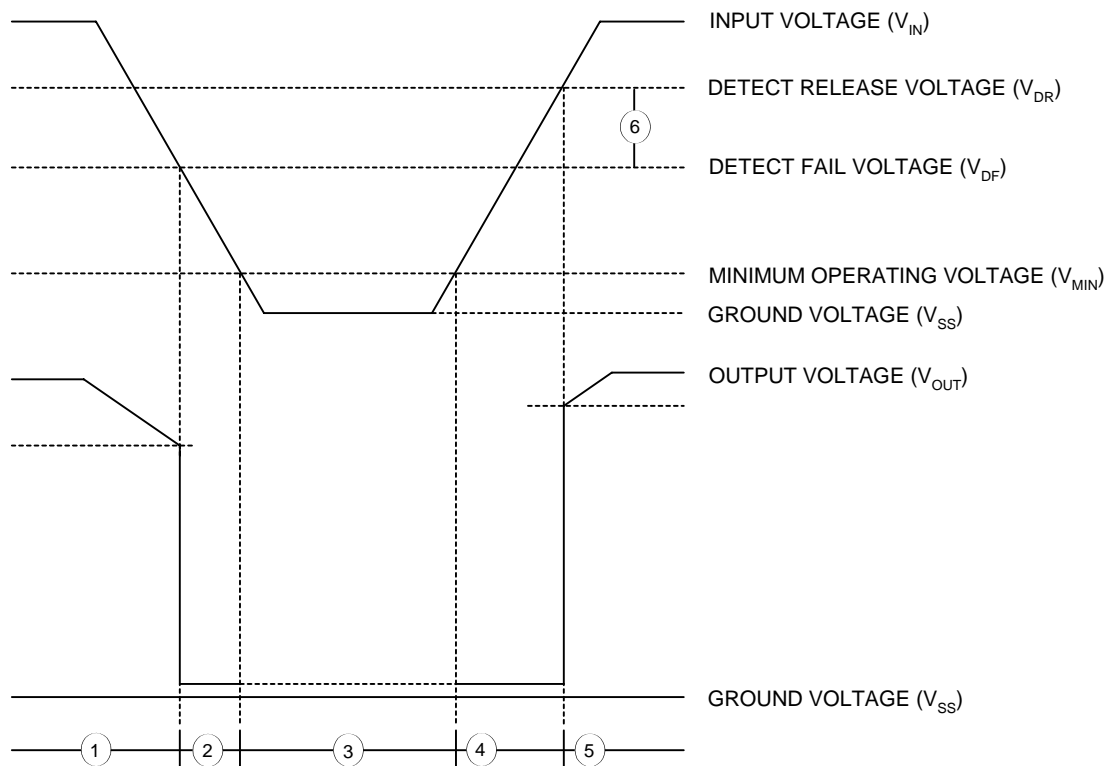
Note: An additional resistor between the  $V_{IN}$  pin and supply voltage may cause deterioration of the characteristics due to increasing of  $V_{DR}$ .

## Functional Description

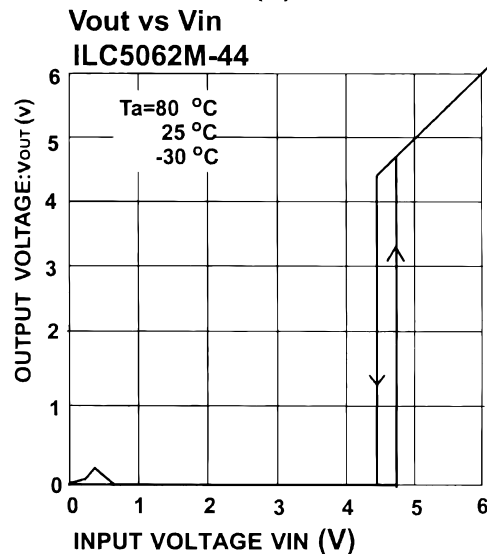
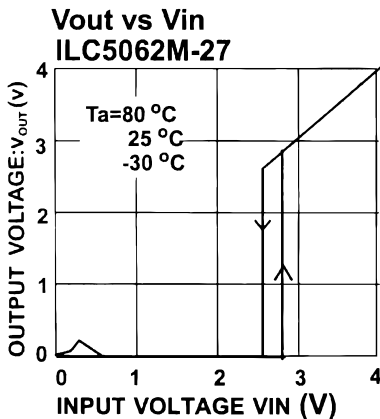
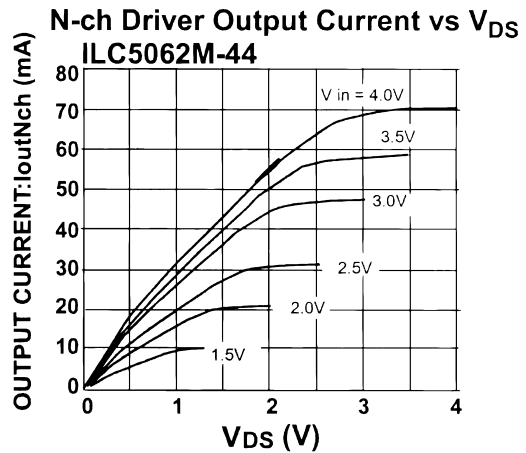
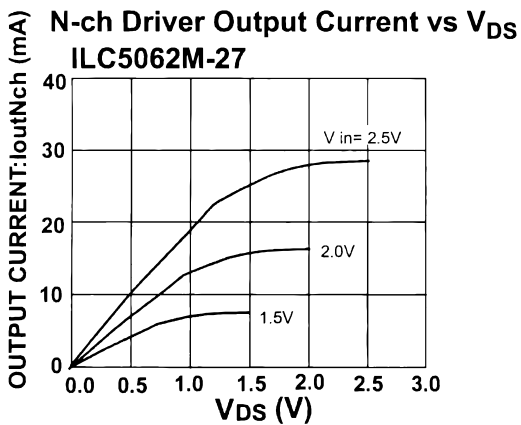
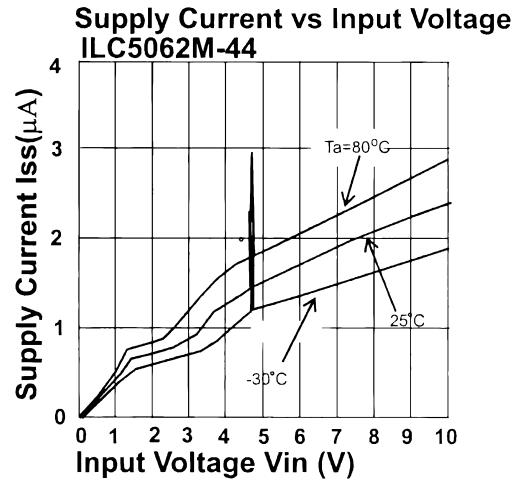
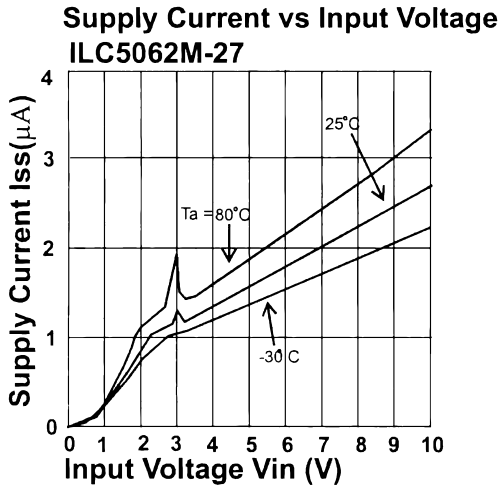
The following designators 1-6 refer to the timing diagram below.

1. While the input voltage ( $V_{IN}$ ) is higher than the detect voltage ( $V_{DF}$ ), the output voltage at  $V_{OUT}$  pin equals the input voltage at  $V_{IN}$  pin.
2. When the input  $V_{IN}$  voltage falls lower than  $V_{DF}$ ,  $V_{OUT}$  drops near ground voltage.
3. If the input voltage decreases below the minimum operating voltage ( $V_{MIN}$ ), the  $V_{OUT}$  output voltage will be undefined.
4. During an increase of the input voltage from the  $V_{SS}$  voltage,  $V_{OUT}$  is undefined at the voltage below  $V_{MIN}$ . Exceeding the  $V_{MIN}$  level, the output stays at the ground level ( $V_{SS}$ ) between the minimum operating voltage ( $V_{MIN}$ ) and the detect release voltage ( $V_{DR}$ ).
5. If the input voltage increases more than  $V_{DR}$ , the output voltage at  $V_{OUT}$  pin equals the input voltage at  $V_{IN}$  pin.
6. The difference between  $V_{DR}$  and  $V_{DF}$  is the hysteresis in the system.

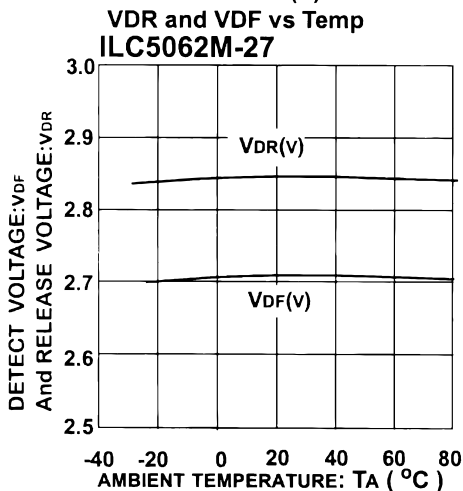
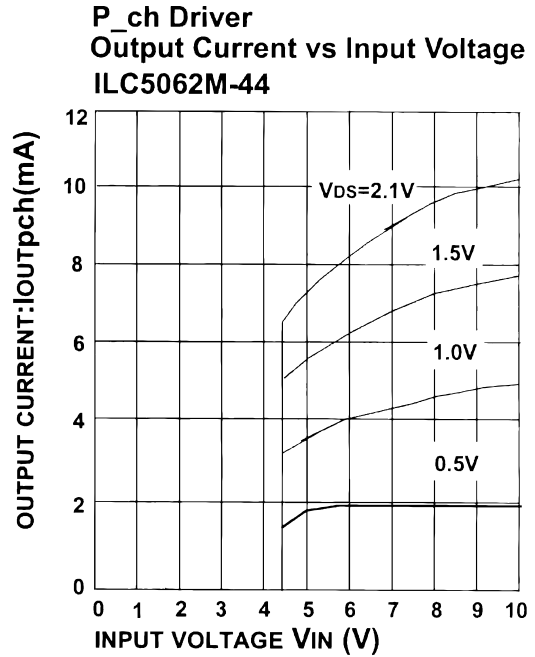
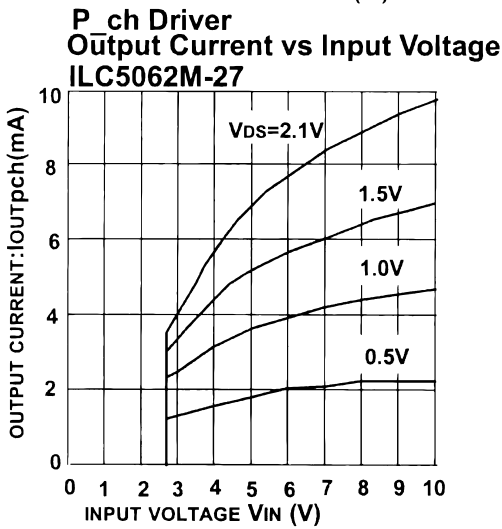
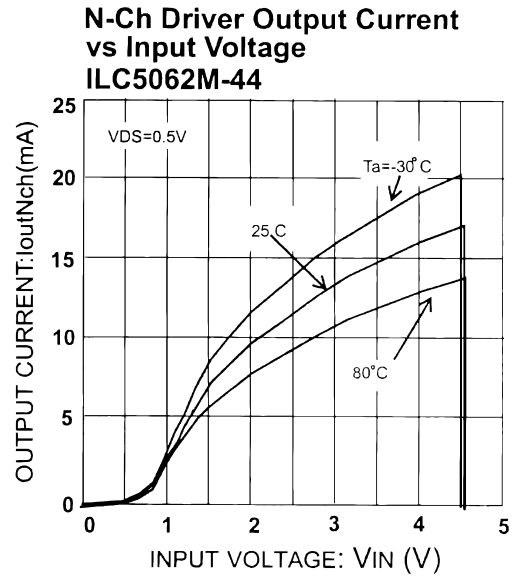
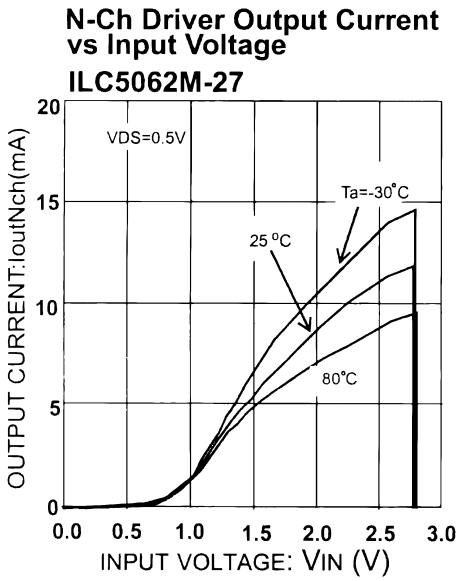
## Timing Diagram



Typical Performance Characteristics - general conditions for all curves.



Typical Performance Characteristics - general conditions for all curves.



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