



## N-Channel Depletion-Mode Vertical DMOS FETs

### Ordering Information

BV <sub>DSX</sub> / BV <sub>DGX</sub>	R <sub>DS(ON)</sub> (max)	I <sub>DSS</sub> (min)	Order Number / Package	
			TO-243AA*	Die**
250V	6.0Ω	300mA	DN3525N8	DN3525NW

Product marking for TO-243AA:

**DN5C\***

Where \* = 2-week alpha date code

\* Same as SOT-89. Products shipped on 2000 piece carrier tape reels.

\*\* Die in wafer form.

### Features

- High input impedance
- Low input capacitance
- Fast switching speeds
- Low on resistance
- Free from secondary breakdown
- Low input and output leakage

### Applications

- Normally-on switches
- Solid state relays
- Converters
- Linear amplifiers
- Constant current sources
- Power supply circuits
- Telecom

### Absolute Maximum Ratings

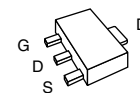
Drain-to-Source Voltage	BV <sub>DSX</sub>
Drain-to-Gate Voltage	BV <sub>DGX</sub>
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C

### Advanced DMOS Technology

These low threshold depletion-mode (normally-on) transistors utilize an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Package Options



TO-243AA  
(SOT-89)

Note: See Package Outline section for dimensions.

## Thermal Characteristics

Package	$I_D$ (continuous)*	$I_D$ (pulsed)	Power Dissipation @ $T_A = 25^\circ\text{C}$	$\theta_{jc}$ $^\circ\text{C/W}$	$\theta_{ja}$ $^\circ\text{C/W}$	$I_{DR}^*$	$I_{DRM}$
TO-243AA	360mA	600mA	1.6W <sup>†</sup>	15	78 <sup>†</sup>	360mA	600mA

\*  $I_D$  (continuous) is limited by max rated  $T_j$ .

<sup>†</sup> Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant  $P_D$  increase possible on ceramic substrate.

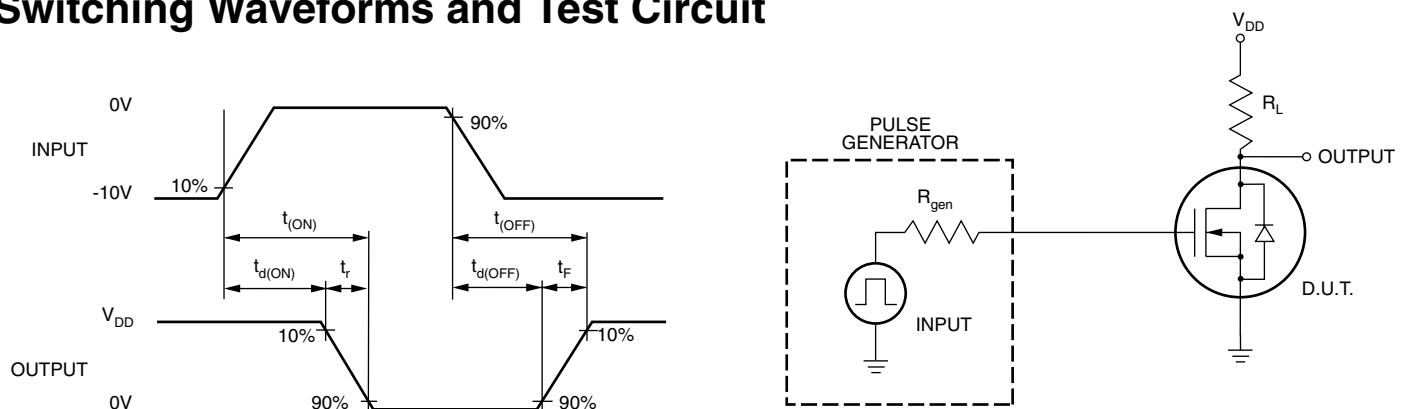
## Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$BV_{DSX}$	Drain-to-Source Breakdown Voltage	250			V	$V_{GS} = -5.0\text{V}$ , $I_D = 100\mu\text{A}$
$V_{GS(OFF)}$	Gate-to-Source OFF Voltage	-1.5		-3.5	V	$V_{DS} = 15\text{V}$ , $I_D = 1.0\text{mA}$
$\Delta V_{GS(OFF)}$	Change in $V_{GS(OFF)}$ with Temperature			4.5	mV/ $^\circ\text{C}$	$V_{DS} = 15\text{V}$ , $I_D = 1.0\text{mA}$
$I_{GSS}$	Gate Body Leakage Current			100	nA	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$
$I_{D(OFF)}$	Drain-to-Source Leakage Current			1.0	$\mu\text{A}$	$V_{GS} = -5.0\text{V}$ , $V_{DS} = \text{Max Rating}$
				1.0	mA	$V_{GS} = -5.0\text{V}$ , $V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{DSS}$	Saturated Drain-to-Source Current	300			mA	$V_{GS} = 0\text{V}$ , $V_{DS} = 15\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			6.0	$\Omega$	$V_{GS} = 0\text{V}$ , $I_D = 200\text{mA}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.1	%/ $^\circ\text{C}$	$V_{GS} = 0\text{V}$ , $I_D = 200\text{mA}$
$G_{FS}$	Forward Transconductance	225			m $\bar{S}$	$I_D = 150\text{mA}$ , $V_{DS} = 10\text{V}$
$C_{ISS}$	Input Capacitance		270	350	pF	$V_{GS} = -5.0\text{V}$ , $V_{DS} = 25\text{V}$ , $f = 1.0\text{MHz}$
$C_{OSS}$	Common Source Output Capacitance		20	60		
$C_{RSS}$	Reverse Transfer Capacitance		5.0	20		
$t_{d(ON)}$	Turn-ON Delay Time			20	ns	$V_{DD} = 25\text{V}$ , $I_D = 150\text{mA}$ , $R_{GEN} = 25\Omega$ , $V_{GS} = 0\text{V to } -10\text{V}$
$t_r$	Rise Time			25		
$t_{d(OFF)}$	Turn-OFF Delay Time			25		
$t_f$	Fall Time			40		
$V_{SD}$	Diode Forward Voltage Drop			1.8	V	$V_{GS} = -5.0\text{V}$ , $I_{SD} = 150\text{mA}$
$t_{rr}$	Reverse Recovery Time		800		ns	$V_{GS} = -5.0\text{V}$ , $I_{SD} = 150\text{mA}$

### Notes:

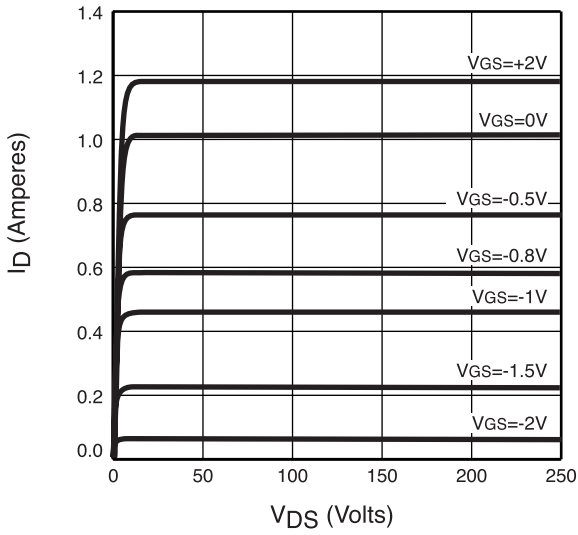
- All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 $\mu\text{s}$  pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit

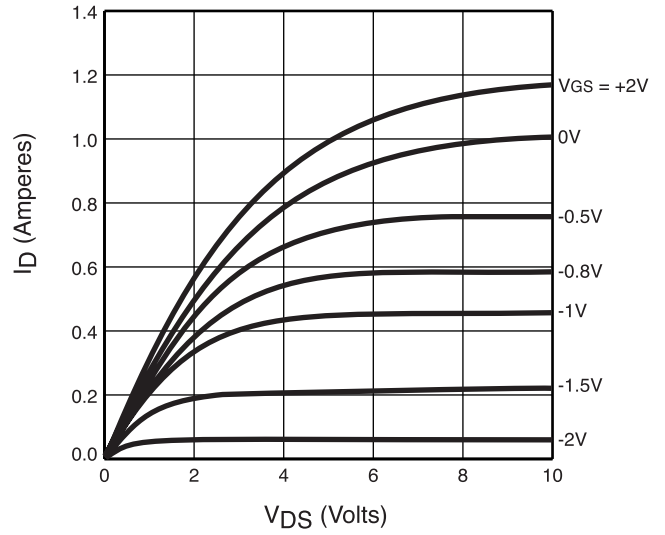


# Typical Performance Curves

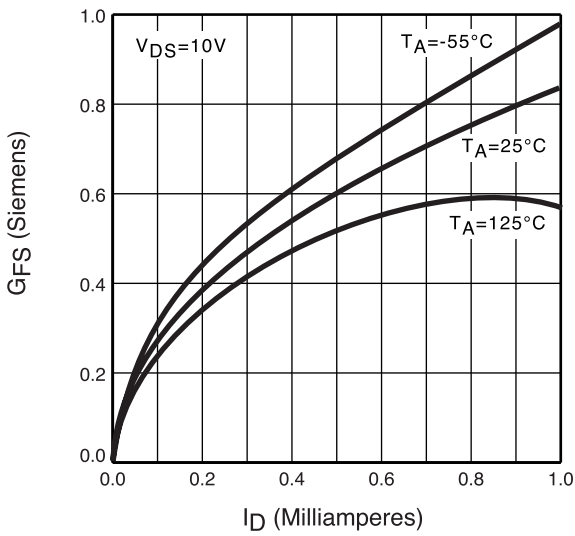
Output Characteristics



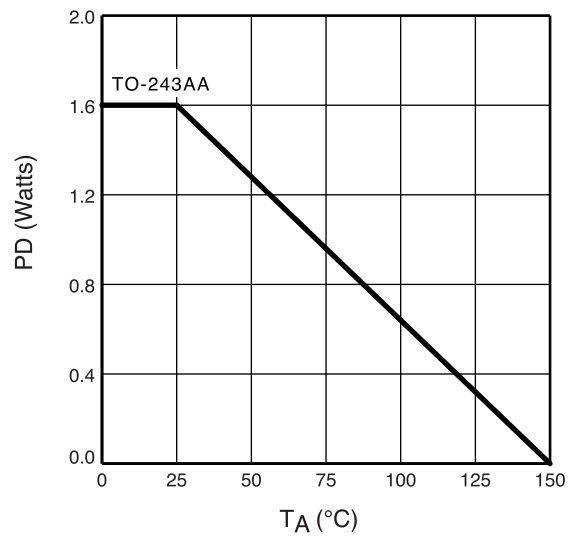
Saturation Characteristics



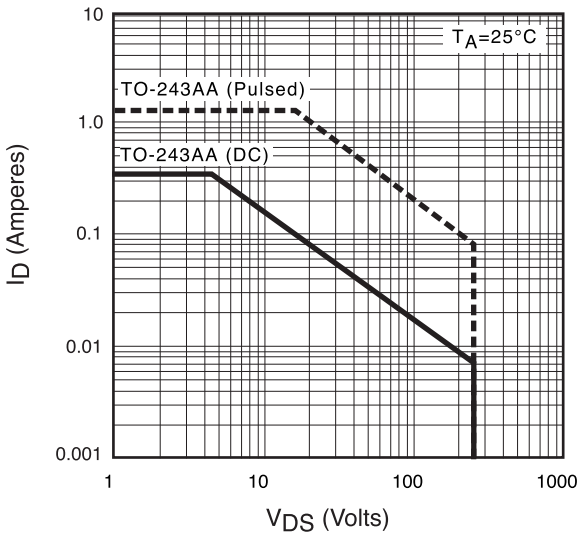
Transconductance vs. Drain Current



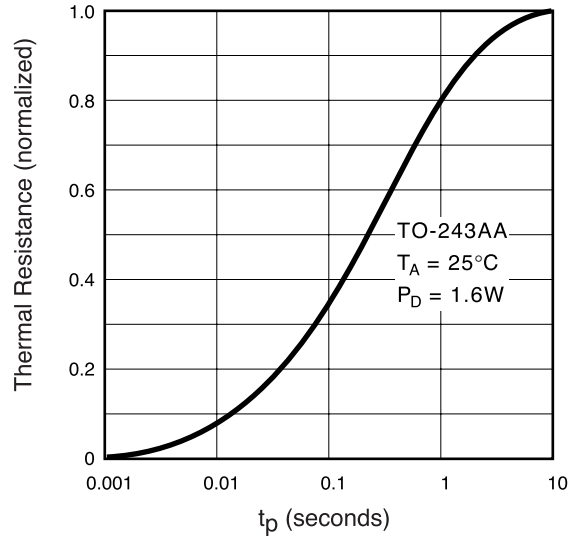
Power Dissipation vs. Ambient Temperature



Maximum Rated Safe Operating Area

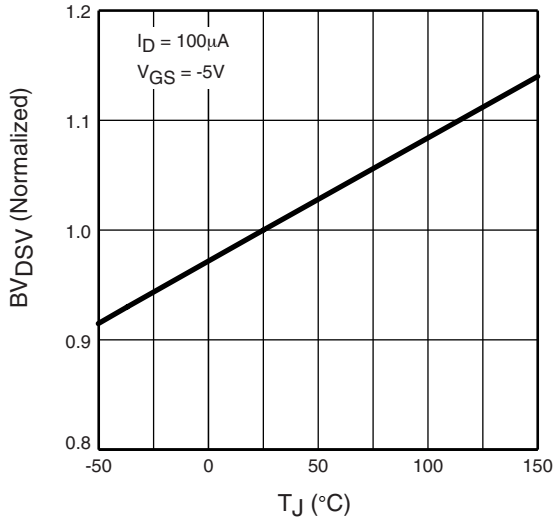


Thermal Response Characteristics

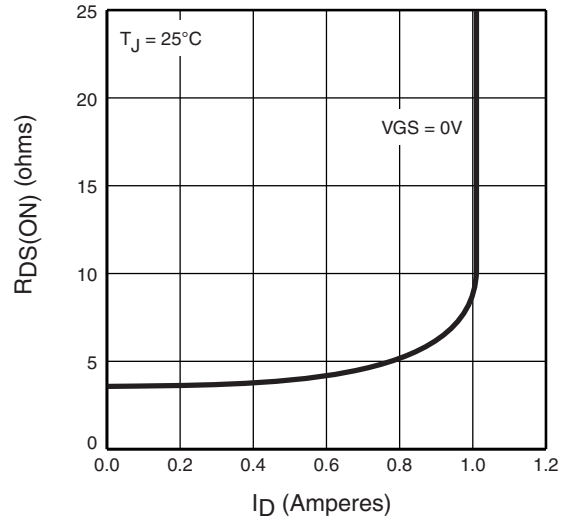


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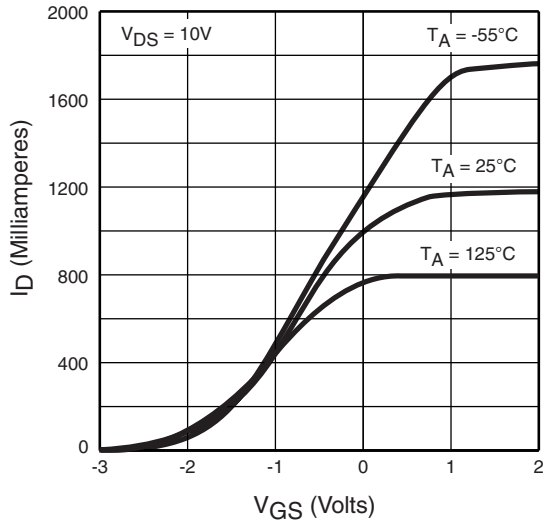
BV<sub>DSV</sub> Variation with Temperature



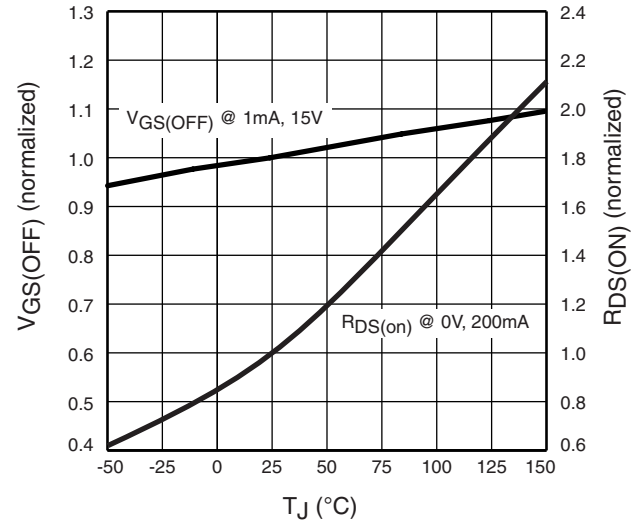
On Resistance vs. Drain Current



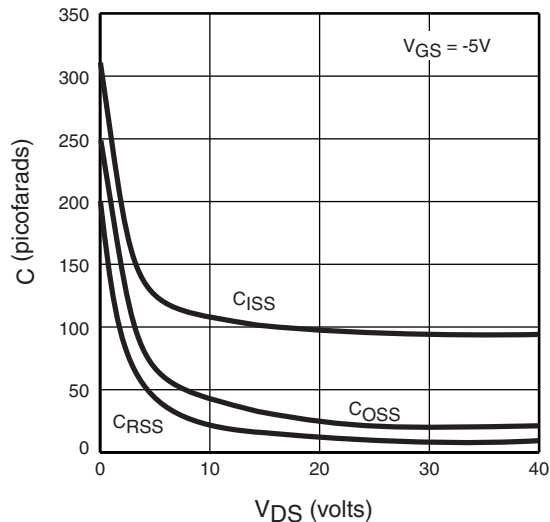
Transfer Characteristics



V<sub>GS(OFF)</sub> and R<sub>DS(ON)</sub> w/ Temperature



Capacitance vs. Drain Source Voltage



Gate Drive Dynamic Characteristics

