

1024-BIT ECL RAM (1024×1)**10415/10415A/10415B****DESCRIPTION**

The 10415 device is a 1024-word by 1-bit, fully encoded ECL Read/Write Random Access Memory designed for high speed scratch pad, control, and buffer storage applications. The device also includes full address decoding on-chip, separate data in and noninverting data out lines, an active LOW chip select.

FEATURES

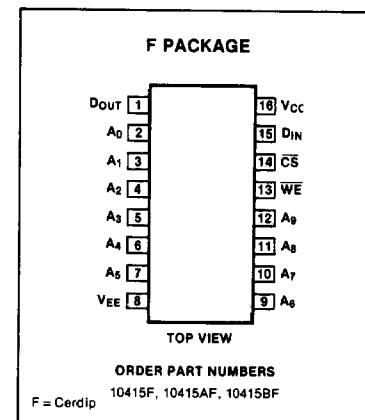
- Organization: 1024 words × 1 bit
- Fully compatible with 10K ECL families
- Operating temperature: 0°C to +75°C

ABSOLUTE MAXIMUM RATINGS

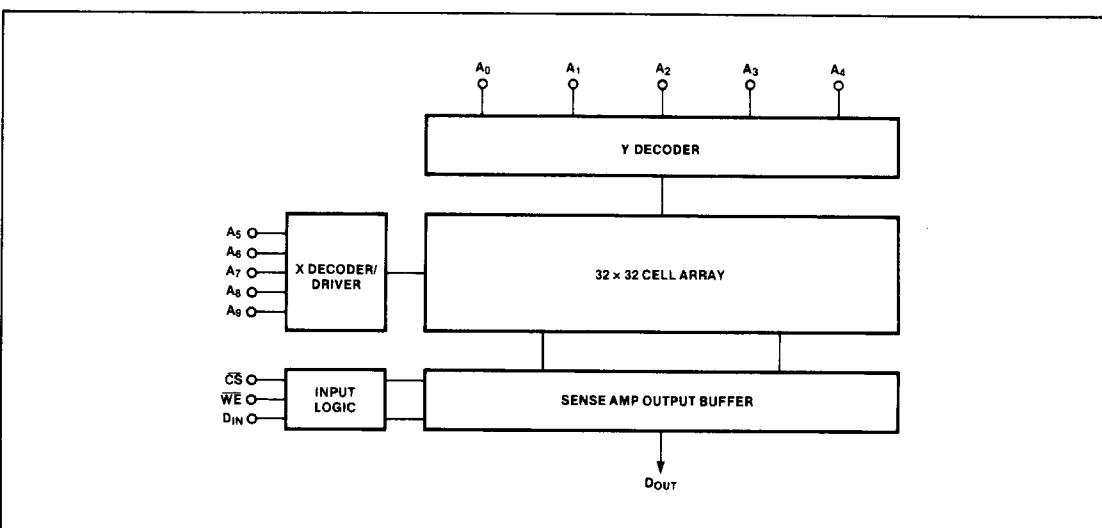
PARAMETER	RATING	UNIT
V_{EE}	Supply voltage	Vdc
V_O	Output voltage	Vdc
I_O	Output current	mA
T_A	Operating	°C
T_{sig}	Storage	°C

TRUTH TABLE

INPUTS			OUTPUT	MODE
\overline{CS}	\overline{WE}	DI		
H	X	X	L	Disable
L	H	X	D_{OUT}	Read
L	L	H	L	Write 1
L	L	L	L	Write 0

PIN CONFIGURATION

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BLOCK DIAGRAM

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DC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V$, $V_{EE} = -5.25V \pm 5\%$, Output load 50Ω to $-2V$, $0^\circ C \leq T_A \leq 75^\circ C$

PARAMETER	TEST CONDITIONS	0°C		+25°C		+75°C		UNIT
		Min	Max	Min	Max	Min	Max	
V_{IH} HIGH V_{IL} LOW V_{IHA} Threshold HIGH V_{ILA} Threshold LOW		–1.870 –1.145	–0.840 –1.490	–1.850 –1.105 –1.475	–0.810 –1.830 –1.045	–0.720 –1.450		V
V_{OH} HIGH V_{OL} LOW V_{OHA} Threshold HIGH V_{OLA} Threshold LOW		$V_{IH} = MAX$ $V_{IL} = MIN$ V_{IHA} V_{ILA}	–1.0 –1.870 –1.020	–0.840 –1.665 –0.980	–0.960 –1.850 –1.650	–0.810 –1.830 –0.900	–0.900 –1.830 –1.625	V
I_{IH} HIGH I_{IL} LOW I_{IL} CS		$V_{IH} = MAX$ $V_{IL} = MIN$ $V_{IL} = MIN$	–6 10	220	–6 10	220	–6 10	μA
I_{EE}	Supply current	$V_{IL} = MIN$		150		150		150 mA
C_{IN} Input						5		pF
NOTES								

1. Voltages are defined with respect to ground, pin 16.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow >400 ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V$, $V_{EE} = -5.2V \pm 5\%$, $0^\circ C \leq T_A \leq +75^\circ C$, $R_L = 50\Omega$ to $-2V$

PARAMETER	10415			10415A			10415B			UNIT
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
T_{AA}	Address access time		20			15			10	ns
T_{BD}	Chip select recovery time		5			5			5	ns
T_{BS}	Chip select access time		5			5			5	ns
T_{WD}	Write disable time ¹		6			6			6	ns
T_{WP}	Write pulse width	12		10			8			ns
T_{WR}	Write recovery time ¹		4.5	10		4.5	10		4.5	10 ns
T_{WHA}	Address hold time ¹	3	0	3	0		3	0		ns
T_{WHC}	Chip select hold time ¹	2	0	2	0		2	0		ns
T_{WHD}	Data hold time ¹	2	0	2	0		2	0		ns
T_{WSA}	Address setup time ¹	1	0	1	0		1	0		ns
T_{WSC}	Chip select setup time ¹	2	0	2	0		2	0		ns
T_{WSD}	Data setup time ¹	2	0	2	0		2	0		ns
t_f	Output fall time ²	0.5	2	0.5	2		0.5	2		ns
t_r	Output rise time ²	0.5	2	0.5	2		0.5	2		ns

NOTES

1. To guarantee a write into the slowest bit.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudo-random testing pattern.
3. AC limits apply after thermal equilibrium has been established.
4. Unit is in a test socket or mounted on a printed circuit board with transverse air flow >400 ft/min.
5. Setup and hold times are guaranteed for $T_W \geq T_W \text{ MIN}$.
6. All propagation measurements to output are measured from 50% of the input pulse to a valid output level ($V_{IH} \text{ MIN}$ or $V_{IL} \text{ MAX}$).
7. Typical values are at $V_{EE} = -5.2V$, $T_A = 25^\circ C$ and maximum loading.

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SWITCHING TIMES TEST CIRCUIT AND TIMING DIAGRAMS

