Preliminary Datasheet

VSC6424

500 Mb/s Video Shift Register IC

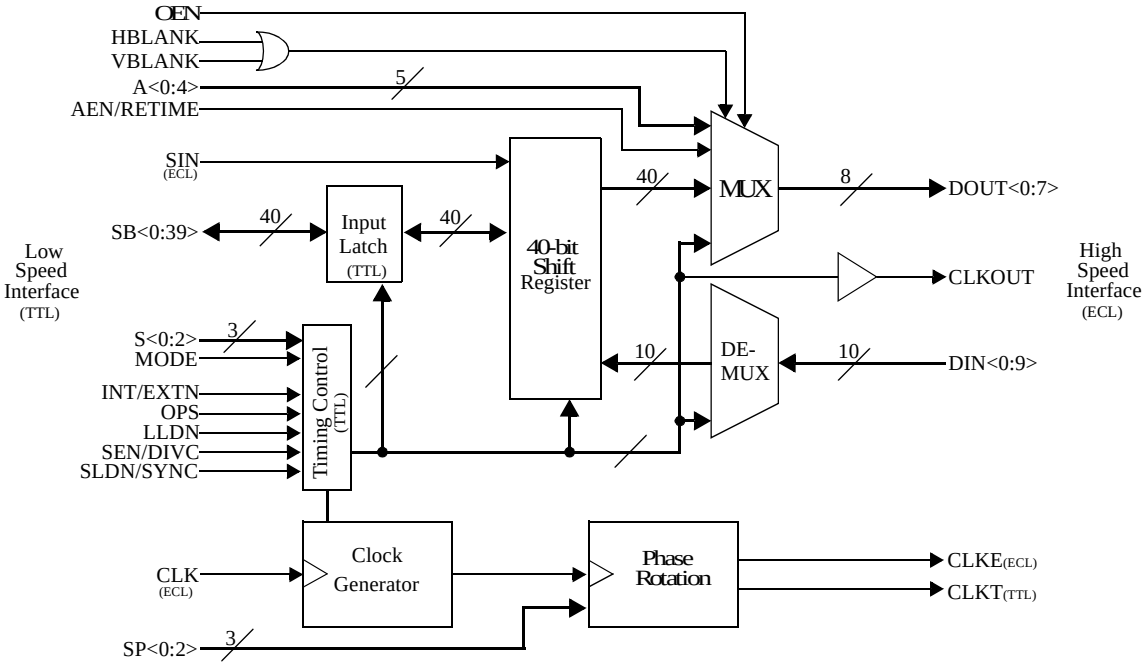
Features

- Multiplex or Demultiplex Operation
- Selectable Shift Register Length
- 500Mb/s Operation using internal timing
- 250Mb/s Operation using external timing
- Functional Replacement for Bt424
- External ECL Reference Voltage (-1.32 V)
- ECL and TTL I/Os: ECL for high-speed interface, TTL for low-speed interface
- Power Supplies: +3.3V and -2V @ 2.7 Watts (Max.)
- Commercial (0^o to $+70^oC$) Temperature Range
- Package: 14mm x 20mm 128 PQFP

General Description

The VSC6424 is a 500Mb/s video shift register IC that is based on a 40-bit user-configured shift register. The shift register may be used either as a multiplexer (parallel in, serial out) or as a demultiplexer (serial in, parallel out). The VSC6424 can be configured into 8 5-bit, 8 4-bit, 5 8-bit, 4 10-bit, 2 16-bit, 2 20-bit, 1 32-bit, or 1 40-bit shift register.

VSC6424 Functional Block Diagram



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Functional Description

The VSC6424 is a 40-bit user configurable shift register designed to provide general purpose serialization or de-serialization for high speed designs. The VSC6424 provides both multiplexer (MUX) and demultiplexer (DEMUX) operations in a single package. With the ability to generate timing signals internally or have them provided externally the VSC6424 maintains the highest design flexibility.

The low speed signals (parallel data, configuration, external timing) use a TTL interface and the high-speed signals (serial data, high-speed clock) use an ECL interface. Two power supplies are utilized, +3.3 Volts and -2 Volts, dissipating a maximum of 2.7 Watts. A -1.32V external reference voltage is necessary for the ECL interface. The part is packaged in a 14mm x 20mm 128-pin plastic quad flat pack with an exposed heat spreader.

Shift Register Mode/Modulus Selection

The shift register can be setup to work as multiplexer or as a demultiplexer. The MODE pin controls the direction of operation (MUX or DEMUX). The select pins S<0:2> put the shift register in one of 8 configurations shown in Table 1

Table 1: Modulus of Operation

S2	*S1*	*S0*	*Multiplexer MODE = 0*	*Demultiplexer MODE = 1*
0	0	0	8 4:1	10 1:4
0	0	1	8 5:1	8 1:5
0	1	0	5 8:1	5 1:8
0	1	1	4 10:1	4 1:10
1	0	0	2 16:1	2 1:16
1	0	1	2 20:1	2 1:20
1	1	0	1 32:1	1 1:32
1	1	1	1 40:1	1 1:40

Internal Timing

The VSC6424 can be set up to use either internal or external timing sources. The VSC6424 contains an internal timing generator that provides load and output rates depending on the modulus selected for the shift register. The timing generator takes an external high speed differential clock (*CLK*). Internal timing mode must be used for designs above 250MHz.

The internal timing generator also provides two low-speed clock outputs, CLKT(TTL) and CLKE(ECL). The low speed clock is brought out so that other ICs can use this to latch the low speed data while in DMUX mode. The slow speed clock output can be the same as the internal clock, or 1/2 the internal frequency by setting DIVC high. These outputs can also be shifted in 45 degree increments, using the *phase select* pins SP<0:2>, to allow compensation for trace delays on the board. Phase rotation is not available in divide by 5 or divide by 10 modes.

The internal high speed clock is also brought out to a differential ECL output (*CLKOUT*). This output is provided for clocking of the high speed data into the next IC.

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The Output Phase Shift (*OPS*) signal gives the capability of selecting which edge of the high speed clock the DOUT data is synchronized to. When *OPS* is low, *DOUT* comes out on the rising edge of *CLK*. When *OPS* is high, *DOUT* comes out on the falling edge of *CLK*. The high speed output clock (*CLKOUT*) is not affected by the state of *OPS*.

External Timing

To provide a functional replacement for older designs using the Bt424, formerly manufactured by Brook-Tree, the VSC6424 provides an external timing mode. This can be accomplished by setting the INT/EXTN pin low to bypass the internal timing generator. In this case the load and shift timing signals are provided through the Shift Enable(SEN), Shift Register Load Control(SLDN), and the Latch Load Control(LLDN) pins.

The VSC6424 has two cycles of propagation delay in multiplexer mode where the Bt424 only has one. This provides the ability to control on which edge of the output clock the output data is clocked on. With the Output Phase Select (OPS) pin low the output data (DOUT) is synchronous with the positive edge of CLKOUT, where if OPS is high the output data is synchronous to the negative edge of CLKOUT. See Figure 6 for a timing diagram example with OPS low.

The shift register can also be loaded with serial data while in external timing mode. This is accomplished by inputting data into the shift register through the Serial Input (SIN) pin. The data is latched on the rising edge of the CLK while SLDN is high and SEN is low. The data is then shifted to the output pins on each clock cycle once Shift Enable (SEN) is set high.

I/O Mapping

There are 10 high speed ECL data inputs and 8 high speed ECL data outputs. Some configurations of operation do not use all these inputs and outputs. The state of the outputs not being used in a given mode is not guaranteed. The following two tables, Table 2 and Table 3, show how the high speed bus (DOUT or DIN) maps to the low speed bus (SB) for a given configuration.

Data is taken and supplied LSB first. The numbers in the table cells refers to the data bit on the low speed bus (SB<0:39>). They are the inputs in MUX mode and the outputs in DEMUX mode.

Table 2: MUX Mode SB to DOUT Cross Reference

S<2:0>	*Modulus*	*DOUT7*	*DOUT6*	*DOUT5*	*DOUT4*	*DOUT3*	*DOUT2*	*DOUT1*	*DOUT0*
000	8 4:1	28-31	24-27	20-23	16-19	12-15	8-11	4-7	0-3
001	8 5:1	35-39	30-34	25-29	20-24	14-19	10-14	5-9	0-4
010	5 8:1	32-39	24-31		16-23		8-15		0-7
011	4 10:1		30-39		20-29		10-19		0-9
100	2 16:1		16-32				0-15		
101	2 20:1				20-39				0-19
110	1 32:1						0-31		
111	1 40:1								0-39

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Table 3: DEMUX Mode DIN to SB Cross Reference

S<2:0>	*Modulus*	*DIN9*	*DIN8*	*DIN7*	*DIN6*	*DIN5*	*DIN4*	*DIN3*	*DIN2*	*DIN1*	*DIN0*
000	10 1:4	36-39	32-35	28-31	24-27	20-23	16-19	12-15	8-11	4-7	0-3
001	8 1:5	35-39	30-34	25-29		20-24	14-19	10-14		5-9	0-4
010	5 1:8	32-29		24-31		16-23		8-15		0-7	
011	4 1:10	30-39		20-29			10-19			0-9	
100	2 1:16			16-32				0-15			
101	2 1:20	20-39					0-19				
110	1 1:32			0-31							
111	1 1:40	0-39									

Initialization

The VSC6424 requires that the SYNC/SLDN input be low for at least one clock cycle after power on, then be set high for at least on clock period to initialize the device. This is an edge sensitive function. In internal timing mode this serves to start the internal clock dividers and set the shift register and low speed output clocks in motion. Additional edges while in internal timing mode serves to synchronize the output clocks as described below. Once this has been done the device takes (2n) cycles to stabilize. During this time the slow bus (SB) should be set to zero. The first data is then latched from the slow bus (SB) at the end of the (2n) cycles. The device is now set to run and will latch data from the slow bus (SB) every (n) cycles. See Table 5 to determine (n) for a selected modulus.

In MUX mode with internal timing the VSC6424 chip can also be initialized by providing a slow speed clock to the SYNC input. This slow speed clock must be synchronized with high speed clock and based on the modulus that the MUX is set to. For example if the VSC6424 is set to 4:1 mode and the high speed clock is set to 500MHz then the SYNC input must be 125MHz. The initialization at power on will still take (2n) cycles of the high speed clock. This allows the system to dictate when the slow speed data is latched and where the shifting begins.

In external timing mode the SLDN/SYNC signal serves to set the shift register in motion once the data has been latched from the slow speed bus.

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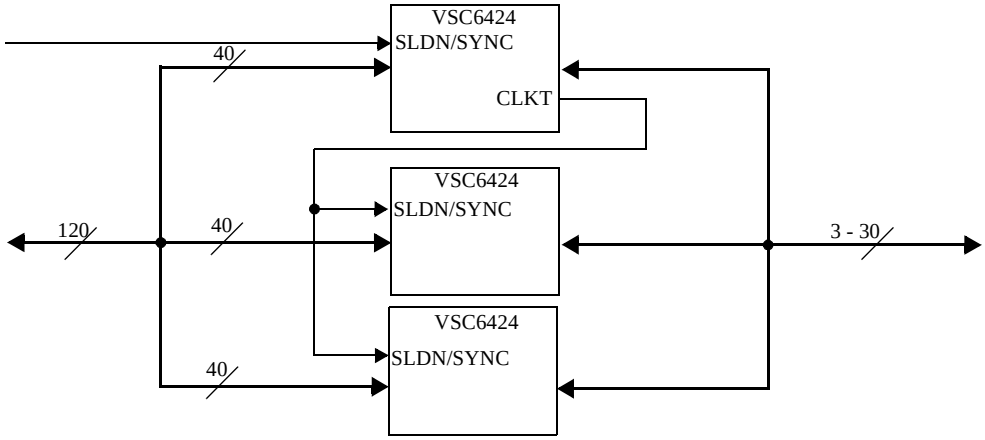
Figure 1: Synchronized VSC6424 Block Diagram



Synchronization

Several VSC6424 chips can be synchronized together while in internal timing mode by connecting the slow speed TTL clock output (*CLKT*) of a master chip to the synchronization input (*SYNC*) of a slave chip. The internal timing generator synchronizes to the rising edge of the SYNC input. Given that (n) is the number of high speed clock cycles for a given modulus mode, synchronization takes two times (n) or (2n) clock cycles to lock in. If it is necessary to synchronize more than two VSC6424 devices use the TTL clock output (CLKT) from one chip to drive the SYNC inputs of each of the slave devices. See Figure 2 for a block diagram. See Figure 7 for a timing illustration of the synchronization timing of the slave chip. See Table 5 to determine (n) for a selected modulus.

In MUX mode multiple VSC6424 chips can also be synchronized by providing a slow speed clock to the SYNC input on all of the devices. This slow speed clock must be synchronized with high speed clock and based on the modulus that the MUX is set to. For example if the VSC6424 is set to 8:1 mode and the high speed clock is set to 400MHz then the SYNC input must be 50MHz.

MPU Address Interface

An *Address Interface* mode translates TTL compatible addresses to ECL compatible output levels. This is provided for compatibility with the Bt424. When the Address Enable (*AEN)* signal is low, data from the Address Line *A<0:4>* TTL input pins is transferred to the *DOUT<0,2,4,6,7>* ECL output pins with one clock cycle delay. When *AEN* is high, the *A<0:4>* inputs are ignored. The *DOUT<0:7>* data is always synchronized to *CLK*, regardless of the state of *AEN*. See Figure 9 for a timing illustration of this function.

Video Blanking

The VSC6424 also has a blanking function for video applications. In multiplexer mode, this function allows zeroing of the high speed outputs (*DOUT<0:7>*). Setting *HBLANK* or *VBLANK* low drives all *DOUT<0:7>* outputs low synchronously with the clock (*CLK*). The outputs will be driven low on the modulus boundary. The outputs are driven low for (n) clock cycles given that (n) is the modulus mode that the chip is set to. See table 4 to determine the value of (n) for a given modulus.

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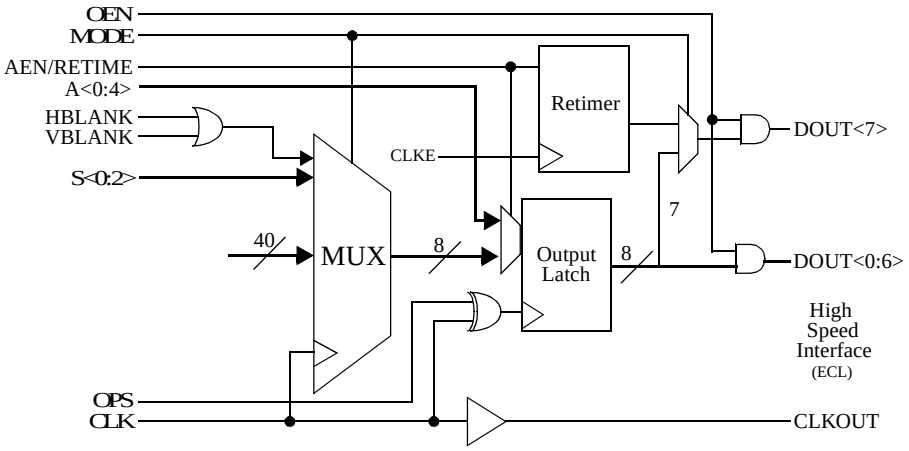
HBLANK or *VBLANK* must be driven low for at least one clock cycle two clock cycles before the desired point of blanking. See Figure 6 for a timing illustration of this function.

Retimer

The chip also contains a retimer function. This function works in *DEMUX* mode. The *RETIME* signal is routed to *DOUT<7>* through a flip-flop. The flip-flop is internally clocked by the low speed ECL output clock (*CLKE*). This function is depicted in the detailed block diagram (Figure 3) below. See Figure 5 for a timing illustration.

Figure 2: Multiplexer Detailed Block Diagram



Termination

It is recommended to leave all unused ECL outputs floating. It is recommended that unused ECL inputs be terminated low (-2V supply). Refer to the following table recommended input termination for all levels.

Table 4: Input Termination Recommendations

Type	*State*	*Input*
ECL	High	ground via a diode
ECL	Low	-2V supply
TTL	High	+3.3V supply
TTL	Low	Ground

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Figure 3: Multiplexer Timing (Internal Timing. 4:1 Mode.)

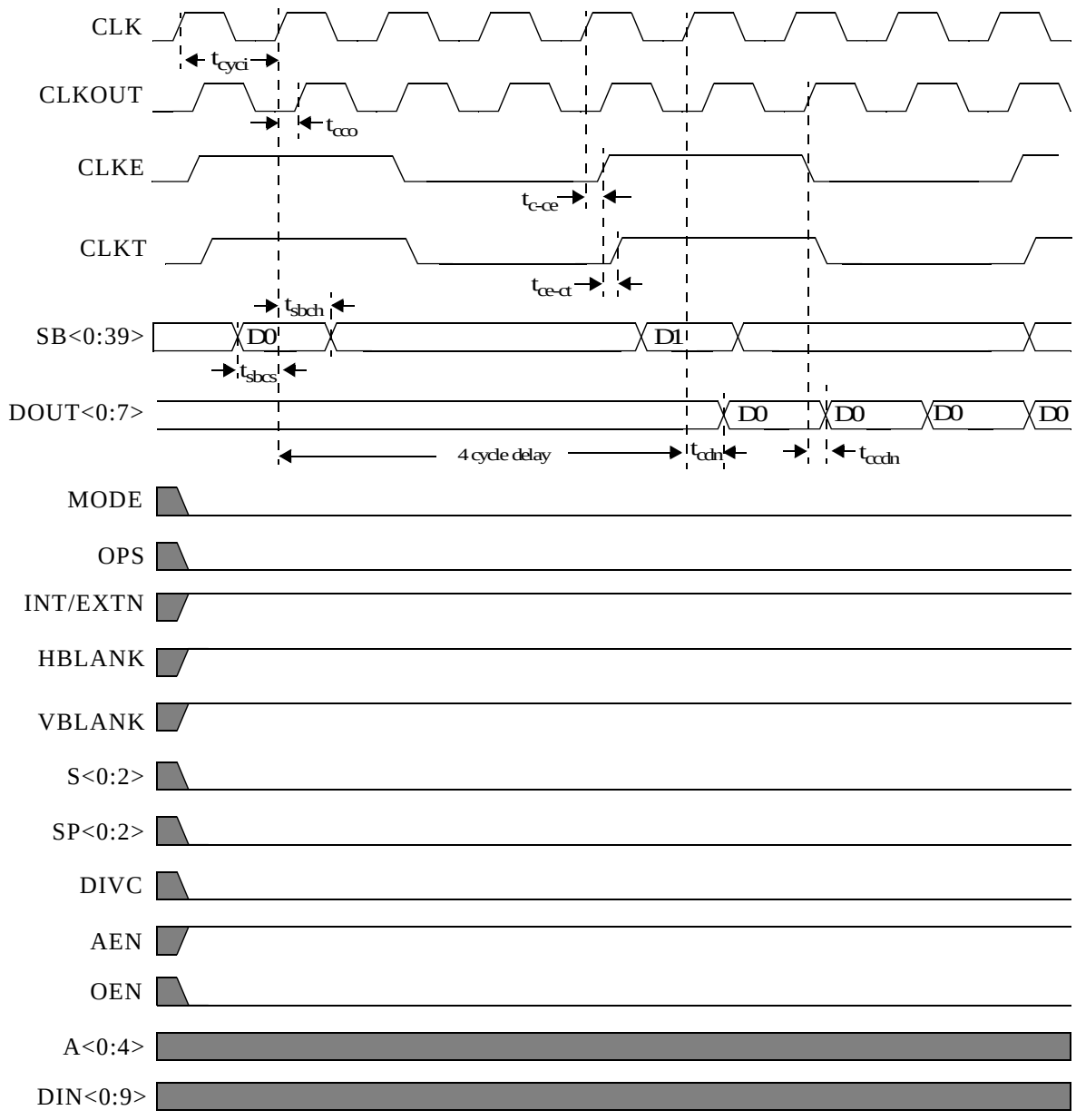

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Figure 4: Demultiplexer and Retimer Timing (Internal Timing. 1:4 Mode.)

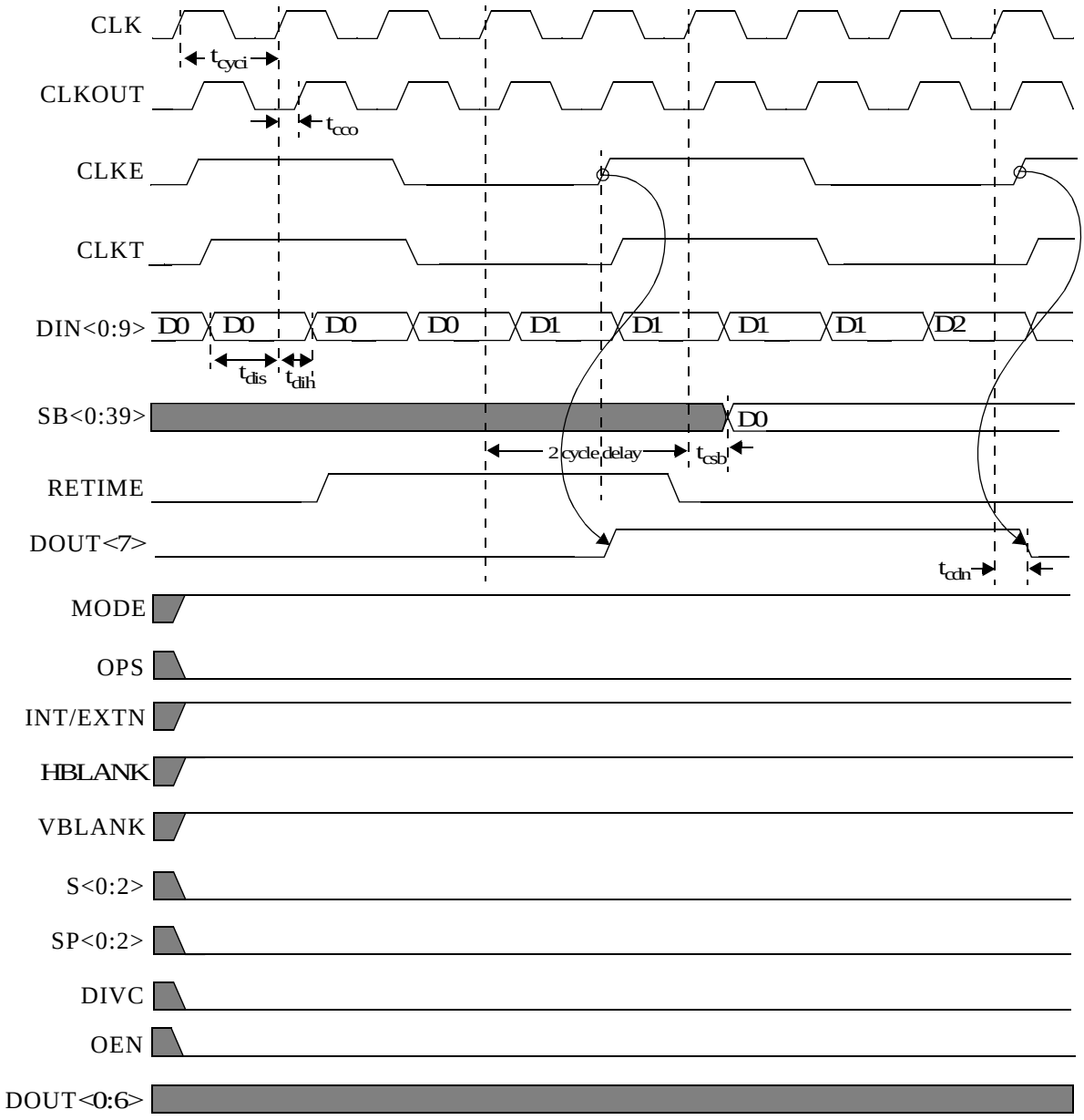

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Figure 5: Multiplexer Timing (External Timing. 4:1 Mode)

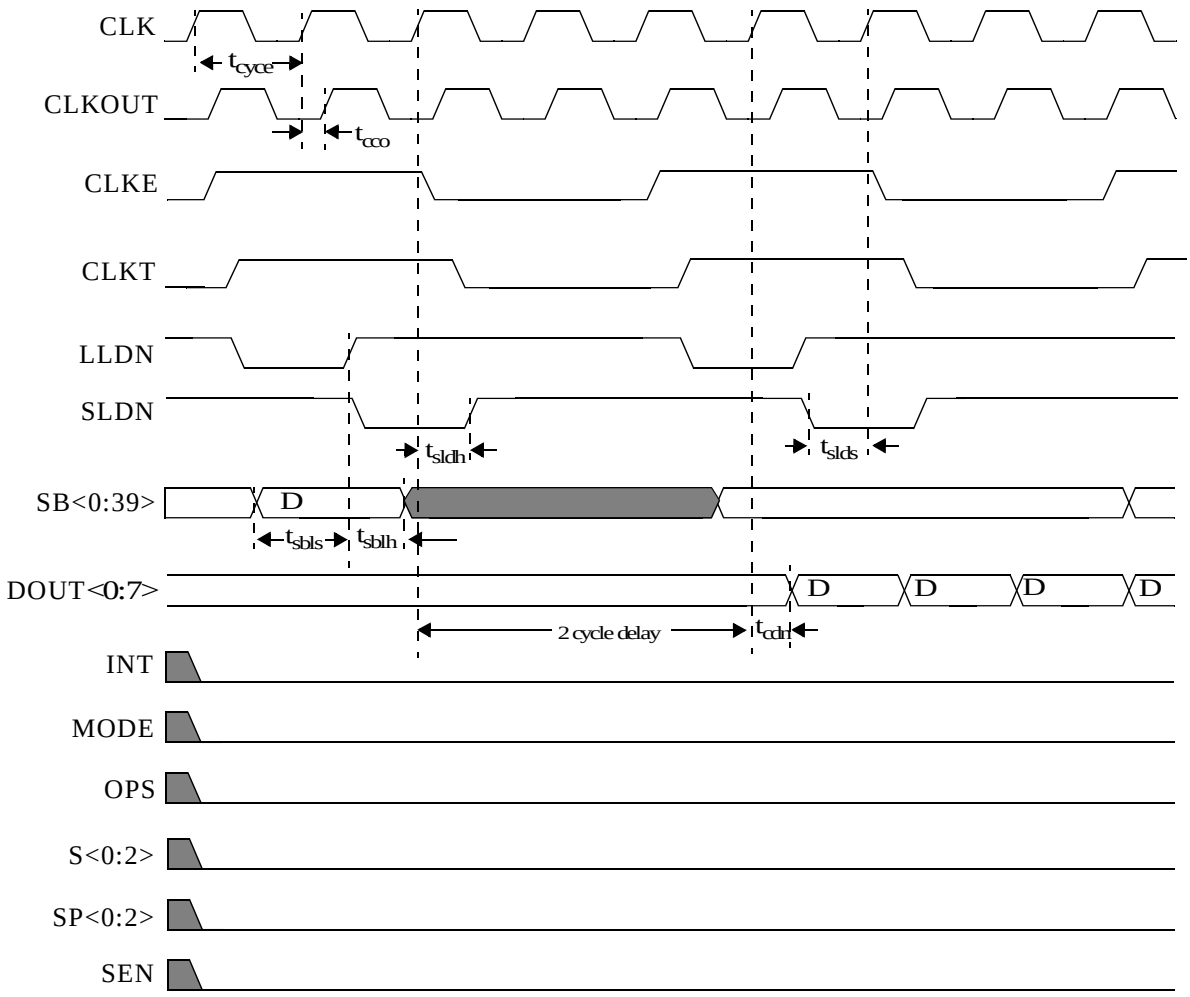

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Figure 6: Initialization Timing 4:1 Mode

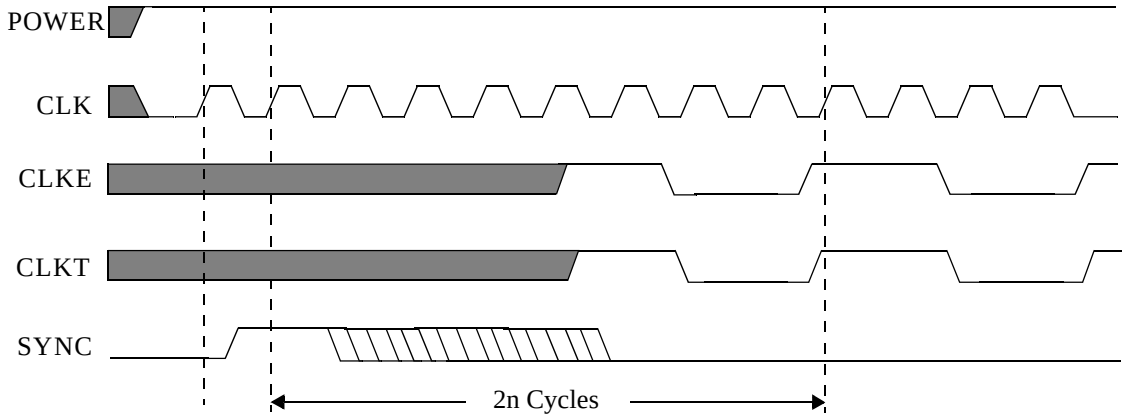

Figure 7: Synchronization Timing

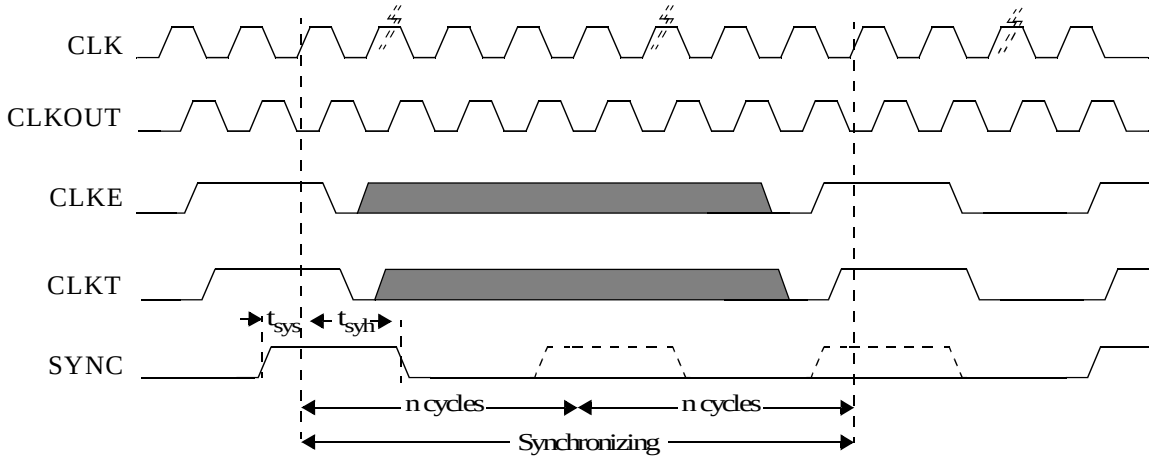

Table 5: Synchronization & Blanking Timing

S<0:2>	000	001	010	011	100	101	110	111
n	4	5	8	10	16	20	32	40

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Figure 8: Blanking Timing (Internal Timing)

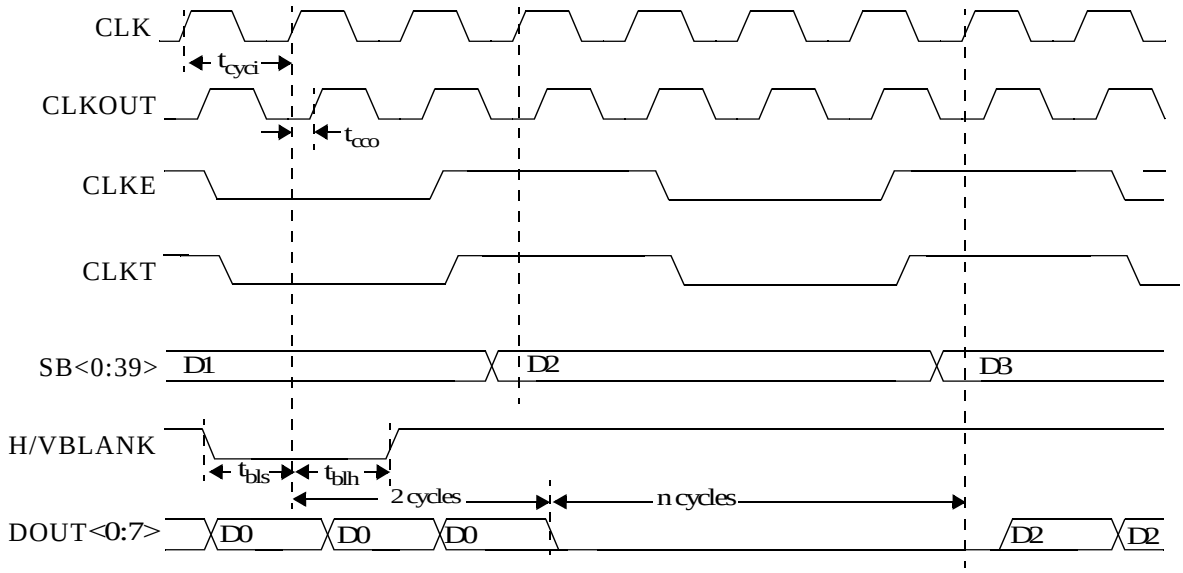

Figure 9: Address Interface / Output Enable Timing

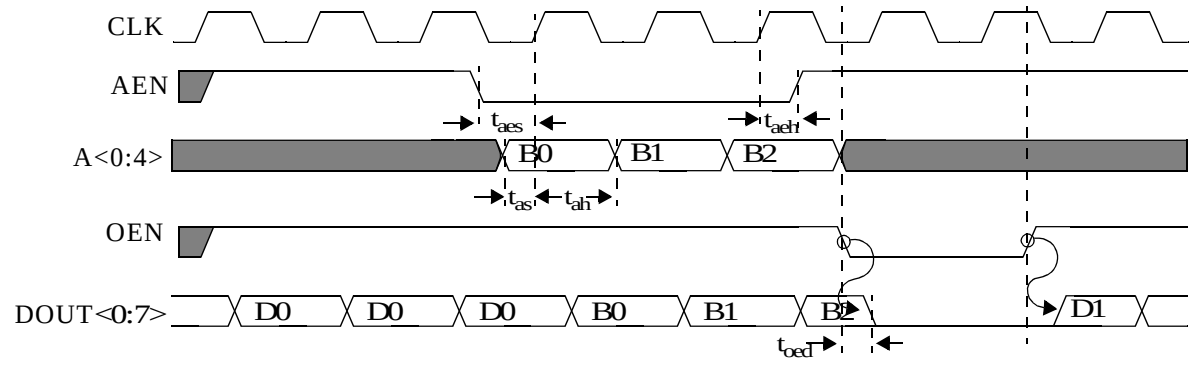

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Table 6: Timing Tables

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
t_{cyci}	Minimum cycle time in internal timing mode	2.0	-	-	ns
t_{cyce}	Minimum cycle time in external timing mode	4.0	-	-	ns
t_{dis}	DIN setup time	200	-	-	ps
t_{dih}	DIN hold time	900	-	-	ps
t_{sbcs}	SB setup with respect to CLK	600	-	-	ps
t_{sbch}	SB hold time with respect to CLK	800	-	-	ps
t_{sbls}	SB setup with respect to LLD	100	-	-	ps
t_{sblh}	SB hold with respect to LLD	1200	-	-	ps
t_{cco}	CLK to CLKOUT delay	1100	-	3500	ps
t_{cdn}	CLK rising to DOUT, with OPS low	1200	-	3700	ps
t_{cdi}	CLK falling to DOUT, with OPS high	1300	-	3900	ps
t_{ccdn}	CLKOUT to DOUT skew, with OPS low	-140	-	1100	ps
t_{ccdi}	CLKOUT to DOUT skew, with OPS high	-50	-	1200	ps
t_{oed}	OEN to DOUT	900	-	3000	ps
t_{dds}	DOUT<*x*> to DOUT<*y*> skew	-	-	100	ps
t_{as}	A<0:4> setup time	1100	-	-	ps
t_{ah}	A<0:4> hold time	200	-	-	ps
t_{aes}	AEN setup time	900	-	-	ps
t_{aeh}	AEN hold time	600	-	-	ps
t_{bls}	H/VBLANK setup	1000	-	-	ps
t_{blh}	H/VBLANK hold	200	-	-	ps
t_{slds}	SLDN setup	1300	-	-	ps
t_{sldh}	SLDN hold	100	-	-	ps
t_{sys}	SYNC setup	800	-	-	ps
t_{syh}	SYNC hold	300	-	-	ps
t_{sis}	SIN setup	700	-	-	ps
t_{sih}	SIN hold	300	-	-	ps
t_{csb}	CLK to SB delay	1700	-	5800	ps
$t_{c\text{-}ce}$	CLK to CLKE delay	1500	-	5200	ps
$t_{ce\text{-}ct}$	CLKE to CLKT skew	400	-	2500	ps

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DC Characteristics

Table 7: ECL Inputs and Outputs

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage	-1020	-	-700	mV	-
V_{OL}	Output LOW voltage	-2000	-	-1620	mV	-
V_{IH}	Input HIGH voltage	-1165	-	-700	mV	-
V_{IL}	Input LOW voltage	-2000	-	-1475	mV	-
I_{IH}	Input HIGH current	-	-	200	µA	$V_{IN}=V_{IH}$ (max)
I_{IL}	Input LOW current	-50	-	-	µA	$V_{IN}=V_{IL}$ (min)

Notes: 1) Load=50Ω to -2.0V.
2) External Reference (V_{ref}) = -1.32 V ± 25mV

Table 8: TTL Inputs and Outputs

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage	2.4	-	V	I_{OH} = -12 mA
V_{OL}	Output LOW voltage	-	0.4	V	I_{OL} = 12mA
V_{IH}	Input HIGH voltage	2.0	V_{TTL} + 1.0 V	V	-
V_{IL}	Input LOW voltage	0	0.8	V	-
I_{IH}	Input HIGH current	-	300	µA	V_{IN} = 2.4 V
I_{IL}	Input LOW current	-50	-	µA	V_{IN} = 0.4 V
I_{OZH}	3-State Output OFF Current HIGH	-	200	µA	V_{OUT} = 2.4 V
I_{OZL}	3-State Output OFF Current LOW	-100	-	µA	V_{OUT} = 0.4 V
I_{OZHB}	3-State Output OFF Current HIGH for Bi-directs	-	500	µA	V_{OUT} = 2.4 V
I_{OH}	Open Collector Output Leakage Current	-	200	µA	V_{OUT} = 2.4 V

Notes: 1) Outputs are open

Power Dissipation

Table 9: VSC6424 Power Supply Currents

Parameter	*Description*	*(Max)*	*Units*
I_{TT}	Power supply current from V_{TT} (-2.0 V±0.1V Max -2.1V)	850	mA
I_{TTL}	Power supply current from V_{TTL} (+3.3 V±0.3V Max +3.6V)	250	mA
P_D	Power dissipation (*Note: Specified with outputs open circuit.*)	2.7	W

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Absolute Maximum Ratings(1)

Power Supply Voltage (V_{TT}) Potential to GND ..... -2.5 V to +0.5 V
Power Supply Voltage (V_{TTL}) Potential to GND ..... -0.5 V to +4.3 V
ECL Input Voltage Applied ..... +0.5 V to V_{TT} -0.5 V
TTL Input Voltage Applied ..... -0.5V to V_{TTL} + 1.0V
Output Current (I_{OUT}) ..... 50 mA
Case Temperature Under Bias (T_C) ..... -55° to + 125°C
Storage Temperature (T_{STG}) ..... -65° to + 150°C

Note: Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage (V_{TT}) ..... -2.0 V±0.1V
Power Supply Voltage (V_{TTL}) ..... +3.3 V±0.3V
Commercial Operating Temperature Range* (T) ..... 0° to 70°C

** Lower limit of specification is ambient temperature and upper limit is case temperature.*

ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC6424 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1500V.

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Package Pin Descriptions

Table 10: Package Pin Identification

Signal	*Pin*	*I/O*	*Level*	*Description*
VCC	7, 9, 18, 30, 32, 44, 45,58, 59, 71, 72, 73, 82, 85, 94, 96, 108, 109, 122, 123			0V Ground Connection.
VTT	3, 6, 13, 26, 33, 70, 77, 90, 97			-2V Supply Connection.
VTTL	5, 8, 21, 31, 34, 48, 55, 69, 95, 98, 112, 119			+3.3V Supply Connection
VREF	4			-1.32V external ECL Reference voltage.
DIN<0:9>	101, 102, 103, 104, 105, 68, 67, 66, 65, 64	I	ECL	The 10 Demultiplexer High-Speed Inputs.
DOUT<0:7>	86, 84, 83, 81, 80, 76, 75, 74	O	ECL	The 8 Multiplexer High-Speed Outputs.
SB<0:39>	89, 91, 92, 93, 110, 111, 113, 114, 115, 116, 117, 118, 120, 121, 10, 11, 12, 14, 15, 16, 17, 19, 20, 22, 23, 24, 25, 27, 28, 29, 46, 47, 49, 50, 51, 52, 53, 54, 56, 57	B	TTL	Slow Bidirectional Bus. Multiplexer Input, Demultiplexer Output.
MODE	62	I	TTL	Mux/DMux select signal. 1 for DMUX, 0 for MUX.
AEN RETIME	100	I	TTL	Address enable. In Mux mode, while AEN is low, the clock transfers A<0:4> to DOUT<0,2,4,6,7>. In DMUX mode it provides retimer input.
CLK	60	I	ECL	Differential Clock Input (*True*)
CLKN	61	I	ECL	Differential Clock Input (*Complement*)
S<0:2>	39, 40, 41	I	TTL	Shift Register Modulus Control
CLKE	87	O	ECL	Low Speed Clock. Clock used for latching the low speed bus in internal timing mode.
CLKT	88	O	TTL	Low Speed Clock. TTL version of above.
SP<0:2>	36, 37, 38	I	TTL	Phase select for output clocks (CLKE, CLKT)
SYNC SLDN	106	I	TTL	Shift register load control. Used to transfer data from input latch to shift register in external timing mode. Data is transferred on the rising edge of CLK while SLDN is low. In internal timing mode, SYNC is the synchronization input.
LLDN	43	I	TTL	Input latch control. In external timing mode, LLDN low makes the low speed input latches transparent.
SIN	42	I	ECL	Serial data in. The shift register can be serially loaded using this pin. The data is latched on rising edge of CLK. Connect to VTT if not used.

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Table 10: Package Pin Identification

Signal	*Pin*	*I/O*	*Level*	*Description*
SEN DIVC	63	I	ECL	Shift enable. In external timing mode, SEN high stops the shift register from shifting. In internal timing mode, DIVC high divides the output clocks (*CLKE, CLKT*)by 2.
OEN	107	I	ECL	Output Enable. OEN high forces the DOUT<0:7> low. This signal is asynchronous.
INT EXTN	99	I	TTL	Timing control. A high sets the chip for internal timing, a low sets the chip for external timing.
A<0:4>	2, 1, 128, 127, 126	I	TTL	Address pins. These pins get transferred to DOUT<0:7> in Address Interface mode.
HBLANK	124	I	TTL	Horizontal blank function. Active low.
VBLANK	125	I	TTL	Vertical blank function. Active low.
OPS	35	I	TTL	Clock phase select. When this signal is low the low speed outputs (*DOUT<0:7>*) are clocked with the rising edge of the clock. Setting it high clocks them with the falling edge of the clock.
CLKOUT	78	O	ECL	High speed clock out (*True*)
CLKOUTN	79	O	ECL	High speed output clock (*Complement*)

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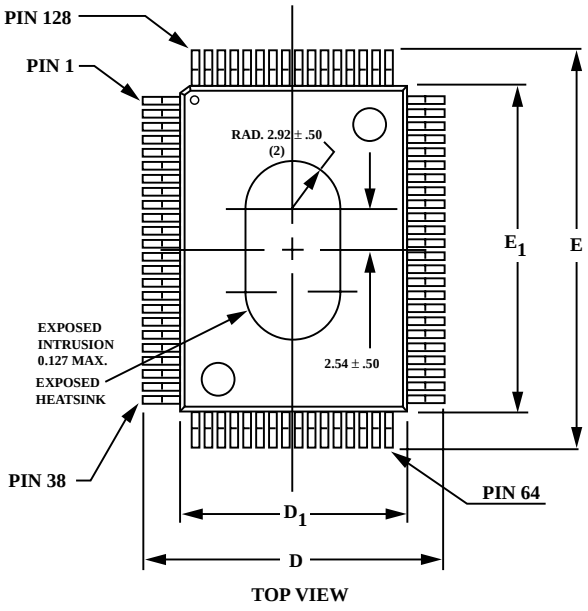
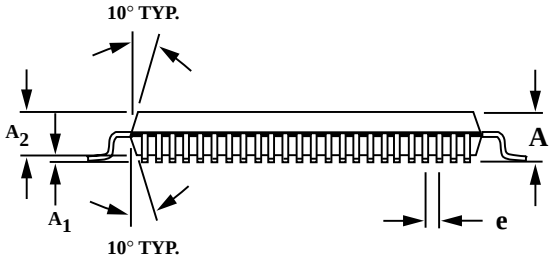
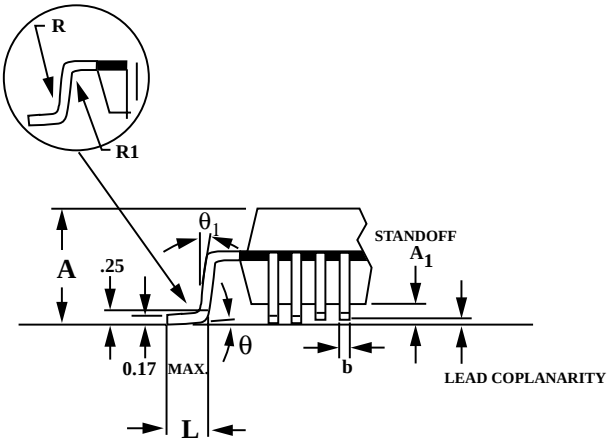
Package Information

The VSC6424 is packaged in a thermally enhanced 128 PQFP with an embedded heat sink.



TOP VIEW





Key	Dimensions	Tolerances
A	3.40	MAX.
A1	.25	MIN.
A2	2.70	± .10
D	17.20	± .20
D1	14.00	± .10
E	23.20	± .20
E1	20.00	± .10
L	.88	+.15/-.10
e	.50	BASIC
b	.22	± .05
ddd	.08	MAX.
Θ	0°-7°	
ccc	.08	MAX.
R1	.20	TYP.
R	.30	TYP.

Part Number:101-267-7
Issue Number: 1

Notes: 1) Drawing is not to scale
2) All dimensions in mm
3) Package represented is also used for the 64, 80, & 100 PQFP packages. Pin count drawn does not reflect the 128 Package.

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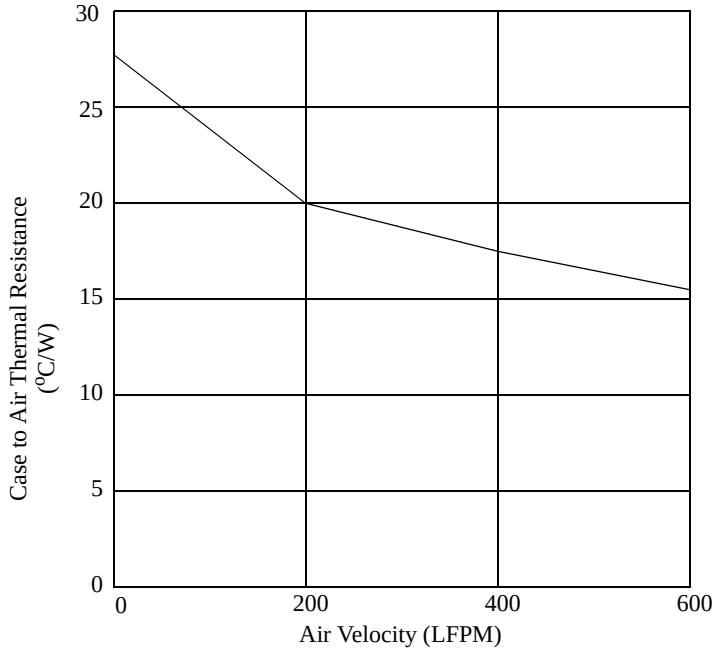
Package Thermal Considerations

Figure 10: ΘCA vs Air Velocity for the 128 PQFP (14mmx20mmx2.7mm)



Air Vel. LFPM	*Theta(ca) °C/W*
0	27.5
100	23.1
200	19.8
400	17.6
600	16.0

Θ_{CA} measurement method: Semi-standard G38-87, in a wind tunnel
Semi-standard G42-88/JEDEC JC 15.1 #1 FR4 PCB 3”x4.5”x0.62”

Notice

This document contains preliminary information about a new product in the preproduction phase of development. The information in this document is based on initial product characterization. Vitesse reserves the right to alter specifications, features, capabilities, functions, manufacturing release dates, and even general availability of the product at any time. The reader is cautioned to confirm this datasheet is current prior to using it for design.

Warning

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