J174 SERIES
P-Channel JFETs

The J174 Series are low-cost p-channel analog switches designed to provide low on-resistance and fast switching. They also work well in conjunction with Siliconix' J111 Series for complimentary switching applications. The J174 Series devices are housed in TO-92 packages and are available with various tape and reel options. (See Section 7.)

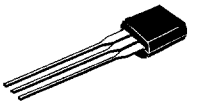
PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (nA)	t_{ON} TYP (ns)
J174	10	85	-1	25
J175	6	125	-1	25
J176	4	250	-1	25
J177	2.25	300	-1	25

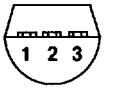
For further design information please consult the typical performance curves PSCIA.

SIMILAR PRODUCTS

- TO-18, See 2N5114 Series
- SOT-23, See SST174 Series
- Chips, See PSCIA Series Die

TO-92 (TO-226AA) BOTTOM VIEW





1 DRAIN
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	30	V
Gate-Source Voltage	V_{GS}	30	
Gate Current	I_G	-50	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature Range	T_J	-55 to 135	°C
Storage Temperature Range	T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

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SPECIFICATIONS[a]			LIMITS					
				J174		J175		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V	45	30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = −15 V, I_D = −10 nA		5	10	3	6	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = −15 V, V_{GS} = 0 V		−20	−135	−7	−70	mA
Gate Reverse Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	0.01		1		1	nA
		T_A = 125°C	5					
Gate Operating Current	I_G	V_{DG} = −15 V, I_D = −1 mA	0.01					
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = −15 V, V_{GS} = 10 V	−0.01		−1		−1	
		T_A = 125°C	−5					
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, V_{DS} = −0.1 V			85		125	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = −1 mA, V_{DS} = 0 V	−0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = −15 V, I_D = −1 mA, f = 1 kHz	4.5					mS
Common-Source Output Conductance	g_{os}		20					µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA, f = 1 kHz			85		125	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V, f = 1 MHz	20					pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = 10 V, f = 1 MHz	5					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = −10 V, I_D = −1 mA, f = 1 kHz	20					$nV/\sqrt{Hz}$
SWITCHING								
Turn-On Time	$t_{d(ON)}$	$V_{GS(ON)}$ = 0 V	10					ns
	t_r	P/N V_{DD} $V_{GS(OFF)}$ R_L	15					
Turn-Off Time	$t_{d(OFF)}$	J174 −10 V 12 V 560Ω J175 −6 V 8 V 1200Ω	10					
	t_f		20					

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

SPECIFICATIONS[a]			LIMITS					
				J176		J177		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V	45	30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = −15 V, I_D = −10 nA		1	4	0.8	2.25	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = −15 V, V_{GS} = 0 V		−2	−35	−1.5	−20	mA
Gate Reverse Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	0.01		1		1	nA
		T_A = 125°C	5					
Gate Operating Current	I_G	V_{DG} = −15 V, I_D = −1 mA	0.01					
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = −15 V, V_{GS} = 10 V	−0.01		−1		−1	
		T_A = 125°C	−5					
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, V_{DS} = −0.1 V			250		300	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = −1 mA, V_{DS} = 0 V	−0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = −15 V, I_D = −1 mA, f = 1 kHz	4.5					mS
Common-Source Output Conductance	g_{os}		20					µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA, f = 1 kHz			250		300	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V, f = 1 MHz	20					pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = 10 V, f = 1 MHz	5					
Equivalent Input Noise Voltage	$\overline{e_n}$	V_{DG} = −10 V, I_D = −1 mA, f = 1 kHz	20					$nV/\sqrt{Hz}$
SWITCHING								
Turn-On Time	$t_{d(ON)}$	$V_{GS(ON)}$ = 0 V	10					ns
	t_r	P/N V_{DD} $V_{GS(OFF)}$ R_L	15					
Turn-Off Time	$t_{d(OFF)}$	J176 −6 V 6 V 5600Ω J177 −6 V 3 V 10000Ω	10					
	t_f		20					

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

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