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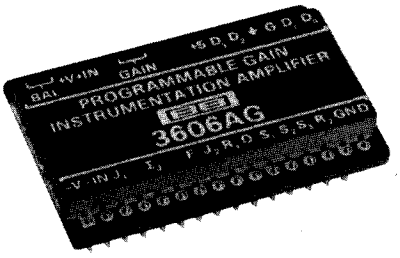
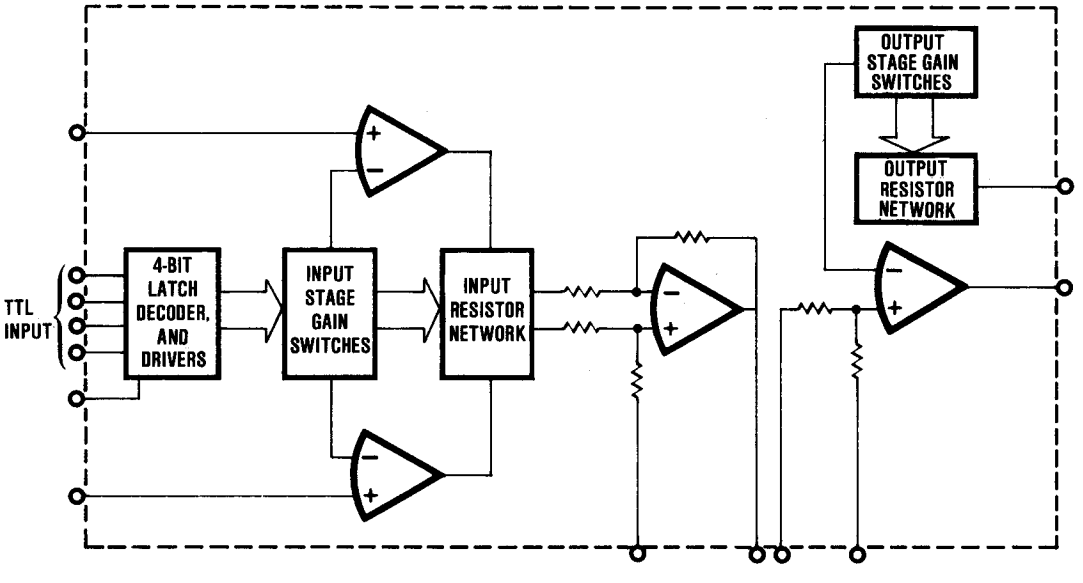


3606

Digitally Controlled Programmable Gain INSTRUMENTATION AMPLIFIER

FEATURES

- 11 BINARY GAINS - 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024V/V
- 4-BIT TTL GAIN CONTROL
- EXCELLENT GAIN NONLINEARITY 0.01% max at G = 1024V/V
- LOW GAIN ERRORS - 0.02% max
- LOW GAIN DRIFT - 10ppm/°C max
- LOW VOLTAGE DRIFT 1μV/°C max RTI, G = 1024V/V
- HIGH CMR - 110dB min, G = 1024V/V
- HIGH INPUT IMPEDANCE - 10 x $10^9\Omega$
- LOW OFFSET VOLTAGE 22μV max RTI, G = 1024V/V 2mV max RTI, G = 1V/V



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SBOS170

DESCRIPTION

The 3606 is a self-contained, Programmable Gain Instrumentation Amplifier (PGIA) whose gain can be changed in 11 binary weighted steps from 1 to 1024V/V. The gain control is accomplished through a 4-bit TTL input.

The PGIA function allows the user to deal with wide dynamic range signals while maintaining high system resolution. For example: when used with a 10-bit A to D converter in a "floating point" system, the 2^{10} gain range of the 3606, plus the 2^{10} range of the converter produces a total system resolution of 2^{20} (|| 1,000,000:1).

Desirable characteristics of a high performance instrumentation amplifier are offered by the 3606: high input impedance (10GΩ), excellent gain nonlinearity (0.01% max, G = 1024V/V; 0.02% max, G = 1V/V), high common-mode rejection (100dB min, G≥ 4V/V), low gain error (0.02% max with no trimming required), low gain temperature coefficient (10ppm/°C max), and low offset voltage drift vs temperature (1μV/°C max, RTI, G = 1024).

Added to these outstanding instrumentation amplifier characteristics is the ability to change 3606's gain under control of a 4-bit TTL input word. An important characteristic of the 3606 PGIA is its low change in offset plus laser trimming minimized this change to a maximum of ±25mV with no external adjustments. With two simple offset adjustments the change can be limited to less than 2mV (1mV typ) at the output over the entire 1V/V to 1024V/V gain range.

A simplified schematic of the 3606 is shown in Figure 1. The circuit consists of a variable gain high input impedance voltage follower input stage (A1 and A2) followed by a unity gain difference amplifier (A3) with a variable gain output stage (A4).

Common-mode voltage is derived for active guard drive to improve system common-mode rejection. Two-pole, low-pass filtering can easily be implemented on the output stage to reduce noise bandwidth and improve system signal-to-noise operation. A latch function is provided to inhibit gain changes while the digital gain control input is changed.

Burr-Brown's instrumentation grade monolithic operational amplifiers, high stability precision thin-film resistor networks and advanced laser-trimming techniques are used by the 3606 to achieve a performance, size and cost combination never before achieved in a PGIA. It is available in a 32-pin dual-in-line package in either ceramic or metal (hermetic) configurations.

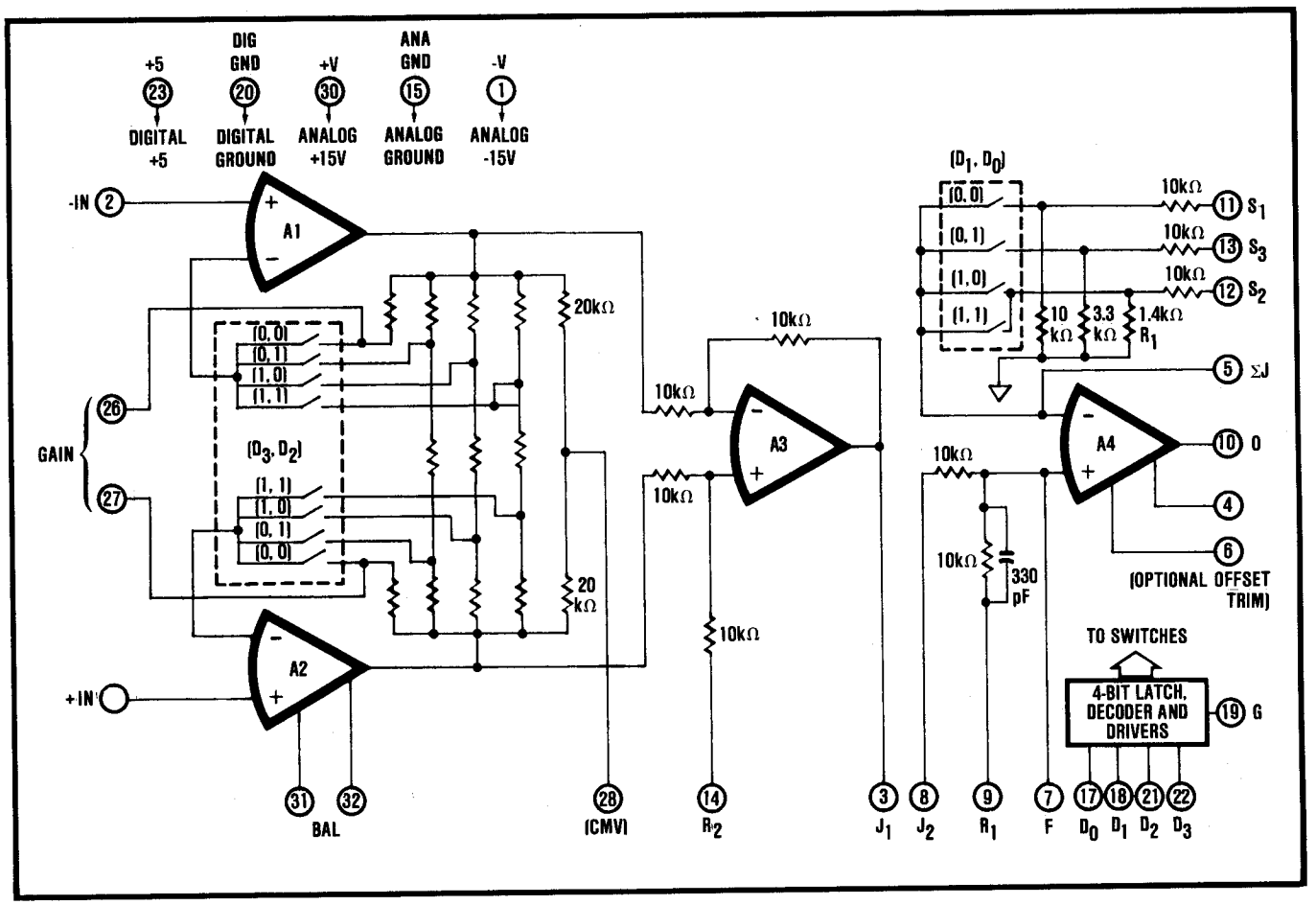


FIGURE 1. Simplified Schematic.

SPECIFICATIONS

ELECTRICAL

Typical at +25°C. unless otherwise noted.

PARAMETER	CONDITIONS	3606A[1] MIN	3606A[1] TYP	3606A[1] MAX	3606B[1] MIN	3606B[1] TYP	3606B[1] MAX	UNITS
GAIN, G[2]								
Inaccuracy	G = 1 to 1024, Io = 1mA		±0.02	±0.05		±0.01	±0.02	%
Nonlinearity[3]	G = 1 to 16		0.001	0.002		*	*	%[5]
	G = 32 to 128		0.003	0.004		*	*	%
	G = 256 to 1024		0.005	0.01		*	*	%
Drift vs Temperature	G = 1 to 1024		±5	±10		*	*	ppm/°C
vs Time	G = 1 to 1024		±0.01					%/1000 hrs
RATED OUTPUT								
Voltage	Io = ±5mA	±10	±12		*	*		V
Current	Vo = ±10V	±5	±10		*	*		mA
Impedance			0.05			*		Ω
INPUT CHARACTERISTICS								
Absolute Max Voltage	No damage			±Vcc			*	V
Common-Mode Voltage Range	Linear operation	±10	±10.5		*	*		V
Differential Impedance			10 || 3			*		$10^9\Omega$ || pF
Common-Mode Impedance			10 || 3			*		$10^9\Omega$ || pF
OFFSET VOLTAGE, RTO[4]								
Initial at +25°C[5]			±(0.02G +1)	±(0.04G +2)		±(0.01G +1)	±(0.02G +2)	mV
vs Temperature	-25°C to +85°C		(±0.0015G ±0.03G_2)	(±0.003G ±0.05G_2)		(±0.0005G ±0.01G_2)	(±0.001G ±0.02G_2)	mV/°C
vs Time			(±0.001G ±0.01G_2)			*		mV/mo
vs Supply			(±0.002G ±0.04G_2)			*		mV/V
vs Gain[6]	With trimming		±1	±2		*	*	mV
INPUT BIAS CURRENT								
Initial	+25°C		±15	±50		±5	±20	nA
vs Temperature	-25°C to +85°C		±0.3			*		nA/°C
vs Supply Voltage			±0.1			*		nA/V
INPUT DIFFERENCE CURRENT								
Initial	+25°C		±15	±50		±5	±20	nA
vs Temperature	−25°C to +85°C		±0.5			*		nA/°C
vs Supply Voltage			±0.1			*		nA/V
INPUT NOISE								
Voltage	$R_{SOURCE} \leq 5k\Omega$							
0.01Hz to 10Hz	G = 1024		1.4			*		μV, p-p
10Hz to 1kHz			1.0			*		μV, rms
Current								
0.01Hz to 10Hz			70			*		nA, p-p
10Hz to 1kHz			20			*		nA, rms
COMMON-MODE REJECTION								
DC, 1kΩ Source Imbalance								
G = 1, 2		80	90		90	100		dB
G = 4 to 6		90	100		100	110		dB
G = 32 to 1024		100	114		110	114		dB
60Hz, 1kΩ Source Imbalance								
G = 1, 2		80	86		*	*		dB
G = 4 to 16		90	96		*	*		dB
G = 32 to 1024		100	106		*	*		dB
DYNAMIC RESPONSE								
±3dB Response	Small Signal							kHz
G = 1			100			*		kHz
G = 32 to 128			40			*		kHz
G = 256 to 1024			10			*		kHz
±1% Response	Small Signal							
G = 1			40			*		kHz
G = 32 to 128			8			*		kHz
G = 256 to 1024			3			*		kHz
Slew Rate	G = 1	0.2	0.5		*	*		V/μsec
Settling Time	G = 128							
to 1%			75			*		μsec
to 0.1%			100			*		μsec
to 0.01%			200			*		μsec

ELECTRICAL (CONT)

Typical at +25°C, unless otherwise noted.

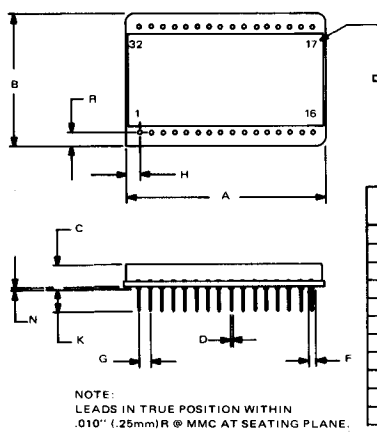
PARAMETER	CONDITIONS	3606A[1] MIN	3606A[1] TYP	3606A[1] MAX	3606B[1] MIN	3606B[1] TYP	3606B[1] MAX	UNITS
LOGIC VOLTAGES								
"0" Level[7]			0	+0.4		*	*	V
"1" Level[7]		+2.4	+5.0		*	*		V
Absolute Max	No damage			+7			*	V
ANALOG SUPPLY								
Rated Voltage			±15			*		VDC
Voltage Range, Derated Performance		±8		±18	*		*	VDC
Current, quiescent			±10	±20		*	*	mA
DIGITAL SUPPLY								
Rated Voltage			+5			*		VDC
Voltage Range		+4.5		+5.5	*		*	VDC
Current, quiescent			10			*		mA
TEMPERATURE RANGE								
Specification		-25		+85	*		*	°C
Storage		-40		+100	*		*	°C

*Specifications same as 3606A.

NOTES:
1. Specify 3606AG or 3606BG for ceramic package and 3606AM or 3606BM for metal package—see below.
2. $G = G_1 \times G_2$.
3. Nonlinearity is the maximum peak deviation from the best straight-line as a percent of full scale peak-to-peak output.
4. RTO = Referred To Output. May be referred to input by dividing by gain G.
5. May be adjusted to zero.
6. Trimmed according to Figure 8.
7. All digital inputs are 1 TTL unit load.

MECHANICAL

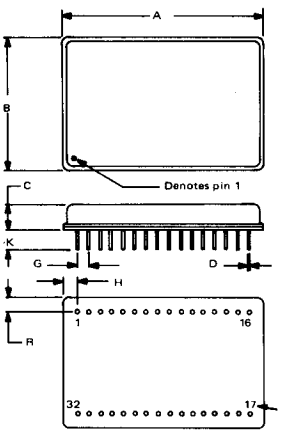
"G" PACKAGE



NOTE:
LEADS IN TRUE POSITION WITHIN .010" (.25mm) R @ MMC AT SEATING PLANE.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.700	1.760	43.18	44.70
B	1.120	1.160	28.45	29.46
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.110	.130	2.79	3.30

"M" PACKAGE



NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.720	1.760	43.69	44.70
B	1.120	1.160	28.45	29.46
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.100	.140	2.54	3.56
K	.150	.300	3.81	7.62
L	.900 BASIC		22.86 BASIC	
R	.100	.140	2.54	3.56

Pin numbers shown for reference only. Numbers may not be marked on package.

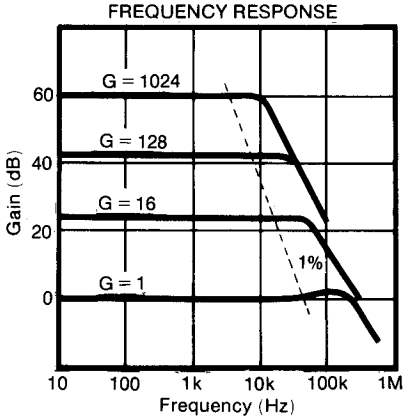
PIN DESIGNATIONS

PIN NO.	DESIG.	FUNCTION	PIN NO.	DESIG.	FUNCTION
1	-V	-15V Analog Supply	17	D_0	Digital Input, LSB
2	-IN	Inverting Input	18	D_1	Digital Input, next LSB
3	J_1	Output of A_3	19	G	Latch
4	(None)	Optional A_4 Offset Trim	20	DIG GND	Digital Ground
5	ΣJ	Summing Junction of A_4	21	D_2	Digital Input, next MSB
6	(None)	Optional A_4 Offset Trim	22	D_3	Digital Input, MSB
7	F	Low-Pass Filter Pin	23	+5	+5 Digital Supply
8	J_2	Input to A_4	24	(None)	No Internal Connection
9	R_1	Output Reference	25	(None)	No Internal Connection
10	O	Output	26	Gain	Optional External Gain
11	S_1	Sense G = 1	27	Gain	Optional External Gain
12	S_2	Sense G = 4	28	(None)	Input CMV
13	S_3	Sense G = 2	29	+IN	Noninverting Input
14	R_2	Output Reference	30	+V	+15V Analog Supply
15	ANA GND	Analog Ground	31	BAL	Optional Input Stage
16	(None)	No Internal Connection	32	BAL	Offset Null

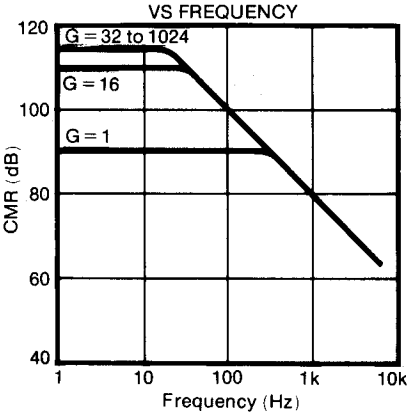
TYPICAL PERFORMANCE CURVES

Typical at +25°C unless otherwise noted.

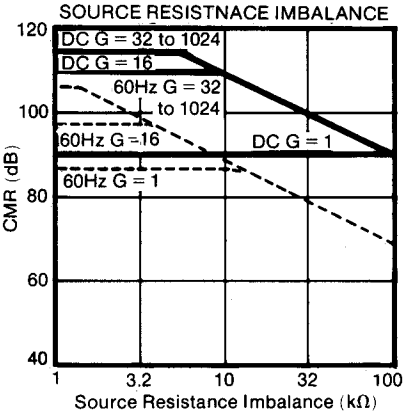
SMALL SIGNAL FREQUENCY RESPONSE



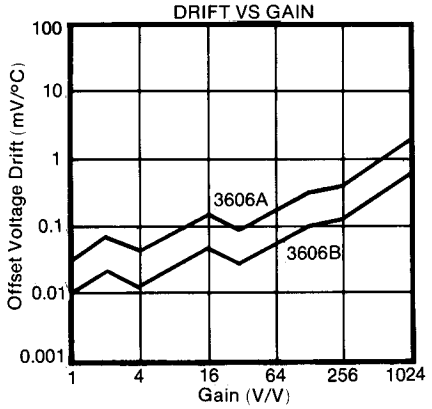
COMMON-MODE REJECTION VS FREQUENCY



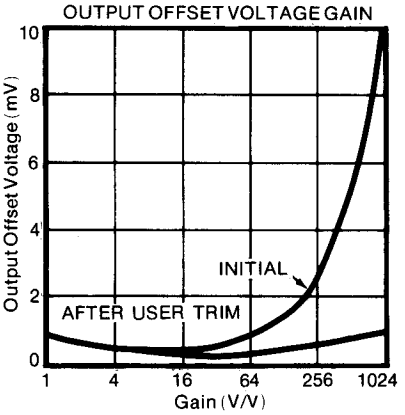
COMMON-MODE REJECTION VS SOURCE RESISTNACE IMBALANCE



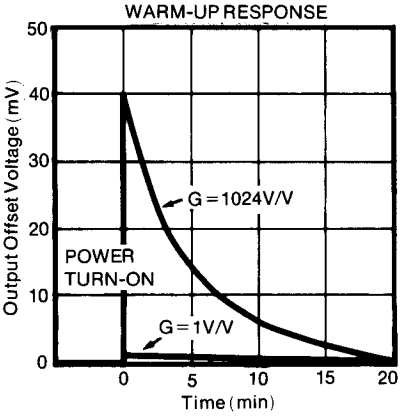
OUTPUT OFFSET VOLTAGE DRIFT VS GAIN



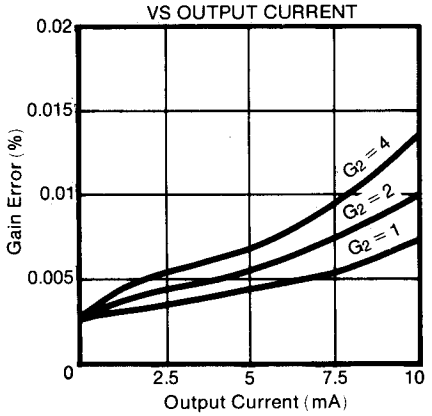
OUTPUT OFFSET VOLTAGE GAIN



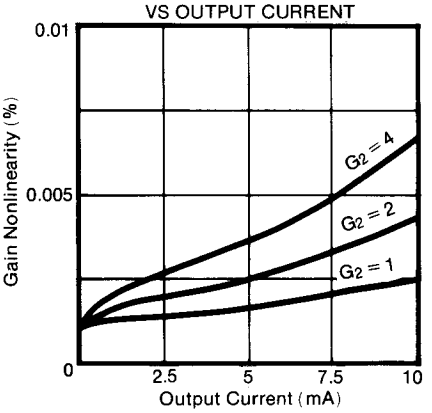
WARM-UP RESPONSE



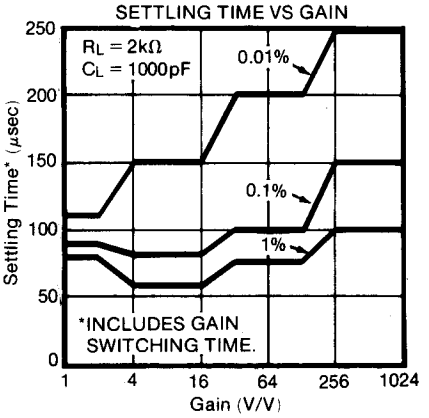
OUTPUT STAGE GAIN ERROR VS OUTPUT CURRENT



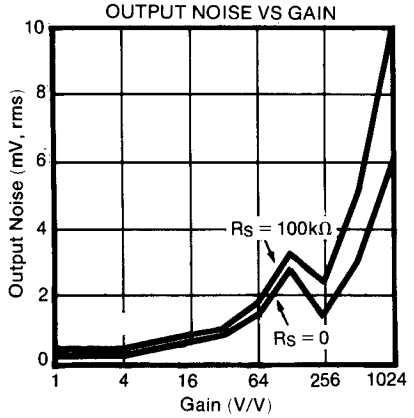
OUTPUT STAGE GAIN NONLINEARITY VS OUTPUT CURRENT



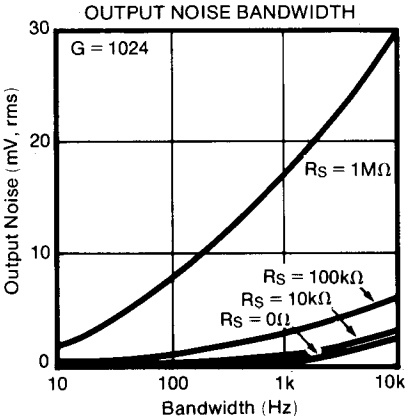
SETTLING TIME VS GAIN



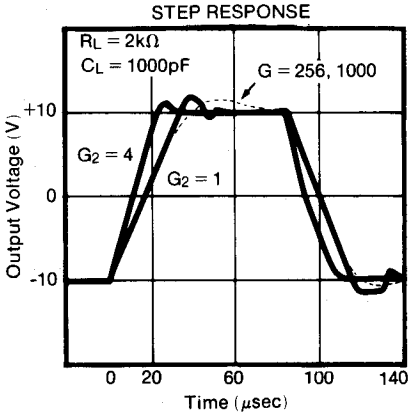
WIDEBAND OUTPUT NOISE VS GAIN



OUTPUT NOISE BANDWIDTH



STEP RESPONSE



INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

Figure 2 shows the proper analog and digital power supply connections. The analog supplies should be decoupled with 1μF tantalum and 1000pF ceramic capacitors as close to the amplifier as possible. Because the amplifier is direct-coupled it must have a ground return path for the bias currents associated with the amplifier inputs at pins 2 and 29. If the ground return path is not inherent in the signal source (floating source) it must be provided externally. The ground return resistance (R_{GR}) should be kept as low as practical. An upper limit of approximately 50MΩ is established by the input bias currents of the amplifier and its common-mode voltage.

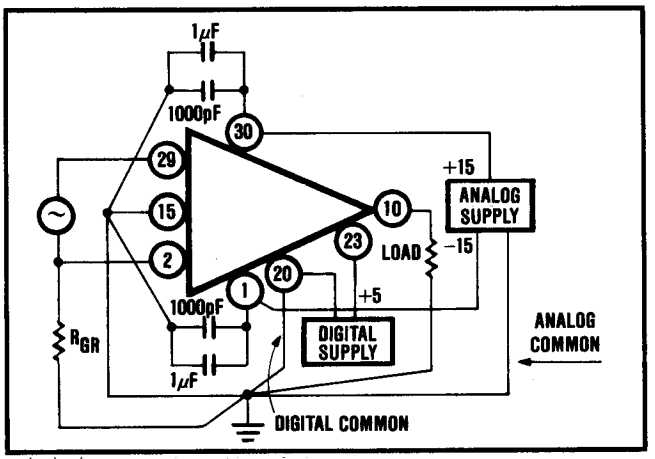


FIGURE 2. Power Supply and Ground Connections.

SIGNAL CONNECTIONS

Basic signal connections are shown in Figure 3. The connection to pin 14 completes the difference amplifier of A_3 (see Figure 1). The 3 to 8 jumper connects the output stage. The pin 9 connection provides a divide-by-two attenuator for the A_4 stage. This is necessary to limit the signal on the output stage switches to maintain signal linearity. The pin 11, 12 and 13 connections to pin 10 close the feedback loop around A_4.

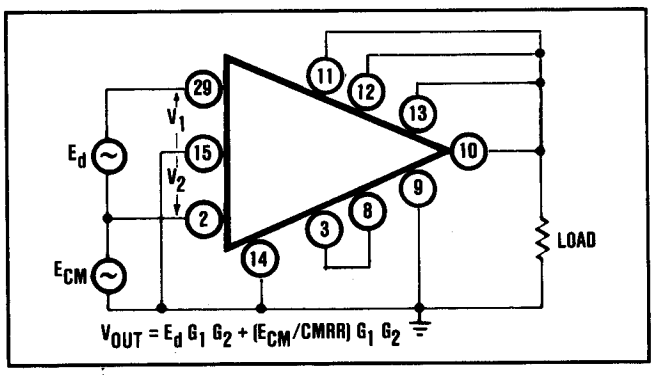


FIGURE 3. Basic Signal Connections.

In the equation shown in Figure 3, G_1 is the input stage gain and G_2 is the output stage gain. CMRR is the common-mode rejection ratio [CMR (in dB) = 20 log CMRR (in V/V)]. Common-mode voltage shown as E_{CM} is actually the average of the two voltages appearing at the two inputs (pins 29 and 2) with respect to pin 15 (V_1 and V_2).

GAIN SETTING

Gain is determined by a 4-bit digital word applied to the input D_0 through D_3 (see Figure 1). Pin 19 provides a latch function for the inputs. When pin 19 is a logic 0, changes on the D_0 through D_3 inputs are inhibited. Pin 19 should be at +5V if the latch is not used.

A gain state truth table is shown in Table I. Gains are determined by the resistor networks shown in Figure 1. For the state D_3, D_2 = 0, 0, the input stage gain is a function of the gain setting resistor R_G connected between pins 26 and 27. If gains of 1, 2 and 4 are desired, no connection should be made to pins 26 and 27 and the resistance across these pins should be kept high with respect to 40kΩ (> 400MΩ).

Gain accuracy is established by laser-trimming the thim-film resistor networks during assembly. No external, user trimming is required.

OUTPUT OFFSET

Output offset may be varied by either of two methods shown in Figure 4. Sources at pin 9 and pin 14 apply voltages to the noninverting inputs of A_4 and A_3 respectively (see Figure 1). Since the output stage gain occurs after these points, the output voltage bias established with V_{R1} and V_{R2} will vary with the output gain, G_2. Sources connected at pins 9 and 14 must have resistances low with respect to 10kΩ in order not to disturb gain accuracy and common-mode rejection.

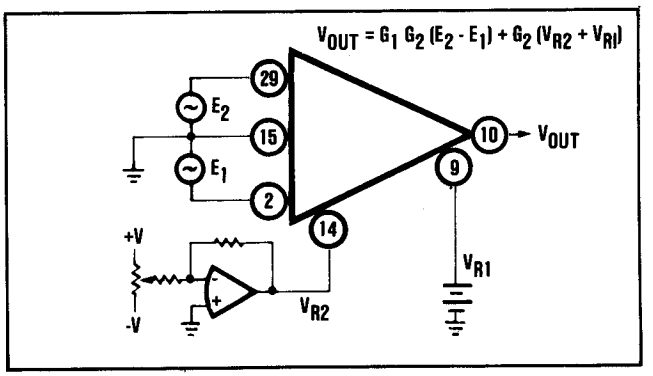


FIGURE 4. Output Offsetting.

LOW-PASS FILTER

For low frequency signals, system performance may be improved by reducing noise bandwidth in the amplifier. This may be accomplished with the addition of one or two external capacitors as shown in Figure 5. C_2 is connected to a 10k/10k attenuator and C_1 is connected as a feedback element across A4 (see Figures 1 and 5). The transfer function is:

$$\frac{V_O}{V_{IN}} = \left[\frac{10 \times 10^3}{100 \times 10^6\, S(C_2 + 330 \times 10^{-12}) + 20 \times 10^3}\right]\left[1 + \frac{10 \times 10^3}{10 \times 10^3\, R_1\, SC_1 + R_1}\right]$$

TABLE I. Gain State Truth Table.

Digital Inputs (G_1)		(G_2)		G_1 (A_1 and A_2) (Pins 2 & 29 to 3)	G_2 (A_4) (Pin 8 to Pin 10)	$G_1 \cdot G_2$ ($R_G^* = \infty$)	$G_1 \cdot G_2$ ($R_G^* \neq \infty$)
D_3	D_2	D_1	D_0				
0	0	0	0	$1 + 40k/R_G$	1	1	$1(1 + 40k/R_G)$
0	0	0	1		2	2	$2(1 + 40k/R_G)$
0	0	1	0		4	4	$4(1 + 40k/R_G)$
0	0	1	1		4	4	$4(1 + 40k/R_G)$
0	1	0	0	4	1	4	4
0	1	0	1		2	8	8
0	1	1	0		4	16	16
0	1	1	1		4	16	16
1	0	0	0	32	1	32	32
1	0	0	1		2	64	64
1	0	1	0		4	128	128
1	0	1	1		4	128	128
1	1	0	0	256	1	256	256
1	1	0	1		2	512	512
1	1	1	0		4	1024	1024
1	1	1	1		4	1024	1024

*R_G connected between pins 26 and 27.

The first term is a first order filter. The second term is more complex. R_1 varies with the output stage gain - 1.4k for $G_2 = 4$ (see Figure 1). The "1 + ..." nature of the transfer function prevents a true first order filter rolloff.

For most applications, the first order low-pass filter obtained by C_2 provides sufficient filtering. The value C_2 required for a desired cutoff frequency (f_2 in Hz) is obtained by the equation shown in Figure 5.

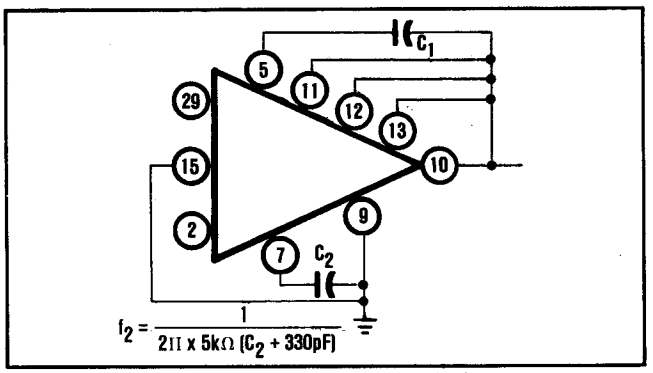


FIGURE 5. Low-Pass Filter Connections.

LARGER OUTPUT CURRENT

The output current rating of the 3606 is a minimum of ±5mA. The linearity of the gain is affected by output current. See Typical Performance Curves. Optimum linearity is achieved with $I_O \leq$ 1mA, $I_O \leq$ 5mA is acceptable. Above 5mA it may be desirable to use a power or current booster as shown in Figure 6. Burr-Brown's 3329 will provide ±100mA output while Burr-Brown's 3553 will supply ±200mA. When either booster is placed inside the feedback loop as shown, the booster's offset voltage produces no significant errors since it is divided by the open-loop gain of the output stage.

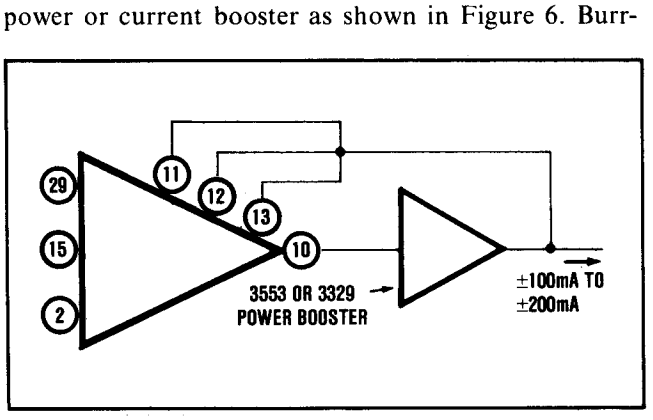


FIGURE 6. Output Current Booster.

GUARD DRIVE CONNECTIONS

Use of the guard drive connection shown in Figure 7 can improve system common-mode rejection when the distributed capacitance of the input lines is significant. The

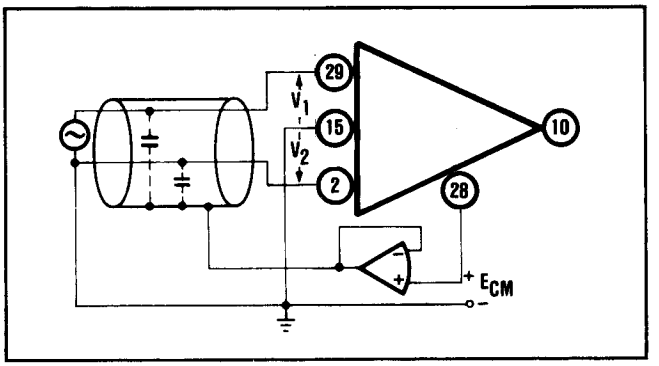


FIGURE 7. Guard Drive Connections.

common-mode voltage which appears on the input lines and on pins 29 and 2 is computed by the 3606 [(V_1 + V_2)/2] and appears at pin 28. It is then fed back to the shield so that the voltage across the distributed capacitances is minimized. This reduces the common-mode current and improves common-mode rejection. The operational amplifier in the voltage follower configuration is used to supply more current than can be obtained from the 20k resistors connected internally to pin 28 (see Figure 1).

OFFSET TRIM

Offset voltages of the 3606 are reduced by laser-trimming during assembly. This reduces the initial offset voltage and the offset voltage change with gain change to levels that are acceptable for most applications. For more critical applications the offset voltages can be externally

nulled to zero. The following steps should be followed (see Figure 8).

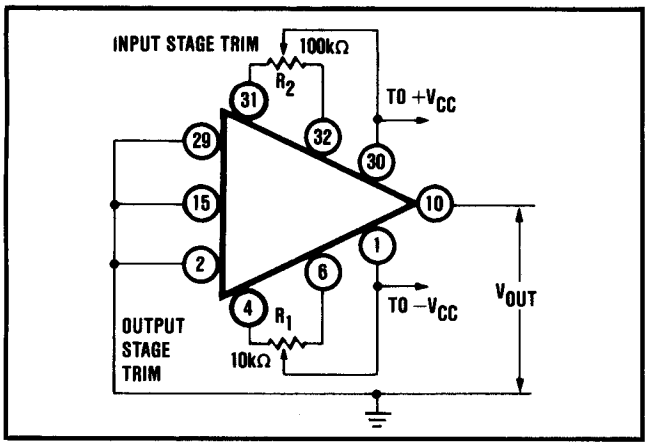


FIGURE 8. Optional Offset Trim.

1. Adjust both R_1 and R_2 to mid-range.
2. Set the gain to minimum (1V/V).
3. Adjust R_1 to make V_{OUT} equal zero.
4. Set the gain to maximum (1024V/V).
5. Adjust R_2 to make V_{OUT} equal zero.

By using this technique, the change in output offset voltage caused by a gain change of 1V/V to 1024V/V may be reduced to, typically 1mV instead of 10mV with no external trimming. Trimming may cause the offset voltage drift vs temperature to increase slightly.

APPLICATIONS

A typical application of 3606 in a microcomputer based data acquisition system is shown in the block diagram below.

The purpose of this system is to be able to acquire data from a specific analog input channel, suitably condition it (amplify it and convert it to digital form) and store it or transmit it for further processing.

Initially the Microcomputer loads the RAM (random access memory) with the required coding for various desired gains via Data Bus. The coding associates the gain state truth table for 3606 with corresponding address locations in the computer memory. So when the computer puts out an instruction to multiplex a specific analog input channel through the multiplexer via the Address Bus, the RAM also receives the same address information and puts out corresponding gain code to the PGIA 3606. The 3606 amplifies the multiplexed signal by the programmed gain value, and outputs it to S/H (sample and hold). The S/H holds the output value when it receives the control signal from the computer and the A/D converts it and outputs it to the computer via the Data Bus under computer control.

The PGIA 3606 allows the system user to modify and reprogram gain values for different analog input channels merely by changing the software computer program. Since different dedicated instruments are not required for various input channels, the PGIA also saves space and overall system costs.

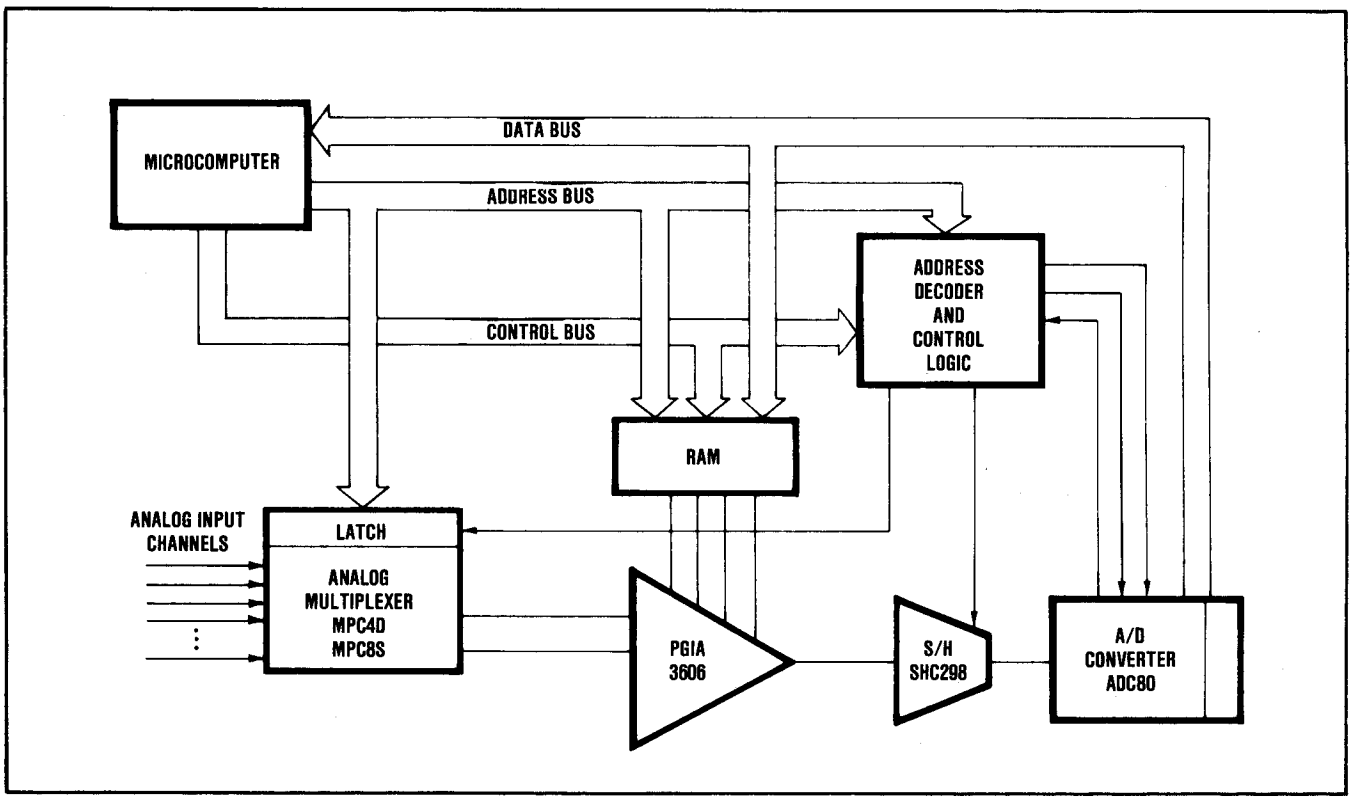


FIGURE 9. Use of 3606 in Data Acquisition System.

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