
MSC7110-01/7112-01

12-Segment × 16-Digit or 16-Segment × 12-Digit Display Controller/Driver

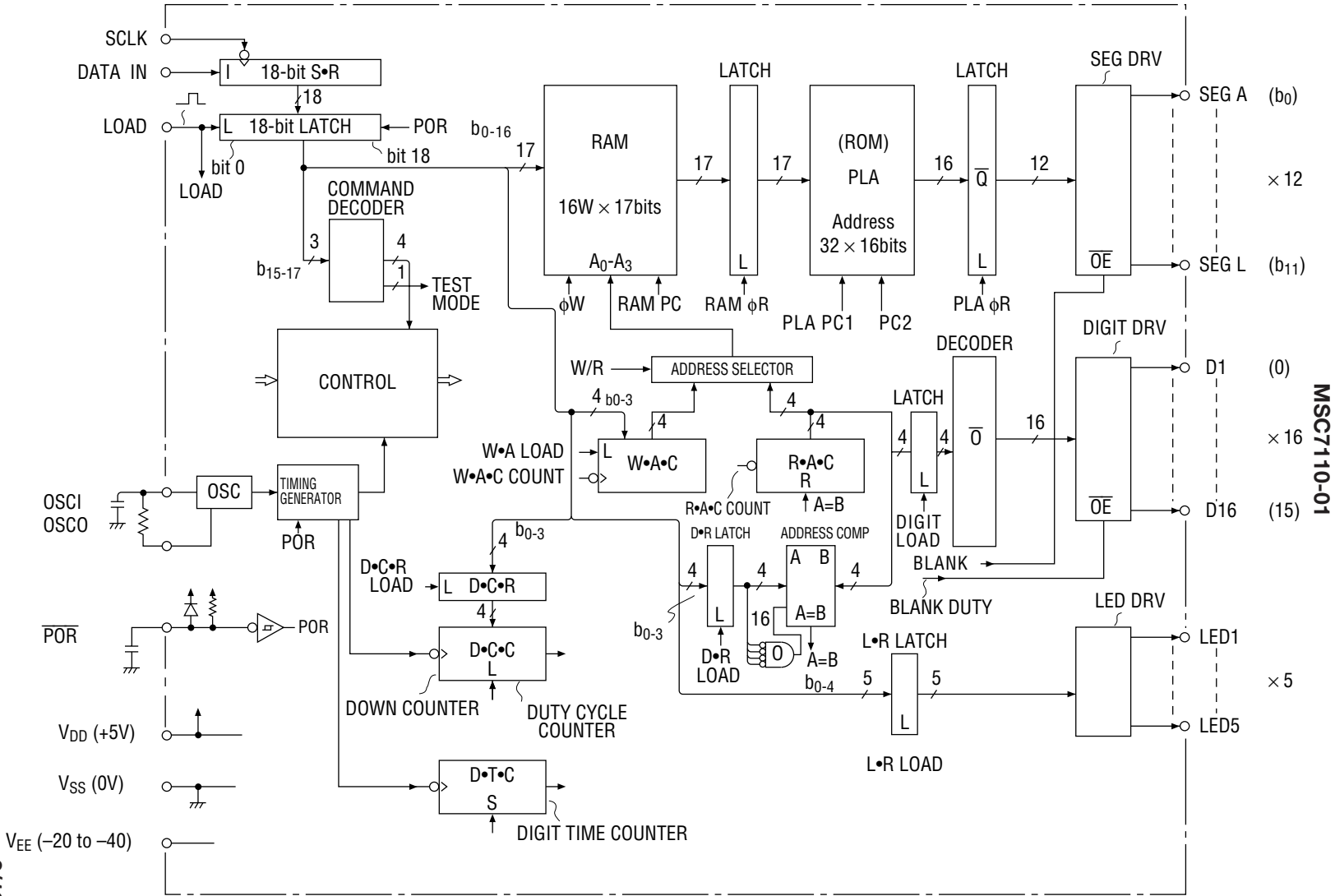
GENERAL DESCRIPTION

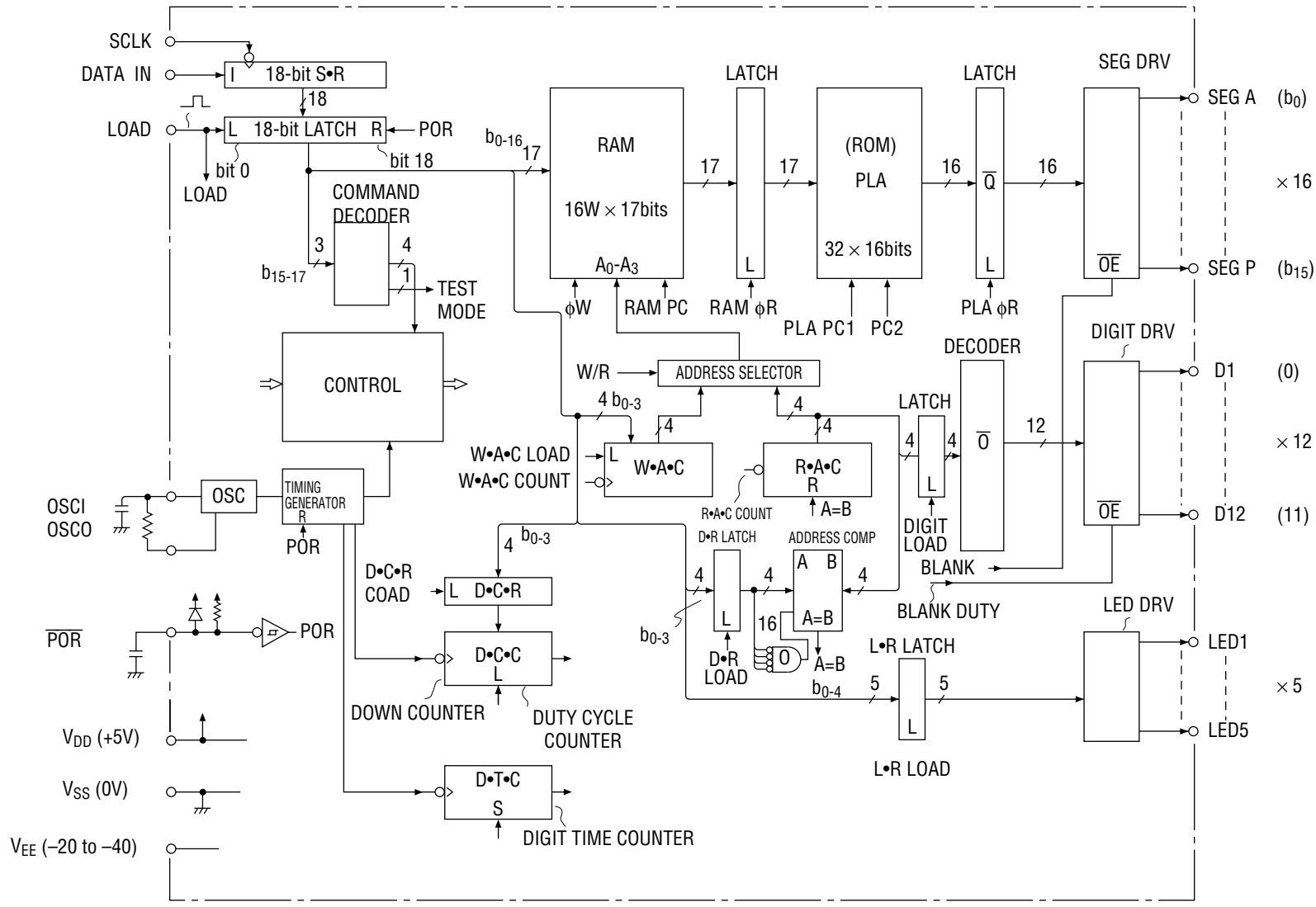
The MSC7110-01/7112-01 is a display controller to display the timer of video tape recorder, channel operation, and other information by a vacuum fluorescent display tube. Display data is input by serial transfer from microcontroller.

FEATURES

- Provides the interface with a microcontroller by three signal lines. : DATA IN, CLOCK, and LOAD
- Driver output can directly be connected to a vacuum fluorescent display tube without a pull-down resistor.
- Display is turned on by dynamic drive mode.
- The number of display digits are programmable in the range of : 1 to 12 digits (MSC7112-01)
1 to 16 digits (MSC7110-01)
- 12-segment driver output : 16 driver outputs (MSC7112-01)
12 driver outputs (MSC7110-01)
- The LED drivers can turn on 5 outputs statically.
- RAM data can directly be displayed.
- The brightness adjustment is programmable and brightness can be adjusted every 1/15 step.
- Built-in power-on-reset circuit
- The vacuum fluorescent display tube driver outputs high withstand voltage : $V_{DD}-V_{EE}=45V$ (max).
- Logic supply voltage : $V_{DD}=5V \pm 10\%$
- Package options:
 - 42-pin plastic SDIP (SDIP42-P-600-1.778) : (Product name : MSC7112-01SS)
 - 44-pin plastic QFP (QFP44-P-910-0.80-2K) : (Product name : MSC7110-01GS-2K/MSC7112-01GS-2K)

BLOCK DIAGRAM

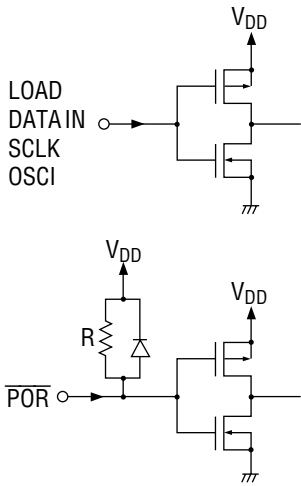




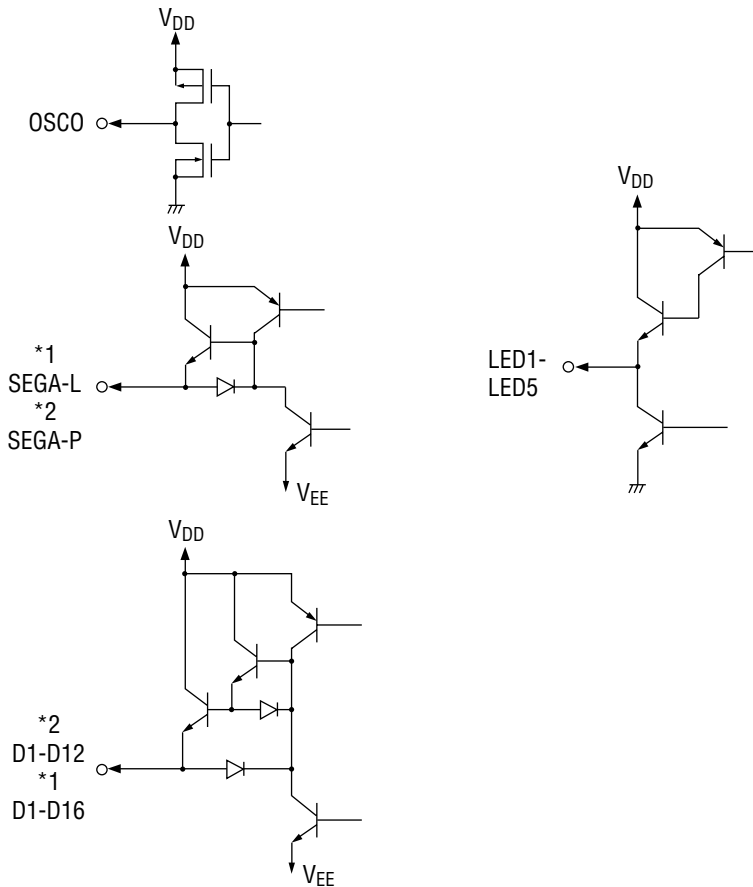
MSC7112-01

INPUT AND OUTPUT CONFIGURATION

Input Pin



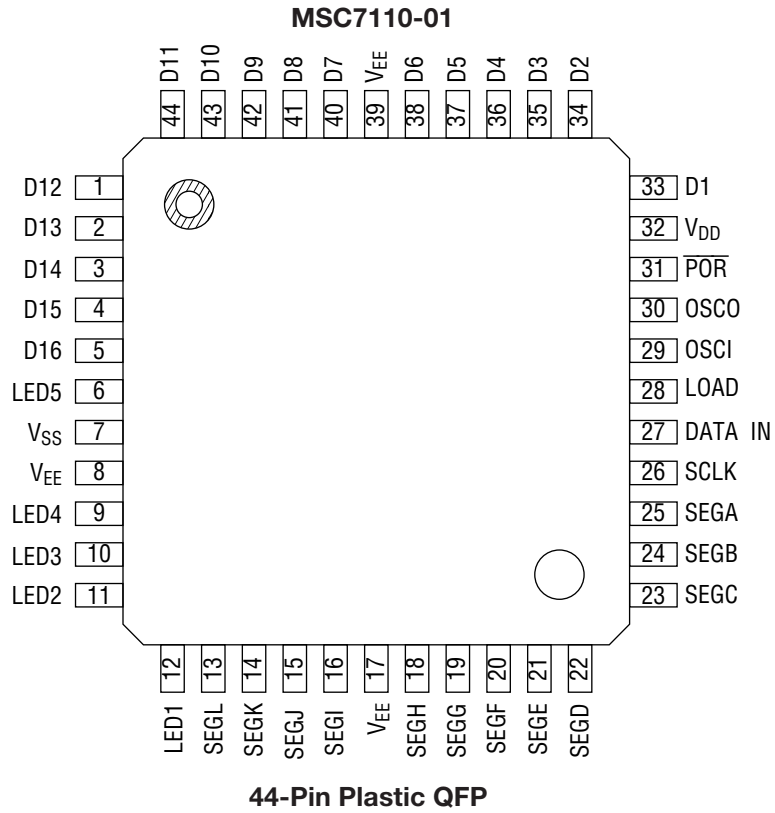
Output Pin



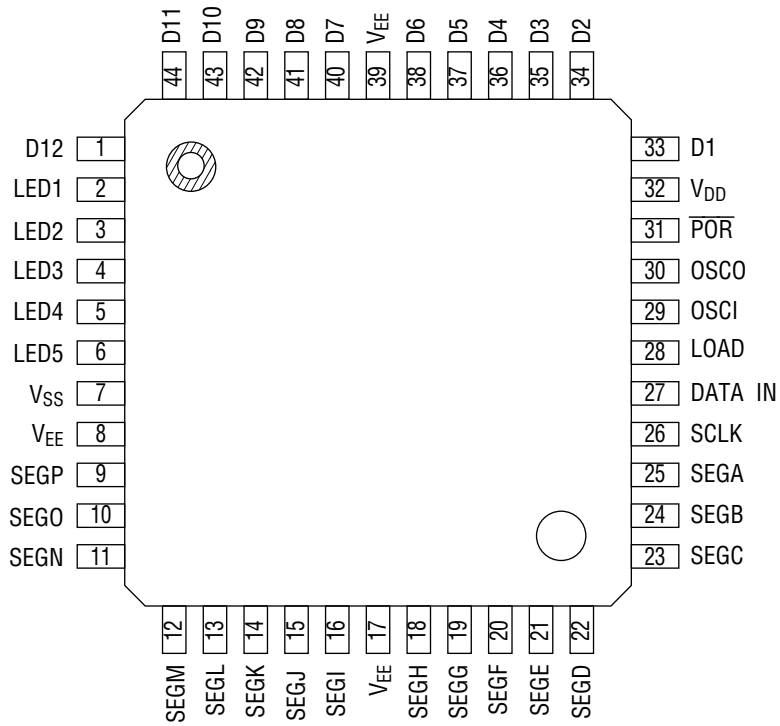
*1 MSC7110-01

*2 MSC7112-01

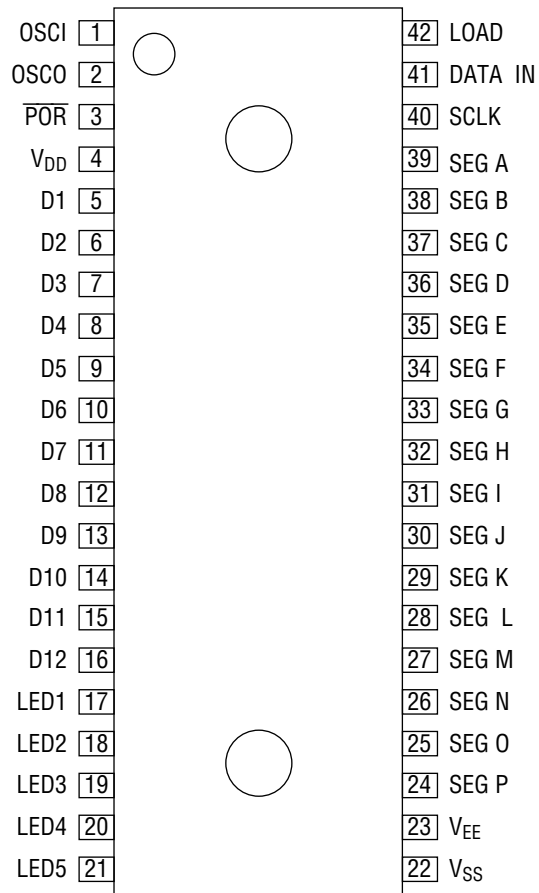
PIN CONFIGURATION (TOP VIEW)



MSC7112-01



MSC7112-01



42-PIN PLASTIC SDIP

Note: The product name actually printed on the product is "C7112-01".

PIN DESCRIPTION

Symbol	Number of Pins	Type	Connected to	Description
V _{DD}	1	—	Power source	V _{DD} -V _{SS} : Supply voltage for internal logic
V _{SS}	1	—		V _{DD} -V _{EE} : Supply voltage for VF display tube driving circuit logic
V _{EE}	1	—		
DATA IN	1	I	Microcontroller	Input of display data of the shift register Input from the MSB (positive logic).
SCLK	1	I		Shift clock of the shift register. Data is shifted at the falling edge of SCLK.
LOAD	1	I		Latch clock input for display data. When this pin is at a "H" level, the data is not latched to pass through the latch circuit. When the pin is at a "L" level, the data when the pin is at the "H" level is latched.
$\overline{\text{POR}}$	1	I Schmitt with pull-up resistor using diode	—	Internal logic reset input upon power-on. During reset, the 18-bit internal latch, duty cycle register, digital register, LED register, and write/read address register are all reset, and the outputs of SEGA to SEGP(*a), D1 to D12 (*b), and LED1 to LED5 go off. Connecting of an external capacitor to the pin allows power-on reset.
OSC I	1	I	—	Input for oscillation circuit When an external resistor and a capacitor are connected, an oscillation circuit is formed. C=100pF, R=47kΩ f _{OSC} =235kHz±20%
OSC O	1	O		
SEGA-L	12 *1	0	Anode side of VF display tube	Output for driving anode electrodes of VF display tube. The output is complementary.
SEGA-P	16 *2	0		
D1-D12	12 2	0	Grid side of VF display tube	Output for driving grid electrodes of VF display tube. The output is complementary.
D1-D16	16 *1	0		
LED1-LED5	5	0	LED	LED driving output. The output is complementary.

*a SEGA to SEGL in case of MSC7110-01

*b D1 to D16 in case of MSC7110-01

*1 In case of MSC7110-01

*2 In case of MSC7112-01

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Range	Unit
Supply Voltage (1)	V_{DD}	—	-0.3 to +6.5	V
Supply Voltage (2)	$V_{DD}-V_{EE}$	—	0 to 50	V
Input Voltage	V_I	—	-0.3 to $V_{DD}+0.3$	V
Power Dissipation	P_D	$T_a \leq 25^\circ\text{C}$	to 500	mW
Storage Temperature	T_{STG}	—	-55 to +150	$^\circ\text{C}$
Output Current	I_{O1}	All SEG output	-10	mA
	I_{O2}	All DIGIT output	-60	mA
	I_{O3}	LED1-LED5	-20	mA

RECOMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Supply Voltage (1)	V_{DD}	—	4.5 to 5.5	V
Supply Voltage (2)	$V_{DD}-V_{EE}$	—	25 to 45	V
Oscillation Frequency	f_{OSC}	—	200 to 500	kHz
Operating Temperature	T_{OP}	—	-20 to +75	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS

DC Characteristics

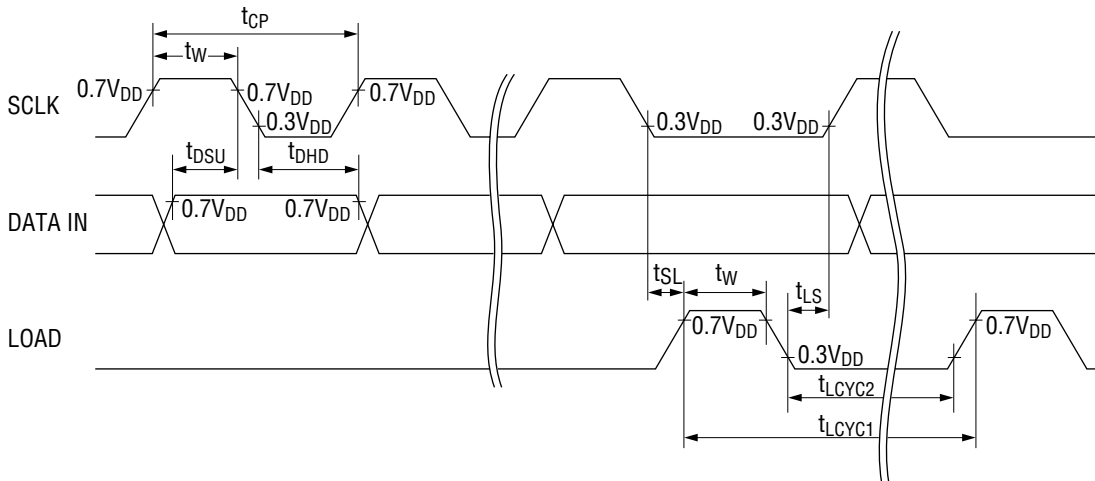
($V_{DD}-V_{EE}=45\text{V}$, $V_{DD}=5\text{V} \pm 10\%$, $T_a=-20$ to $+75^\circ\text{C}$)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
High Level Input Voltage	V_{IH}	—	$0.7V_{DD}$	—	—	V	All input
Low Level Input Voltage	V_{IL}	—	—	—	$0.3V_{DD}$	V	All input
High Level Input Current	I_{IH}	$V_{DD}=5.5\text{V}$, $V_I=V_{DD}$	—	—	1	μA	All input
Low Level Input Current (1)	I_{IL1}	$V_{DD}=5.5\text{V}$, $V_I=0\text{V}$	—	—	-1	μA	All input except POR
Low Level Input Current (2)	I_{IL2}	$V_{DD}=5.5\text{V}$, $V_I=0\text{V}$	-27	-55	-110	μA	$\overline{\text{POR}}$
High Level Output Voltage (1)	V_{OH1}	$V_{DD}=4.5$, $I_{OH}=-6\text{mA}$	$V_{DD}-2.2$	$V_{DD}-1.5$	—	V	All SEG output
Low Level Output Voltage (1)	V_{OL1}	$V_{DD}=4.5$, $I_{OL}=0.2\text{mA}$	—	$V_{EE}+0.8$	$V_{EE}+1.3$	V	All SEG output
High Level Output Voltage (2)	V_{OH2}	$V_{DD}=4.5$, $I_{OH}=-30\text{mA}$	$V_{DD}-2.9$	$V_{DD}-2.3$	—	V	All DIGIT output
Low Level Output Voltage (2)	V_{OL2}	$V_{DD}=4.5$, $I_{OL}=0.2\text{mA}$	—	$V_{EE}+0.8$	$V_{EE}+1.3$	V	All DIGIT output
High Level Output Voltage (3)	V_{OH3}	$V_{DD}=4.5$, $I_{OH}=-10\text{mA}$	$V_{DD}-1.5$	—	—	V	LED1-LED5
Low Level Output Voltage (3)	V_{OL3}	$V_{DD}=4.5$, $I_{OL}=0.1\text{mA}$	—	—	0.5	V	LED1-LED5
Current Consumption	I_{DD}	$V_{DD}=5.5\text{V}$, No load $f_{OSC}=245\text{kHz}$	—	8.5	15	mA	—

AC Characteristics

 $(V_{DD}=5V\pm 10\%, T_a=-20 \text{ to } +75^\circ\text{C})$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK Cycle Time	t_{CP}	—	2	—	—	μs
SCLK, LOAD Pulse Width	t_W	—	1	—	—	μs
Data Setup Time	t_{DSU}	—	500	—	—	ns
Data Hold Time	t_{DHD}	—	500	—	—	ns
SCLK-LOAD Time	t_{SL}	—	2	—	—	μs
LOAD-SCLK Time	t_{LS}	—	2	—	—	μs
LOAD Cycle Time 1*	t_{LCYC1}	$f_{OSC}=245\text{kHz}$	205	—	—	μs
LOAD Cycle Time 2	t_{LCYC2}	$f_{OSC}=245\text{kHz}$	200	—	—	μs

* $t_{LCYC1} > 16/f_{OSC}$ must be satisfied.

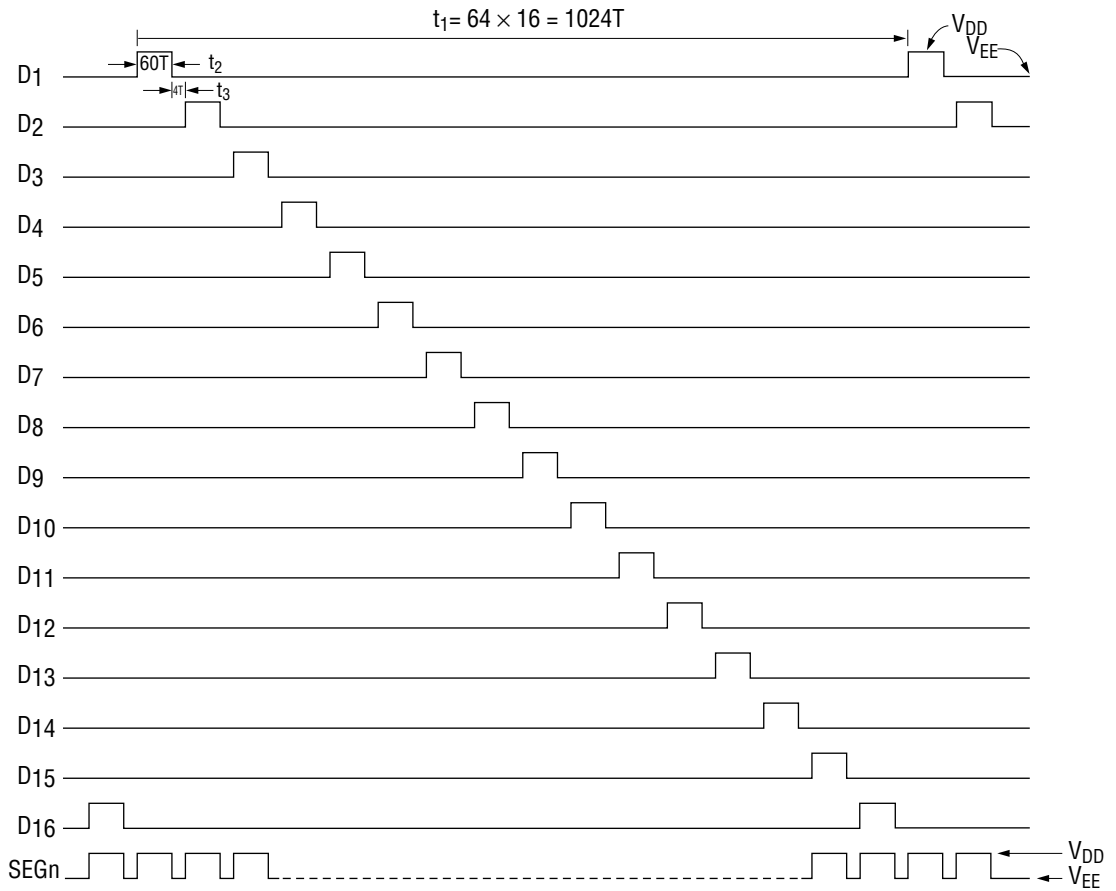
Oscillation Characteristics

 $(V_{DD}=5V, V_{DD}-V_{EE}=25V \text{ to } 45V, T_a=-20 \text{ to } +75^\circ\text{C})$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Oscillation Frequency	f_{OSC}	$C=100\text{pF}, R=47\text{k}\Omega$	188	235	282	kHz	OSCI, OSCO

TIMING DIAGRAM

16-digit display



t_1 =Frame cycle	f_{OSC} =245kHz
t_2 =Display timing	t_1 =4.096ms
t_3 =Blank timing	t_2 =240 μ s
	t_3 =16 μ s
	$T=1/f_{OSC}$

FUNCTION DESCRIPTION

Command Description

Command	Function	Input data																	
		MSB b ₁₇	b ₁₆	b ₁₅	b ₁₄	b ₁₃	b ₁₂	b ₁₁	b ₁₀	b ₉	b ₈	b ₇	b ₆	b ₅	b ₄	b ₃	b ₂	b ₁	LSB b ₀
DATA DISPLAY	The RAM data is output directly to the SEGA to SEGP pins (Positive logic)	0	0	*1 SEGP	*1 SEGO	*1 SEGN	*1 SEGM	SEGL	SE GK	SE GJ	SE GI	SE GH	SE GG	SE GF	SE GE	SE GD	SE GC	SE GB	SE GA
L.R LOAD	Display data is set in the LED register and output to the LED1 to LED5 pins (Positive logic)	1	0	0	×	×	×	×	×	×	×	×	×	×	LED5	LED4	LED3	LED2	LED1
D.R LOAD	The number of digits is set in the digit register.	1	0	1	0	×	×	×	×	×	×	×	×	×	×	2 ³	2 ²	2 ¹	2 ⁰
W.A.C LOAD	The write address is set in the write address counter. (The write position is set.)	1	1	0	×	×	×	×	×	×	×	×	×	×	×	2 ³	2 ²	2 ¹	2 ⁰
D.C.R LOAD	The duty value is set in the duty cycle register.	1	1	1	×	×	×	×	×	×	×	×	×	×	×	2 ³	2 ²	2 ¹	2 ⁰
TEST MODE LOAD	The TEST mode is set.	1	0	1	1	×	×	×	×	×	×	×	×	×	×	×	×	×	×

× : Don't Care

*1: Ignored in the case of MSC7110-01.

Relation between write address and digit output

Write address count	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Corresponding digit output	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	*1	*1	*1	*1

*1: Ignored in the case of MSC7112-01

Inputting Display Data

LED display

Display data is output to the LED1 to LED5 pins in correspondence with each bit by executing the L. RLOAD command. Input data uses positive logic. When the data is 1, the LED lights. When the data is 0, the LED goes off.

VF display (RAM direct display)

Set optional data in the digit register and the duty register, and execute the W.A.C LOAD command to set the display digit position. Execute the DATA DISPLAY command to write the b0 to b15 (*1) display data in the RAM. The write address counter is incremented by one. The write address counter counts sequentially 0, 1, 2,-----, 14, 15, 0, 1, ----- regardless of the value of the digit register.

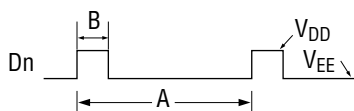
*1 : b₀ to b₁₁ display data in the case of MSC7110-01.

Brightness Adjustment

The brightness can be adjusted by using the values of the duty cycle register (D.C.R) and the digit register (D.R). The value of the duty cycle register changes the pulse width (B) at the D1 to D16 output pins, and the value of the digit register changes the cycle (A).

The table below gives the relation between the value of the duty cycle register and the duty. When all the values of the duty cycle register are 0 (in the case of 16-digit display), the display is blank.

D.C.R				DUTY	D.C.R				DUTY	D.C.R				DUTY	D.C.R				DUTY
b ₃	b ₂	b ₁	b ₀	B/A	b ₃	b ₂	b ₁	b ₀	B/A	b ₃	b ₂	b ₁	b ₀	B/A	b ₃	b ₂	b ₁	b ₀	B/A
0	0	0	0	—	0	1	0	0	16/1024	1	0	0	0	32/1024	1	1	0	0	48/1024
0	0	0	1	4/1024	0	1	0	1	20/1024	1	0	0	1	36/1024	1	1	0	1	52/1024
0	0	1	0	8/1024	0	1	1	0	24/1024	1	0	1	0	40/1024	1	1	1	0	56/1024
0	0	1	1	12/1024	0	1	1	1	28/1024	1	0	1	1	44/1024	1	1	1	1	60/1024



$A=64 \times n=64 \times 16=1024$
 n : Number of display digits

Number of Display Digits

The number of display digits is set by the digit register. The number of display digits ranges from 1 to 16 (*1). The value of the digit register and the number of digits are as follows:

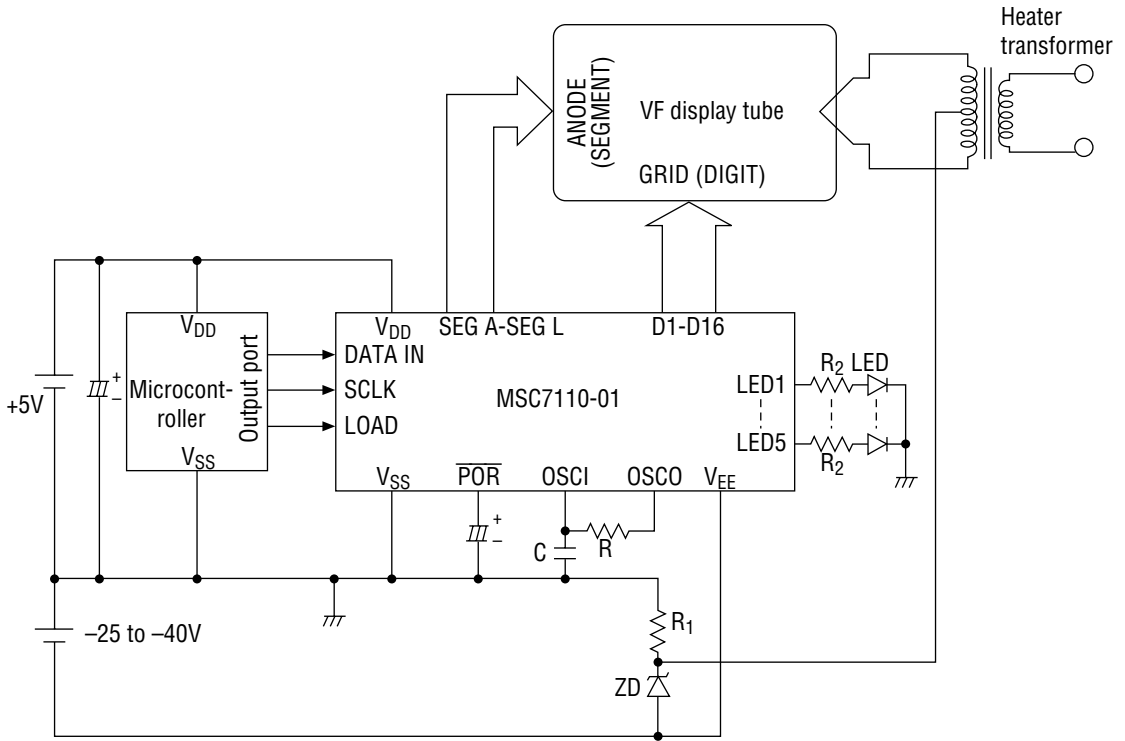
D.R				Control	D.R				Control	D.R				Control	D.R				Control
b ₃	b ₂	b ₁	b ₀	digit	b ₃	b ₂	b ₁	b ₀	digit	b ₃	b ₂	b ₁	b ₀	digit	b ₃	b ₂	b ₁	b ₀	digit
0	0	0	0	^{*2} D1-D16	0	1	0	0	D1-D4	1	0	0	0	D1-D8	1	1	0	0	D1-D12
0	0	0	1	D1-D1	0	1	0	1	D1-D5	1	0	0	1	D1-D9	1	1	0	1	^{*2} D1-D13
0	0	1	0	D1-D2	0	1	1	0	D1-D6	1	0	1	0	D1-D10	1	1	1	0	^{*2} D1-D14
0	0	1	1	D1-D3	0	1	1	1	D1-D7	1	0	1	1	D1-D11	1	1	1	1	^{*2} D1-D15

*1 1 to 12 digits in the case of the MSC7112-01

*2 Ignored in the case of the MSC7112-01

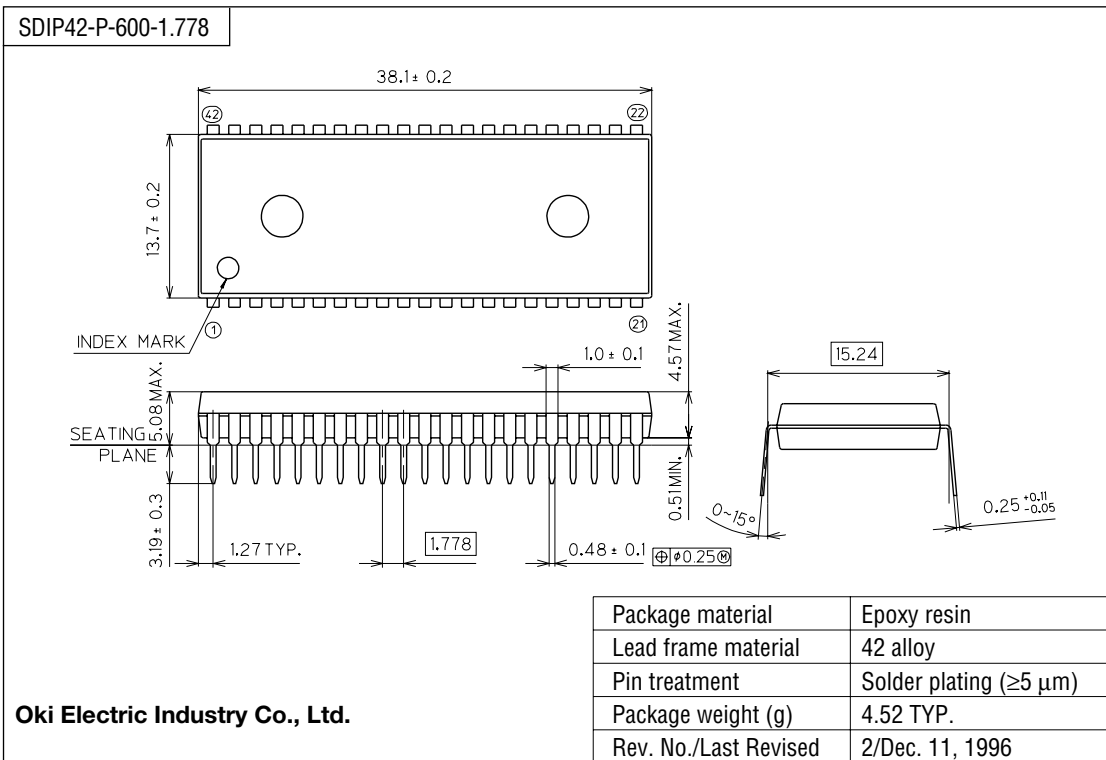
APPLICATION CIRCUIT

MSC7110-01



PACKAGE DIMENSIONS

(Unit : mm)

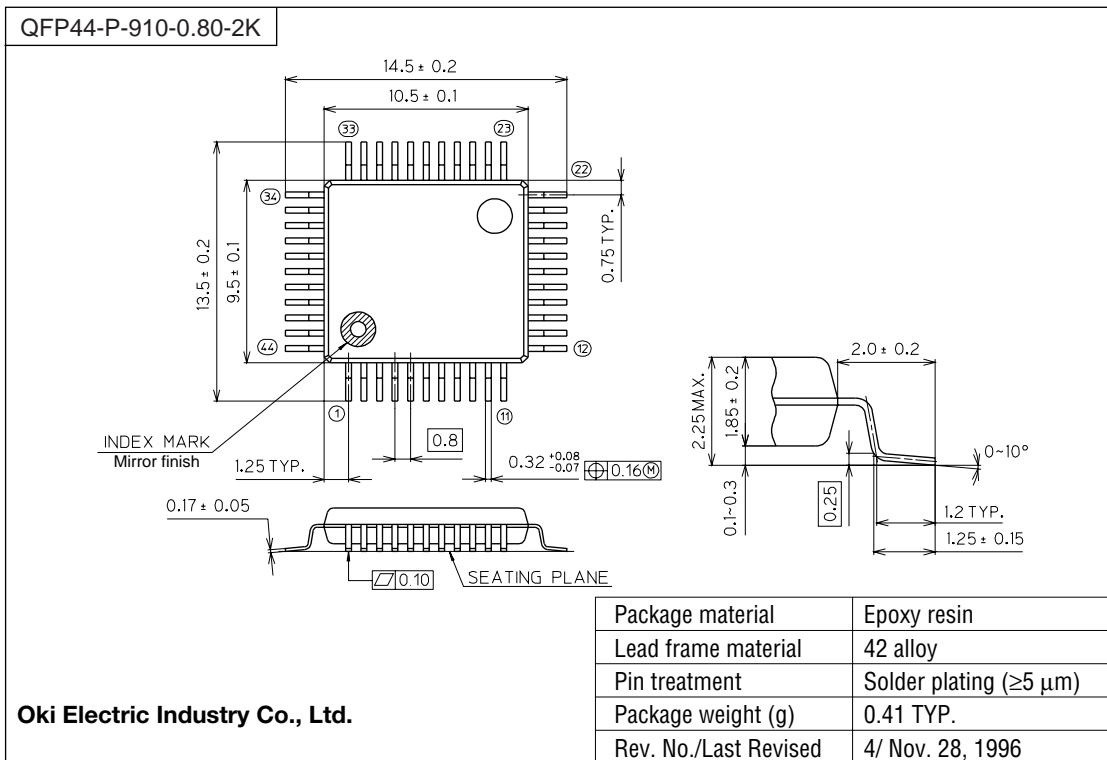


Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)



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