Features

- JEDEC Standard PC-133 SDRAM DIMM
- Low Latency PC-133 Modules (3:2:2) @ 133 MHz
  - CAS Latency = 3
  - RAS to CAS Delay = 2
  - Precharge Delay = 2
- Fast 4.6 ns Clock Access Time
- Overclock Existing PC Systems to 133 MHz
- Ideal for Low Cost 133 MHz Bus Speed Systems
- Supports CAS Latency = 1, 2, 3
- On-board Serial Presence Detect (SPD)
- Unbuffered 168-pin DIMM
- 4K Refresh / 64 ms
- Single 3.3V ± 0.3V Power Supply
- Available on-line at http://www.pc133memory.com

Description

The Enhanced Memory Systems 32MB, 64MB and 128MB low latency PC-133 HSDRAM DIMMs are the fastest unbuffered SDRAM DIMMs available. Low latency (3:2:2) improves performance in high-end desktop publishing and graphics applications, particularly with UMA system architectures. The fast 4.6 ns clock access time allows unbuffered DIMM operation at 133 MHz for lower memory latency, and lower costs than registered DIMMs.

The 32MB module (SM3208DT-7.5) is organized as 4Mx64, the 64MB module (SM6408DT-7.5) is organized as 8Mx64, and the 128MB module (SM12808DT-7.5) is organized as 16Mx64. The 128MB ECC module (SM12809DT-7.5) is organized as 16Mx72. Each module contains a serial presence EEPROM programmed by Enhanced Memory Systems, which contains information on the module type, module organization, component speed, and other attributes relevant to the system controller.

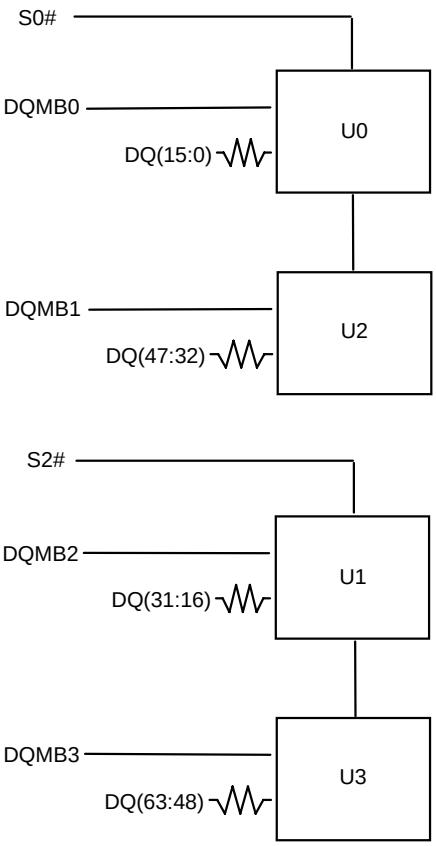
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	DNU	86	DQ32	128	CKE0
3	DQ1	45	S2#	87	DQ33	129	S3#
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	Vdd	48	DNU	90	Vdd	132	RFU
7	DQ4	49	Vdd	91	DQ36	133	Vdd
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vdd	101	DQ45	143	Vdd
18	Vdd	60	DQ20	102	Vdd	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	CKE1	105	CB4	147	NC
22	CB1	64	Vss	106	CB5	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vdd	68	Vss	110	Vdd	152	Vss
27	WE#	69	DQ24	111	CAS#	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0#	72	DQ27	114	S1#	156	DQ59
31	DNU	73	Vdd	115	RAS#	157	Vdd
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	CK2	121	A9	163	CK3
38	A10/AP	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	Vdd	82	SDA	124	Vdd	166	SA1
41	Vdd	83	SCL	125	CK1	167	SA2
42	CK0	84	Vdd	126	RFU	168	Vdd

Enhanced Memory Systems Inc., 1850 Ramtron Dr., Colo Spgs, CO 80921
PHONE: (800) 545-DRAM; FAX: (719) 488-9095; http://www.edram.com

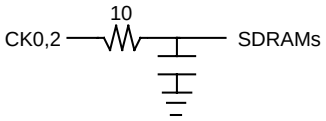
Pin Descriptions

Symbol	Type	Function
CK0,1,2,3	Input	Clocks: All SDRAM input signals are sampled on the positive edge of CK.
CKE0,1	Input	Clock Enables: CKE activate (high) or deactivate (low) the CK signals. Deactivating the clock initiates the Power-Down and Self-Refresh operations (all banks idle), or Clock Suspend operation. CKE is synchronous until the device enters Power-Down and Self-Refresh modes where it is asynchronous until the mode is exited.
S0,1,2,3#	Input	Chip Select: S# enables (low) or disables (high) the command decoder. When the command decoder is disabled, new commands are ignored but previous operations continue.
RAS#, CAS#, WE#	Input	Command Inputs: Sampled on the rising edge of CK, these inputs define the command to be executed.
BA1, BA0	Input	Bank Addresses: These inputs define to which of the 4 banks a given command is being applied.
A0-A11	Input	Address Inputs: A0-A11 define the row address during the Bank Activate command. A0-A8 define the column address during Read and Write commands. A10/AP invokes the Auto-precharge operation. During manual Precharge commands, A10/AP low specifies a single bank precharge while A10/AP high precharges all banks. The address inputs are also used to program the Mode Register.
DQ0-DQ63	Input/ Output	Data I/O: Data bus inputs and outputs. For Write cycles, input data is applied to these pins and must be set-up and held relative to the rising edge of clock. For Read cycles, the device drives output data on these pins after the CAS latency is satisfied.
DQMB0-7	Input	Data I/O Mask Inputs: DQMB0-7 inputs mask write data (zero latency) and acts as a synchronous output enable (2-cycle latency) for read data.
CB0-7	Input/ Output	ECC Check Bits
V_{DD}	Supply	Power Supply: +3.3 V
V_{SS}	Supply	Ground
SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bi-directional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence detect data transfer to and from the module
SA0-2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence detect device.
WP	Input	Serial Presence Detect Write Protect: Active high inhibits writes to the SPD EEPROM. WP must be driven low for normal read/write operations.
RFU	-	Reserved for Future Use: These pins should be left unconnected.
DNU	-	Do not use.
NC	-	No connect - open pin.

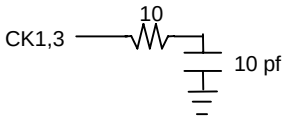
32MB DIMM Functional Block Diagram – SM3208DT-7.5

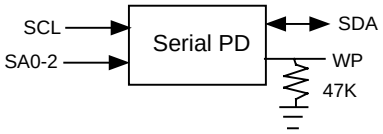


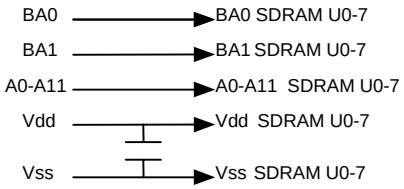
Clock Wiring	
CK0	2 SDRAM+15 pf
CK1	Termination
CK2	2 SDRAM+15 pf
CK3	Termination

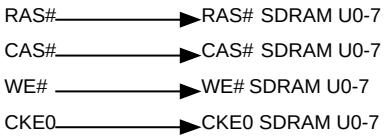


Clock Termination



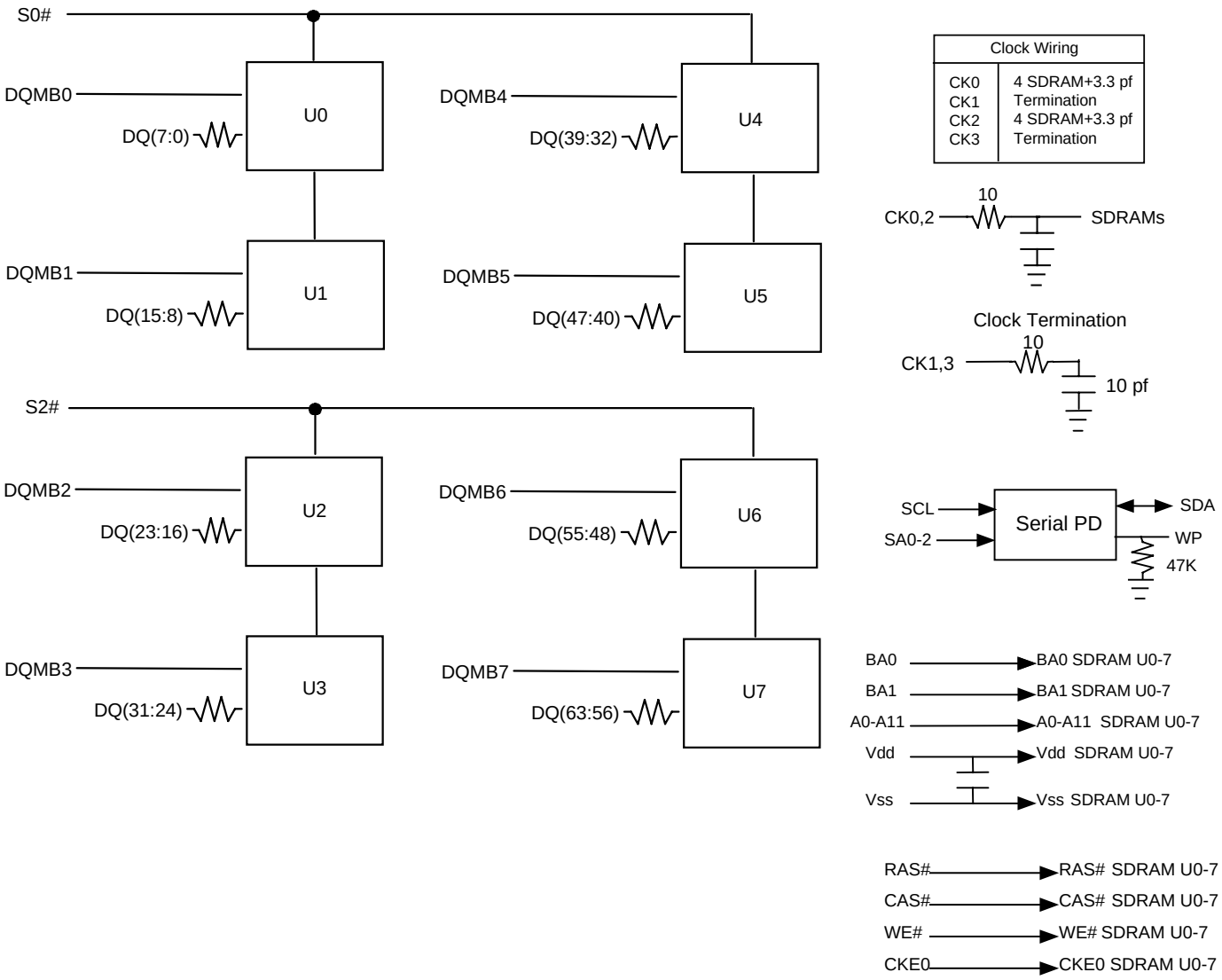






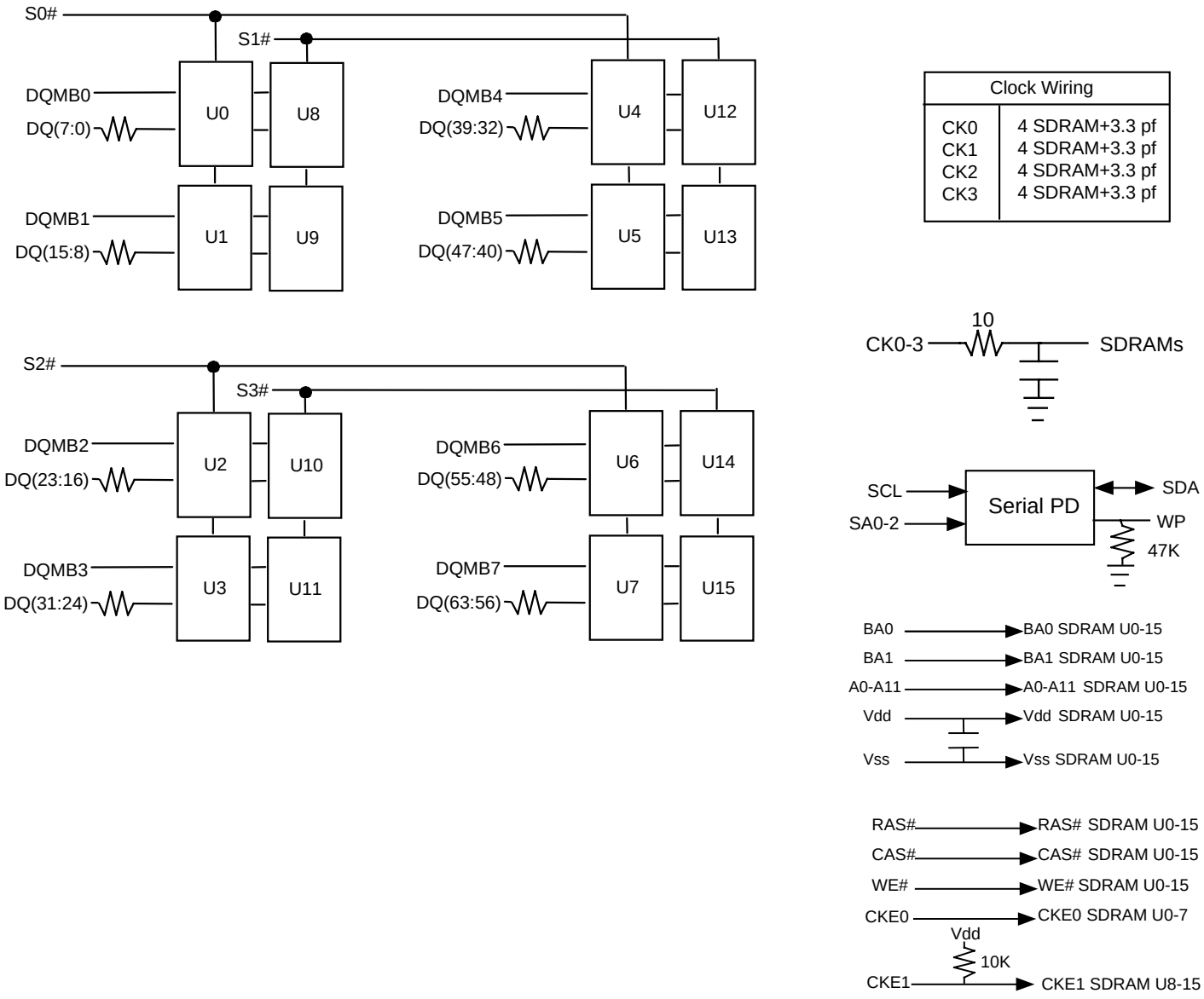
Note: All DQ resistor values are 10 ohms
All CK resistor values are 10 ohms
U0-U7 are SM3603T-7.5

64MB DIMM Functional Block Diagram – SM6408DT-7.5



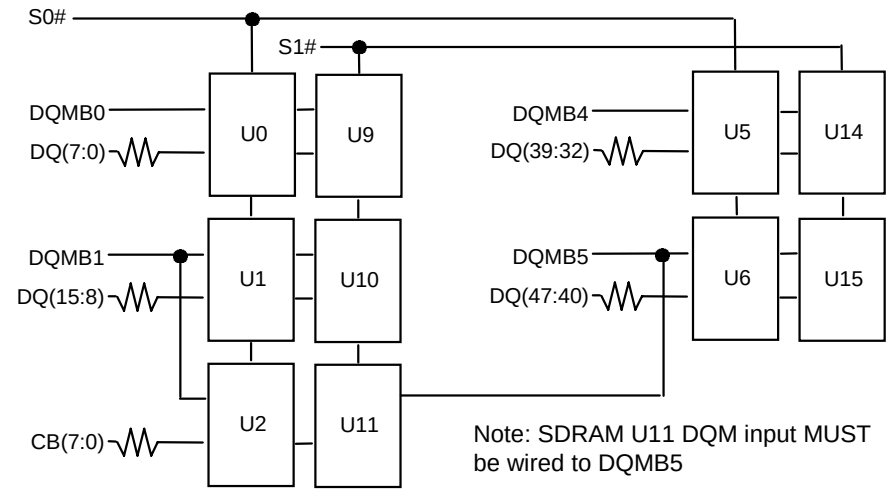
Note: All DQ resistor values are 10 ohms
All CK resistor values are 10 ohms
U0-U7 are SM3603T-7.5

128MB DIMM Functional Block Diagram – SM12808DT-7.5

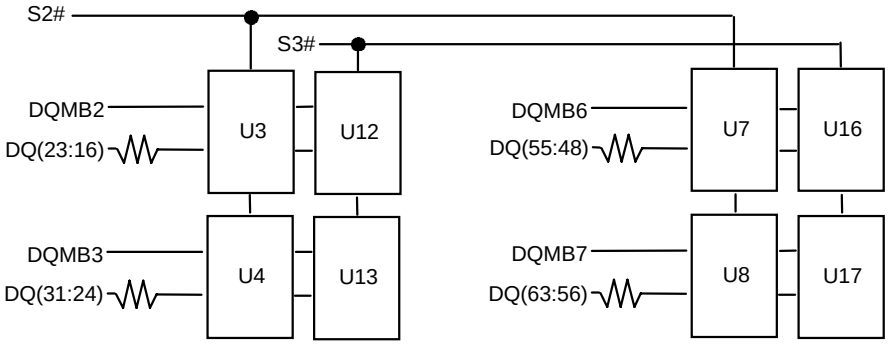


Note: All DQ resistor values are 10 ohms
All CK resistor values are 10 ohms
U0-U15 are SM3603T-7.5

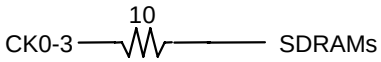
128MB ECC DIMM Functional Block Diagram – SM12809DT-7.5

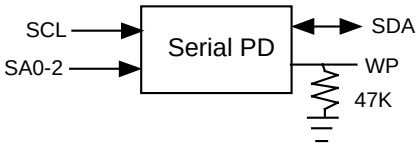


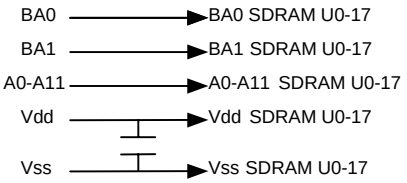
Note: SDRAM U11 DQM input MUST be wired to DQMB5

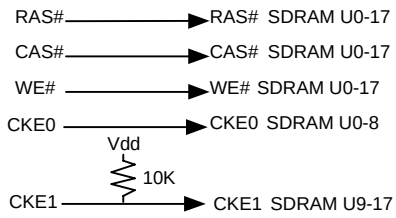


Clock Wiring	
CK0	5 SDRAM
CK1	5 SDRAM
CK2	4 SDRAM+3.3 pf
CK3	4 SDRAM+3.3 pf









Note: All DQ resistor values are 10 ohms
All CK resistor values are 10 ohms
U0-U15 are SM3603T-7.5

Electrical Characteristics

Absolute Maximum Ratings

Description	Symbol	Value
Power Supply Voltage	V_{DD}	-1V to +4.6V
Voltage on any Pin with Respect to Ground	V_{IN}, V_{OUT}	-0.5V to +4.6V
Operating Temperature (ambient)	T_A	0°C to +70°C
Storage Temperature	T_{stg}	-55°C to +125°C
Power Dissipation	P_D	TBD
DC Output Current (I/O pins)	I_{OUT}	50mA

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these, or any other conditions above those listed in the operational section of the specification, is not implied. Exposure to conditions at absolute maximum ratings for extended periods may affect device reliability.

DC Operating Conditions (T_A = 0°C to 70°C)

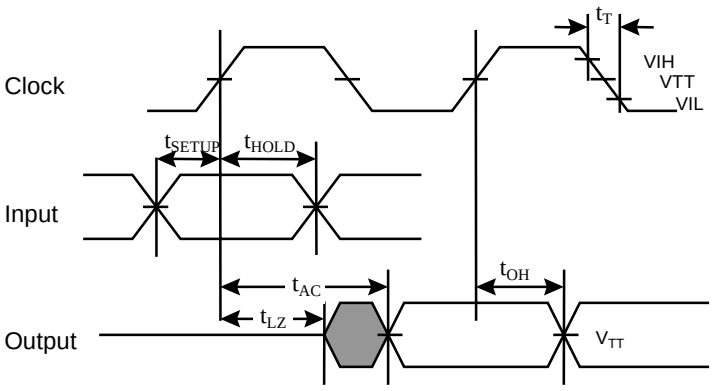
Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{DD}	Supply Voltage	3.0	3.3	3.6	V	
V_{IH}	Input High Voltage	2.0	3.3	V_{DD} + 0.3	V	
V_{IL}	Input Low Voltage	-0.3	0.0	0.8	V	
$I_{I(L)}$	Input Leakage Current	-	-	±1	µA	
$I_{O(L)}$	Output Leakage Current	-	-	±1	µA	
V_{OH}	Output High Voltage (I_{OUT} = -4mA)	2.4	-	V_{DD}	V	
V_{OL}	Output Low Voltage (I_{OUT} = +4mA)	0.0	-	0.4	V	

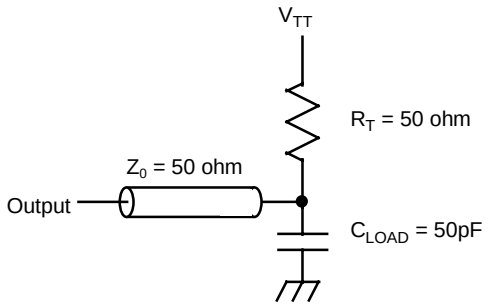
Capacitance (T_A = 25°C, f = 1MHz, VDD = 3.3V ±0.3V, not 100% tested)

Symbol	Parameter	32MB	64MB	128MB		Units
		non-ECC	non-ECC	non-ECC	ECC	
C_{In1}	Input Capacitance (BA1, BA0, A0-11, RAS, CAS)	25	38	65	71	pF
C_{In2}	Input Capacitance (S0 - S3)	14	21	21	24	pF
C_{In3}	Input Capacitance (CK0 - CK3)	26	26	26	26	pF
C_{In4}	Input Capacitance (CKE0, CKE1)	25	38	38	42	pF
C_{In5}	Input Capacitance (DQMB0-7)	12	12	14	14	pF
C_{In6}	Input Capacitance (SCL, SA0-2)	12	12	12	12	pF
$C_{I/O1}$	I/O Capacitance (SDA)	12	12	12	12	pF
$C_{I/O2}$	I/O Capacitance (DQ0-63, CB0-7)	8.5	8.5	13	13	pF

AC Characteristics (T_A = 0°C to 70°C)

1. An initial pause of 200µs is required after power-up, then a Precharge All Banks command must be given followed by a minimum of eight Auto (CBR) Refresh cycles before the Mode Register Set operation can begin.
2. AC timing tests have V_{IL} = 0.8V and V_{IH} = 2.0V with the timing referenced to the V_{TT} = 1.4V crossover point.





AC Output Load Circuit

3. The transition time is measured between V_{IH} and V_{IL} (or between V_{IH} and V_{IL}).
4. AC measurements assume t_T = 1ns.
5. In addition to meeting the transition rate specification, the clock and CKE must transition V_{IH} and V_{IL} (or between V_{IH} and V_{IL}) in a monotonic manner.

AC Operating Conditions (T_A = 0°C to 70°C)

Symbol	Parameter	-7.5		Units	Notes
		Min	Max		
Clock and Clock Enable Parameters					
t_{CK3}	Clock Cycle Time, CL = 3	7.5		ns	
t_{CK2}	Clock Cycle Time, CL = 2	10		ns	
t_{CK1}	Clock Cycle Time, CL = 1	20		ns	
t_{CKH3}, t_{CKL3}	Clock High & Low Times, CL=3	2.5	-	ns	1
t_{CKH2}, t_{CKL2}	Clock High & Low Times, CL=2	3.5	-	ns	1
t_{CKH1}, t_{CKL1}	Clock High & Low Times, CL=1	4.5	-	ns	1
t_{CKES}	Clock Enable Set-Up Time	1.5	-	ns	
t_{CKEH}	Clock Enable Hold Time	0.8	-	ns	
t_{CKSP}	CKE Set-Up Time (Power down mode)	1.5	-	ns	
t_T	Transition Time (Rise and Fall)	-	4	ns	
Common Parameters					
t_{CS}	Command and Address Set-Up Time	1.5	-	ns	
t_{CH}	Command and Address Hold Time	0.8	-	ns	
t_{RCD}	RAS to CAS Delay Time	15	-	ns	
t_{RC}	Bank Cycle Time	52.5	120K	ns	
t_{RAS}	Bank Active Time	37.5	120K	ns	
t_{RP}	Precharge Time	15	-	ns	
t_{RRD}	Bank to Bank Delay Time (Alt. Bank)	15	-	ns	
t_{CCD}	CAS to CAS Delay Time (Same Bank)	7.5	-	ns	
t_{MRD}	Mode Register Set to Active Delay	2	-	CLK	

Notes:

1. Assumes clock rise and fall times are equal to 1ns. If rise or fall time exceeds 1ns, other AC timing parameters must be compensated by an additional $[(t_{rise}+t_{fall})/2\text{-}1]$ ns.

Symbol	Parameter	-7.5		Units	Notes
		Min	Max		
Read and Write Parameters					
t_{AC3}	Clock Access Time, CL = 3	-	4.6	ns	1,2
t_{AC2}	Clock Access Time, CL = 2	-	6.0	ns	1,2
t_{AC1}	Clock Access Time, CL = 1	-	15.0	ns	1,2
t_{OH3}	Data Output Hold Time (CL=3)	2.7	-	ns	
t_{OH2}	Data Output Hold Time (CL=2)	3.0	-	ns	
t_{OH1}	Data Output Hold Time (CL=1)	3.5	-	ns	
t_{LZ}	Data Output to Low-Z Time	1	-	ns	
t_{HZ2}	Data Output to High-Z Time (CL=2, 3)	-	4.6	ns	3
t_{HZ1}	Data Output to High-Z Time (CL=1)	-	7.0	ns	3
t_{DQZ}	DQM Data Output Disable Time	2	-	CLK	
t_{DS}	Data Input Set-Up Time	1.5	-	ns	
t_{DH}	Data Input Hold Time	0.8	-	ns	
t_{DPL}	Data Input to Precharge	15	-	ns	
t_{DAL}	Data Input to ACTV/Refresh	30	-	ns	4
t_{DQW}	Data Write Mask Latency	0	-	CLK	
Refresh Parameters					
t_{REF}	Refresh Period	-	64	ms	5, 6
t_{SREX}	Self Refresh Exit Time	2CLK+t_{RC}	-	ns	7

Notes:

1. Access time is measured at 1.4V (LVTTL) at max clock rate for the CAS latency specified. See AC Test Load.
2. Access time is based on a clock rise time of 1ns. If clock rise time is longer than 1ns, then (trise/2-0.5) ns must be added to the access time.
3. Referenced to the time at which the output achieves an open circuit condition.
4. tDAL is equal to tDPL + tRP.
5. 4096 cycles.
6. Any time that the refresh period has been exceeded, a minimum of two Auto-Refresh (CBR) commands must be given to “wake up” the device.
7. Self-Refresh exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self-Refresh Exit is not completed until tRC is satisfied once the Self-Refresh Exit command is registered.

Serial Presence Detect (SPD) for PC-133 DIMMs

Byte	Description		32MB	64MB	128MB	32MB	64MB	128MB
						** Hex Code **		
0	Number of bytes written into EEPROM		128	128	128	80	80	80
1	Total number of SPD bytes		256	256	256	08	08	08
2	Memory Type		SDRAM	SDRAM	SDRAM	04	04	04
3	Number of Row Addresses		12	12	12	0C	0C	0C
4	Number of Column Addresses		8	9	9	08	09	09
5	Number of Module Banks		1	1	2	01	01	02
6	Module Data Width		x64	x64	x64 x72	40	40	40 48
7	Module Data Width (cont'd)		0	0	0	00	00	00
8	Voltage Interface Levels		LVTTL	LVTTL	LVTTL	01	01	01
9	Cycle Time at max CAS Latency		7.5 ns	7.5 ns	7.5 ns	75	75	75
10	SDRAM Clock Access Time		5.0 ns	4.6 ns	4.6 ns	50	46	46
11	DIMM config (non-parity, parity, ECC)		--- Non-parity --- --- ECC ---			00	00	00 02
12	Refresh Rate and Type		--- 15.625us / Self ---			80	80	80
13	Primary SDRAM Width		x16	x8	x8	10	08	08
14	Error Checking Data Width	x64 x72	N/A	N/A	N/A x8	00	00	00 08
15	Min. CAS-to-CAS Delay (tCCD)		1 clk	1 clk	1 clk	01	01	01
16	Burst Lengths Supported		--- 1,2,4,8,Full Pg ---			8F	8F	8F
17	Number of Banks on SDRAM Device		4	4	4	04	04	04
18	CAS Latencies Supported		1,2,3	1,2,3	1,2,3	07	07	07
19	CS Latency		0	0	0	01	01	01
20	Write Latency		0	0	0	01	01	01
21	SDRAM Module Attributes		--- Unbuffered ---			00	00	00
22	SDRAM Device Attributes		+/-10% Vdd, Precharge All, Wr-1/RdBrst			0E	0E	0E
23	Min. Clock Cycle Time at CL=2		10 ns	10 ns	10 ns	A0	A0	A0
24	Clock Access Time at CL=2 (tAC2)		6 ns	6 ns	6 ns	60	60	60
25	Min. Clock Cycle Time at CL=1		20	20	20	50	50	50
26	Clock Access Time at CL=1 (tAC1)		15	15	15	3C	3C	3C
27	Min. Row Precharge Time (tRP)		15 ns	15 ns	15 ns	0F	0F	0F
28	Min. Row-to-Row Delay (tRRD)		15 ns	15 ns	15 ns	0F	0F	0F
29	Min. RAS-to-CAS Delay (tRCD)		15 ns	15 ns	15 ns	0F	0F	0F
30	Min. RAS Pulse Width (tRAS)		37.5 ns	37.5 ns	37.5 ns	26	26	26
31	Density of each bank on module		32MB	64MB	64MB	08	10	10
32	Cmd/Addr input set-up time		1.5 ns			15	15	15
33	Cmd/Addr input hold time		0.8 ns			08	08	08
34	Data input set-up time		1.5 ns			15	15	15
35	Data input hold time		0.8 ns			08	08	08
36-61	Superset Information		-	-	-	00	00	00
62	SPD Rev.		1.2			12	12	12
63	Checksum for bytes 0-62	non-ECC ECC	-	-	-	15	0C	0D 1F
64-71	JEDEC ID code		Enhanced Memory Systems			7F32FFFFFFFFFFFF		
72	Manufacturing Location		-	-	-	xxxx	xxxx	xxxx
73-90	Manufacturer's Part #		SM3208DT	SM6408DT	SM12808DT	xxxx	xxxx	xxxx
91,92	PCB Rev. Code		-			rrrr	rrrr	rrrr
93,94	Manufacturing Date		yyww code			yyww	yyww	yyww
95-98	Assembly Serial #		serial number			ssss	ssss	ssss
99-125	Manufacturer's Specific Data		open			00	00	00
126	Intel specification frequency		133MHz			64	64	64
127	Intel specification CL and clock support		-	-	-	AF	AF	FF

Revision Log

Revision	Date	Summary of Changes
1.4	5/2/00	Added CAS 1 data, and this revision log.

Ordering Information

These PC-133 HSDRAM DIMMs may be purchased on-line at http://www.pc133memory.com, which is an e-commerce function of Enhanced Memory Systems Inc., or call 1-800-568-1868.

Part Number	Capacity	I/O Width	I/O Type	Package	Power Supply	Maximum Operating Frequency (MHz)
SM3208DT-7.5	32 MB	x64	LVTTL	168-pin DIMM	3.3V	133
SM6408DT-7.5	64 MB	x64	LVTTL	168-pin DIMM	3.3V	133
SM12808DT-7.5	128 MB	x64	LVTTL	168-pin DIMM	3.3V	133
SM12809DT-7.5	128 MB	x72	LVTTL	168-pin DIMM	3.3V	133

Note: Enhanced Memory Systems Low Latency PC-133 HSDRAM DIMMs are labeled per the Intel PC SDRAM DIMM Naming Convention. This convention requires identification of the bus speed, latency, clock access time, and SPD revision code. The code for these DIMM modules is PC133-322-46100.

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