4-Bit Bistable Latches

DESCRIPTION

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

The LS75 feature complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and is available in various 16-pin packages. For higher component density applications, the 'LS77 4-bit latch is available in 14-pin flat packages.

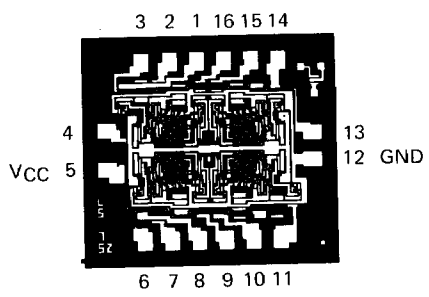
These circuits are completely compatible with all popular TTL or DTL families. All inputs are diode-clamped to minimize transmission-line effects and simplify system design.

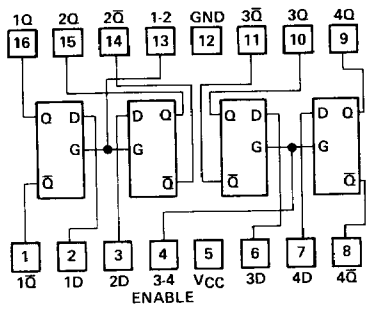
FUNCTION TABLE
(Each Latch)

INPUTS		OUTPUTS	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = high level, L = low level, X = Irrelevent
Q_0 = the level of Q before the high-to-low transition of G

LS75

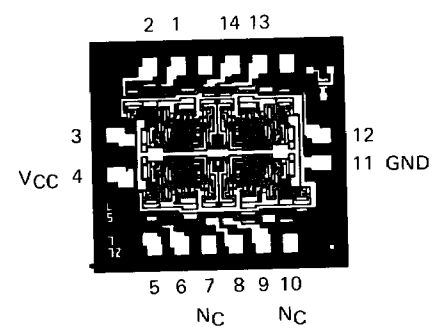


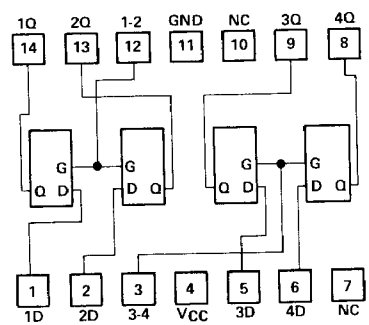


logic: see function table

Die Size .065 x .059

LS77

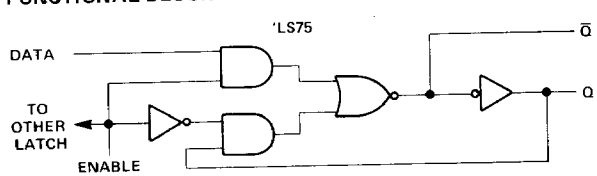


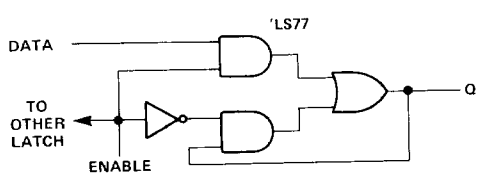


logic: see function table

Die Size .065 x .059

FUNCTIONAL BLOCK DIAGRAMS (each latch)





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Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Width of enabling pulse, t_w	20			20			ns
Setup time, t_{su}	20			20			ns
Hold time, t_h	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS†		9LS/54LS			9LS/74LS			Unit
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC}=MIN, I_I=-8mA				-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC}=MIN, V_{IH}=2 V, V_{IL}=V_{IL} max, I_{OH}=-440 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max	I_{OL}=4 mA		0.25	0.4		0.25	0.4	V
			I_{OL}=8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=MAX, V_I=7 V	D input			0.1			0.1	mA
			G input			0.4			0.4	
I_{IH}	High-level input current	V_{CC}=MAX, V_I=2.7 V	D input			20			20	μA
			G input			80			80	
I_{IL}	Low-level input current	V_{CC}=MAX, V_I=0.4 V	D input			-0.4			-0.4	mA
			G input			-1.6			-1.6	
I_{OS}	Short-circuit output current§	V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}	Supply current	V_{CC}=MAX, See Note 1	'LS75		6.3	12		6.3	12	mA
			'LS77		6.9	13				

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 1: I_{CC} is tested with all input grounded and all outputs open.

Switching Characteristics V_{CC} = 5.0V Over Recommended Free-Air Temperature Range.

Parameter	From (Input)	To (Output)	9LS/54LS75									Unit
			−55°C			+25°C			+125°C			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Condition: C_L = 15pF, R_L = 2.0k (See Fig. A, page 2-174 and Fig. 1, page 2-32)												
t_{PLH}	D	Q		18	31		15	27		18	31	ns
t_{PLH}				12	16		9	17		12	16	
t_{PHL}	D	$\overline{Q}$		15	19		12	20		15	19	ns
t_{PHL}				10	14		7	15		10	14	
t_{PLH}	G	Q		18	22		15	27		18	22	ns
t_{PHL}				17	21		14	25		17	21	
t_{PLH}	G	$\overline{Q}$		19	23		16	30		19	23	ns
t_{PHL}				10	14		7	15		10	14	
Test Condition: C_L = 50pF, R_L = 2.0k (See Fig. A, page 2-174 and Fig. 1, page 2-32)												
t_{PLH}	D	Q		22	37		19	33		22	37	ns
t_{PHL}				16	22		13	18		16	22	
t_{PLH}	D	$\overline{Q}$		19	25		16	21		19	25	ns
t_{PHL}				14	20		11	16		14	20	
t_{PLH}	G	Q		22	28		19	24		22	28	ns
t_{PHL}				21	27		18	23		21	27	
t_{PLH}	G	$\overline{Q}$		23	29		20	25		23	29	ns
t_{PHL}				14	20		11	16		14	20	

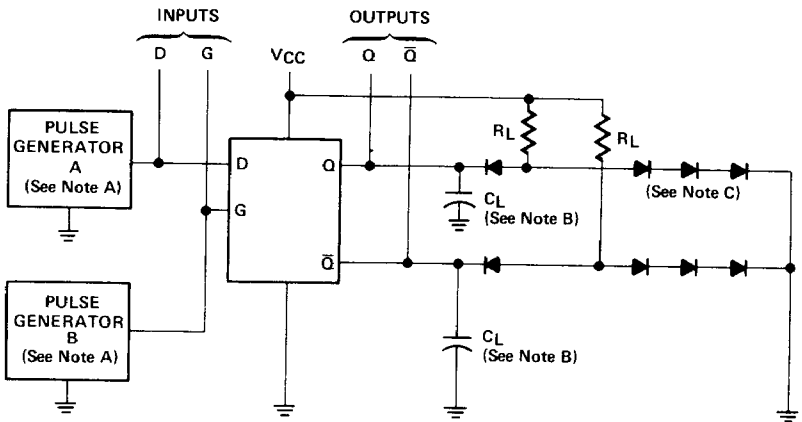
Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS devices only.

Switching Characteristics V_{CC} = 5.0V Over Recommended Free-Air Temperature Range.

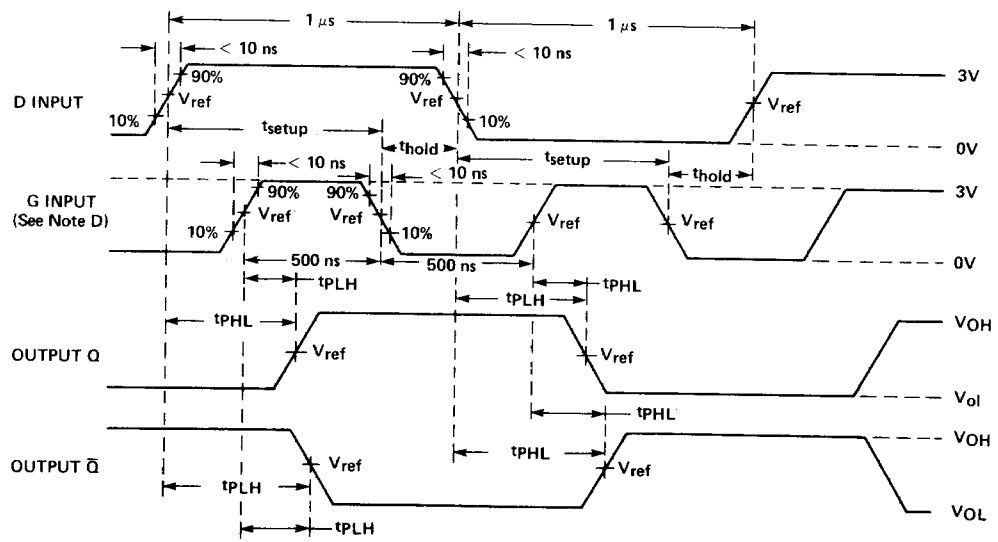
Parameter	From (Input)	To (Output)	9LS/54LS77									Unit
			−55°C			+25°C			+125°C			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 15pF, R_L = 2.0k (See Fig. A, page 2-174 and Fig. 1 page 2-32)												
t_{PLH}	D	Q		15	24		11	19		14	23	ns
t_{PHL}				12	20		9	17		12	20	
t_{PLH}	G	Q		13	21		10	18		13	21	ns
t_{PHL}				13	21		10	18		13	21	
Test Conditions: C_L = 50pF, R_L = 2.0k (See Fig. A, page 2-174 and Fig. 1, page 2-32)												
t_{PLH}	D	Q		17	28		15	24		18	28	ns
t_{PHL}				16	26		13	22		17	26	
t_{PLH}	G	Q		17	27		14	23		18	27	ns
t_{PHL}				17	27		14	23		18	27	

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS devices only.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1.

NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$; for pulse generator A, PRR≤500 kHz; for pulse generator B, PRR≤1 MHz. Positions of D and G input pulses are varied with respect to each other to verify setup times.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064.

D. When measuring propagation delay times from the D input, the corresponding G input must be held high.

E. $V_{ref} = 1.3$ V.

† Complementary Q outputs are on the 'LS75 only.