# Preliminary 8Mb (256Kx36 & 512Kx18) and 4Mb (128Kx36 & 256Kx18) SRAM

## Features

- 256K x 36 or 512K x 18 organizations
- 128K x 36 or 256K x 18 organizations
- 0.25 Micron CMOS technology
- Synchronous Register-Latch Mode of Operation with Self-Timed Late Write
- Single Differential HSTL Clock
- +3.3V Power Supply, Ground, 2.0Volt max $V_{DDQ,}$ and 0.85Volt $V_{REF}$
- HSTL Input and Output levels,
- Registered Addresses, Write Enables, Synchronous Select, and Data Ins.
- Latched Outputs
- Common I/O
- Asynchronous Output Enable and Power Down Inputs
- Boundary Scan using limited set of JTAG 1149.1 functions
- Byte Write Capability & Global Write Enable
- 7 x 17 Bump Ball Grid Array Package with SRAM JEDEC Standard Pinout and Boundary SCAN Order
- Programmable Impedance Output Drivers

## Description

The 4 and 8Mb SRAMs—IBM0436A4ACLAB, IBM0436A8ACLAB, IBM0418A4ACLAB, and IBM0418A8ACLAB—are Synchronous Register-Latch Mode, high-performance CMOS Static Random Access Memories that are versatile, have wide I/O, and can achieve 3.8 ns cycle times. Differential K clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of the K clock, all Addresses, Write-Enables, Sync Select, and Data Ins are registered internally. Data Outs are updated from output registers off the falling edge of the K clock. An internal Write buffer allows write data to follow one cycle after addresses and controls. The chip is operated with a single +3.3V power supply and is compatible with HSTL I/O interfaces.

## x36 BGA Pinout (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| **A** | $V_{DDQ}$ | SA | SA | NC | SA | SA | $V_{DDQ}$ |
| **B** | NC | NC | SA | NC | SA | NC,SA(8Mb) | NC |
| **C** | NC | SA | SA | $V_{DD}$ | SA | SA | NC |
| **D** | DQ19 | DQ18 | $V_{SS}$ | ZQ | $V_{SS}$ | DQ9 | DQ10 |
| **E** | DQ22 | DQ20 | $V_{SS}$ | $\overline{SS}$ | $V_{SS}$ | DQ11 | DQb13 |
| **F** | $V_{DDQ}$ | DQ21 | $V_{SS}$ | $\overline{G}$ | $V_{SS}$ | DQ12 | $V_{DDQ}$ |
| **G** | DQ24 | DQ23 | $\overline{SBWc}$ | NC | $\overline{SBWb}$ | DQ14 | DQb15 |
| **H** | DQ25 | DQ26 | $V_{SS}$ | NC | $V_{SS}$ | DQ17 | DQb16 |
| **J** | $V_{DDQ}$ | $V_{DD}$ | $V_{REF}$ | $V_{DD}$ | $V_{REF}$ | $V_{DD}$ | $V_{DDQ}$ |
| **K** | DQ34 | DQ35 | $V_{SS}$ | K | $V_{SS}$ | DQ8 | DQ7 |
| **L** | DQ33 | DQ32 | $\overline{SBWd}$ | $\overline{K}$ | $\overline{SBWa}$ | DQ5 | DQ6 |
| **M** | $V_{DDQ}$ | DQ30 | $V_{SS}$ | $\overline{SW}$ | $V_{SS}$ | DQ3 | $V_{DDQ}$ |
| **N** | DQ31 | DQ29 | $V_{SS}$ | SA | $V_{SS}$ | DQ2 | DQ4 |
| **P** | DQ28 | DQ27 | $V_{SS}$ | SA | $V_{SS}$ | DQ0 | DQ1 |
| **R** | NC | SA | M1* | $V_{DD}$ | M2* | SA | NC |
| **T** | NC | NC | SA | SA | SA | NC | ZZ |
| **U** | $V_{DDQ}$ | TMS | TDI | TCK | TDO | NC | $V_{DDQ}$ |

**Note:** * M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to $V_{DD}$ and $V_{SS}$ respectively.

## x18 BGA Pinout (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| **A** | $V_{DDQ}$ | SA | SA | NC | SA | SA | $V_{DDQ}$ |
| **B** | NC | NC | SA | NC | SA | NC,SA(8Mb) | NC |
| **C** | NC | SA | SA | $V_{DD}$ | SA | SA | NC |
| **D** | DQ14 | NC | $V_{SS}$ | ZQ | $V_{SS}$ | DQ0 | NC |
| **E** | NC | DQ15 | $V_{SS}$ | $\overline{SS}$ | $V_{SS}$ | NC | DQ1 |
| **F** | $V_{DDQ}$ | NC | $V_{SS}$ | $\overline{G}$ | $V_{SS}$ | DQ2 | $V_{DDQ}$ |
| **G** | NC | DQ16 | $\overline{SBWb}$ | NC | NC | NC | DQ3 |
| **H** | DQ17 | NC | $V_{SS}$ | NC | $V_{SS}$ | DQ4 | NC |
| **J** | $V_{DDQ}$ | $V_{DD}$ | $V_{REF}$ | $V_{DD}$ | $V_{REF}$ | $V_{DD}$ | $V_{DDQ}$ |
| **K** | NC | DQ13 | $V_{SS}$ | K | $V_{SS}$ | NC | DQ8 |
| **L** | DQ12 | NC | NC | $\overline{K}$ | $\overline{SBWa}$ | DQ7 | NC |
| **M** | $V_{DDQ}$ | DQ10 | $V_{SS}$ | $\overline{SW}$ | $V_{SS}$ | NC | $V_{DDQ}$ |
| **N** | DQ11 | NC | $V_{SS}$ | SA | $V_{SS}$ | DQ6 | NC |
| **P** | NC | DQ9 | $V_{SS}$ | SA | $V_{SS}$ | NC | DQ5 |
| **R** | NC | SA | M1 | $V_{DD}$ | M2 | SA | NC |
| **T** | NC | SA | SA | NC | SA | SA | ZZ |
| **U** | $V_{DDQ}$ | TMS | TDI | TCK | TDO | NC | $V_{DDQ}$ |

**Note:** * M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to $V_{DD}$ and $V_{SS}$ respectively.

## Pin Description

| | | | |
|---|---|---|---|
| SA0-SA18 | Address Input<br>SA0-SA18 for 512Kx18<br>SA0-SA17 for 256Kx36<br>SA0-SA17 for 256Kx18<br>SA0-SA16 for 128Kx36 | $\overline{G}$ | Asynchronous Output Enable |
| DQ0-DQ35 | Data I/O<br>DQ0-DQ17 for 512Kx18<br>DQ0-DQ35 for 256Kx36 | $\overline{SS}$ | Synchronous Select |
| K, $\overline{K}$ | Differential Input Register Clocks | M1, M2 | Clock Mode Inputs- Selects Single or Dual Clock Operation. |
| $\overline{SW}$ | Write Enable, Global | $V_{REF}$(2) | HSTL Input Reference Voltage |
| $\overline{SBWa}$ | Write Enable, Byte a (DQ0-DQ8) | $V_{DD}$ | Power Supply (+3.3V) |
| $\overline{SBWb}$ | Write Enable, Byte b (DQ9-DQ17) | $V_{SS}$ | Ground |
| $\overline{SBWc}$ | Write Enable, Byte c (DQ18-DQ26) | $V_{DDQ}$ | Output Power Supply |
| $\overline{SBWd}$ | Write Enable, Byte d (DQ27-DQ35) | ZZ | Asynchronous Sleep Mode |
| TMS,TDI,TCK | IEEE 1149.1 Test Inputs (LVTTL levels) | ZQ | Output Driver Impedance Control |
| TDO | IEEE 1149.1 Test Output (LVTTL level) | NC | No Connect |

## Ordering Information

| Part Number | Organization | Speed | Leads |
|---|---|---|---|
| IBM0436A8ACLAB - 3P | 256K x 36 | 3.7ns Access / 3.8ns Cycle | 7 x 17 BGA |
| IBM0436A8ACLAB - 4P | 256K x 36 | 4.2ns Access / 4.2ns Cycle | 7 x 17 BGA |
| IBM0436A8ACLAB - 4F | 256K x 36 | 4.3ns Access / 4.3ns Cycle | 7 x 17 BGA |
| IBM0436A8ACLAB - 4H | 256K x 36 | 4.5ns Access / 4.5ns Cycle | 7 x 17 BGA |
| IBM0436A8ACLAB - 5 | 256K x 36 | 5.0ns Access / 5.0ns Cycle | 7 x 17 BGA |
| IBM0436A8ACLAB - 5H | 256K x 36 | 5.5ns Access /5.5ns Cycle | 7 x 17 BGA |
| IBM0436A4ACLAB - 3P | 128K x 36 | 3.7ns Access / 3.8ns Cycle | 7 x 17 BGA |
| IBM0436A4ACLAB - 4P | 128K x 36 | 4.2ns Access / 4.2ns Cycle | 7 x 17 BGA |
| IBM0436A4ACLAB - 4F | 128K x 36 | 4.3ns Access / 4.3ns Cycle | 7 x 17 BGA |
| IBM0436A4ACLAB - 4H | 128K x 36 | 4.5ns Access / 4.5ns Cycle | 7 x 17 BGA |
| IBM0436A4ACLAB - 5 | 128K x 36 | 5.0ns Access / 5.0ns Cycle | 7 x 17 BGA |
| IBM0436A4ACLAB - 5H | 128K x 36 | 5.5ns Access /5.5ns Cycle | 7 x 17 BGA |
| IBM0418A4ACLAB - 3P | 256K x 18 | 3.7ns Access / 3.8ns Cycle | 7 x 17 BGA |
| IBM0418A4ACLAB - 4P | 256K x 18 | 4.2ns Access / 4.2ns Cycle | 7 x 17 BGA |
| IBM0418A4ACLAB - 4F | 256K x 18 | 4.3ns Access / 4.3ns Cycle | 7 x 17 BGA |
| IBM0418A4ACLAB - 5 | 256K x 18 | 5.0ns Access / 5.0ns Cycle | 7 x 17 BGA |
| IBM0418A4ACLAB - 5H | 256K x 18 | 5.5ns Access /5.5ns Cycle | 7 x 17 BGA |
| IBM0418A8ACLAB - 3P | 512K x 18 | 3.7ns Access / 3.8ns Cycle | 7 x 17 BGA |
| IBM0418A8ACLAB - 4P | 512K x 18 | 4.2ns Access / 4.2ns Cycle | 7 x 17 BGA |
| IBM0418A8ACLAB - 4F | 512K x 18 | 4.3ns Access / 4.3ns Cycle | 7 x 17 BGA |
| IBM0418A8ACLAB -4H | 512K x 18 | 4.5ns Access / 4.5ns Cycle | 7 x 17 BGA |
| IBM0418A8ACLAB -5 | 512K x 18 | 5.0ns Access / 5.0ns Cycle | 7 x 17 BGA |
| IBM0418A8ACLAB -5H | 512K x 18 | 5.5ns Access /5.5ns Cycle | 7 x 17 BGA |

## Revision Log

| Revision | Contents of Modification |
|---|---|
| 5/99 | Initial Release, including 3.8ns speed sort. |

For a complete datasheet, please contact your IBM sales representative.



For more information contact your IBM Microelectronics sales representative or
visit us on World Wide Web at http://www.chips.ibm.com

IBM Microelectronics manufacturing is ISO 9000 compliant.