INCH-POUND

MIL-M-38510/706A
29 October 1991
SUPERSEDING
MIL-M-38510/706
28 October 1988

MILITARY SPECIFICATION

MICROCIRCUITS, LINEAR, BIPOLAR, SEMICUSTOM (CELL ARRAY) DEVICES, MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, bipolar, semicustom (cell array) devices. Two product assurance classes (B and S) and a choice of case outline/lead finish are provided for each type, and are reflected in the complete Part or Identifying Number (PIN).

1.2 PIN. The PIN shall be in accordance with MIL-M-38510, and as specified herein.

1.2.1 Device types. The device types (total number of usable cells) and circuit organization shall be as identified in the specific altered item drawing (AID) and as follows:

Device type	Circuit
01	≤ 8 macrocell locations
02	≤ 12 macrocell locations
03	≤ 16 macrocell locations
04	≤ 4 macrocell locations
05	Multichip; see AID for individual die types

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

Letter	Case outline (see MIL-M-38510, appendix C)	Manufacturer (see 6.4)
C	D-1 (14-lead, .785" x .310" x .200"), dual-in-line package	1/
E	D-2 (16-lead, .840" x .310" x .200"), dual-in-line package	A
J	D-3 (24-lead, 1.290" x .610" x .225"), dual-in-line package	1/
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package	A
P	D-4 (8-lead, .405" x .310" x .200"), dual-in-line package	1/
Q	D-5 (40-lead, 2.096" x .620" x .225"), dual-in-line package	A
R	D-8 (20-lead, 1.060" x .310" x .200"), dual-in-line package	A
V	D-6 (18-lead, .960" x .310" x .200"), dual-in-line package	A
X	C-5 (44-terminal, .662" x .120"), square chip carrier package	A
Y	See figure 2 (28-lead, 1.490" x .310" x .200"), dual-in-line package	A
Z	C-J1 (44-terminal, .658" x .658" x .190"), J-leaded chip carrier package	A
2	C-2 (20-terminal, .358" x .100"), square chip carrier package 2/	A
3	C-4 (28-terminal, .460" x .100"), square chip carrier package	A

1/ These outlines are not available from any manufacturer for any device type at this time.
2/ Available for device type 01 only.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441-5700, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A
FSC 5962

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1.3 Absolute maximum ratings.

Supply voltage - +32 V dc or ±16 V dc
Differential input voltage - - - - - - - - - - - - - +30 V
Input voltage range - - - - - - - - - - - - - - - - - +15 V
npn/pnp small device collector current - - - - - - 10 mA
npn large device collector current - - - - - - - - 200 mA
Macrocell biasing current (I_{set}) - - - - - - - - - - 2 mA
Junction temperature (T_J) - - - - - - - - - - - - - +175°C
Maximum power dissipation - - - - - - - - - - - - - 900 mW
Storage temperature range - - - - - - - - - - - - - -65°C to +150°C
Operating temperature range - - - - - - - - - - - - -55°C to +125°C
Lead temperature (soldering, 10 seconds) - - - - - +300°C

1.4 Recommended dc operating conditions.

Supply voltage (V_{CC}):
Single supply- +5 V dc to +30 V dc
Dual supply- ±15 V dc
DC input voltage range (V_{IN}) - - - - - - - - - - - - $+V_{CC}$
Ambient operating temperature (T_A) - - - - - - - - - -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.2).

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-976 - Certification Requirements for JAN Microcircuits.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Standardizatioon Document Order Desk, Building 4D, Robbins Avenue, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document forms a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation (see 6.2).

RAYTHEON COMPANY, SEMICONDUCTOR DIVISION

RLA Series Linear Array Design Manual

(Applications for copies should be addressed to Raytheon Company, Semiconductor Division, 350 Ellis Street, Mountain View, CA 94039-7016.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for related associated detail specifications, specification sheets, or MS standards), the text of this document shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Altered item drawing (AID) requirements. 3/ The following items, as a minimum, must be provided to the device manufacturer by the customer as part of an altered item drawing:

3.2.1 Terminal connections and pin assignments.

3.2.2 Package type selected from manufacturer's offering and in accordance with MIL-M-38510, appendix C (see 1.2.3).

3.2.3 Functional block diagram.

3.2.4 Functional description, terms, and symbols.

3.2.5 Cell-level diagram.

3.2.6 Pin function description.

3.2.7 Schematic circuits. The schematic circuits describing the personalized cell array shall be included.

3.2.8 Device electrical performance characteristics. To include dc parametric, ac parametric, and ac functional, as selected from the manufacturer's data sheet. Electrical performance characteristics apply over the full recommended ambient operating temperature range.

3.2.9 Dynamic response diagram. The dynamic response diagram will show all critical interrelated inputs and outputs. Response diagrams shall consist of one or more diagrams showing critical inter-relationships between two or more signals. Applicable response requirements, such as settling times, slew rates, and propagation delays, will also be shown.

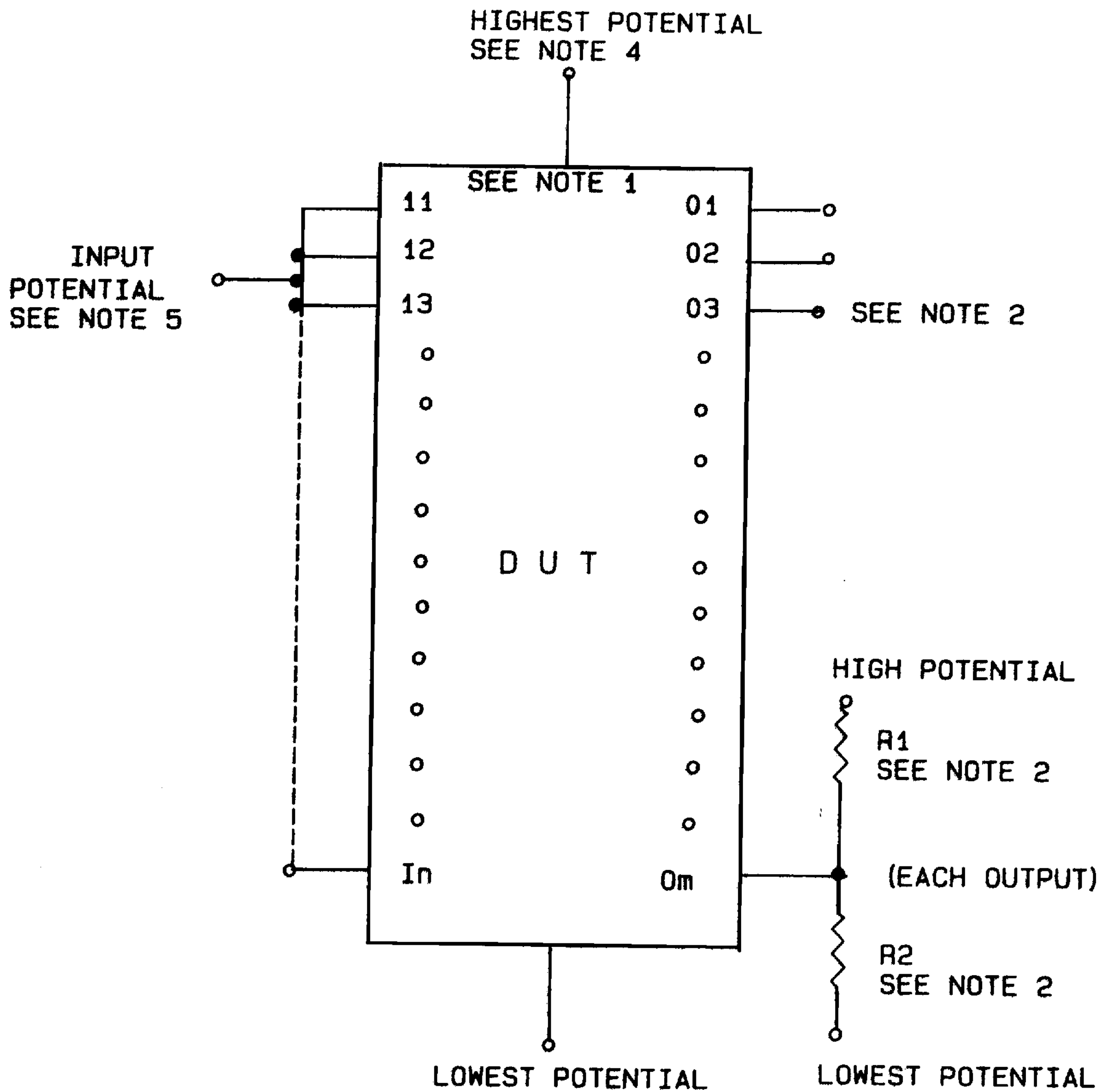
3.2.10 Burn-in circuit. The burn-in circuit shall be as specified on figure 1 herein for the AID device.

3.2.11 Maximum power dissipation and thermal characteristics. In accordance with 1.3 and MIL-M-38510, appendix C.

3.2.12 Device type. As specified in 1.2.1 herein. When device type 05 is used, the AID shall contain information describing the types of die used, as well as their physical and electrical configuration.

3.2.13 Case outlines. The case outlines shall be as specified in 1.2.3 herein and figure 2.

3/ An altered item drawing, (AID) contains all essential information (design, test, etc.) regarding a particular customer personalization of a cell array microcircuit.



NOTES:

1. I = input, O = output, n (m) = highest numbered input (output).
2. All outputs are connected through load resistors to the highest and lowest potentials The value of the resistor shall be chosen so as not to overstress the output stage beyond its current sourcing/sinking capacity.
3. Pin designations determined by customer configuration.
4. In the case of multiple power pins, all connections shall be tied to the appropriate level.
5. Potential chosen such that the input stages are reversed biased. As a minimum, reverse bias voltage will equal the maximum recommended supply voltage.

FIGURE 1. Burn-in circuit requirements (device specific).

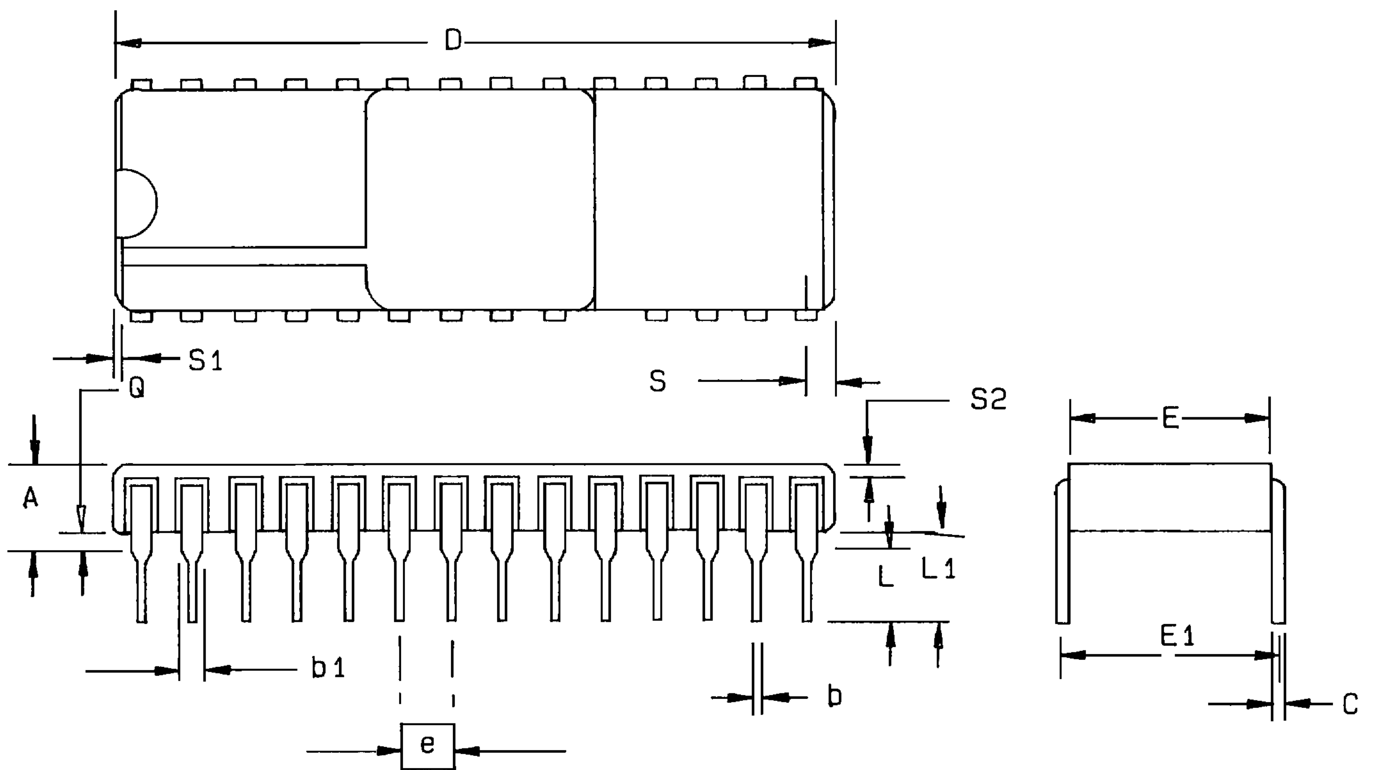


FIGURE 2. Case outline Y.

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A		.200		5.08	
b	.014	.023	0.36	0.58	8
b1	.038	.065	0.97	1.65	2, 8
c	.008	.015	0.20	0.38	8
D		1.490		37.85	4
E	.280	.310	7.71	7.87	4
E1	.290	.320	7.37	8.13	7
E2					
E3					
e	.100 BSC		2.54 BSC		5, 9
L	.125	.200	3.18	5.08	
L1	.150		3.81		
Q	.015	.060	0.38	1.52	3
Q1					
S		.100		2.54	6
S1	.005		0.13		6
S2	.005		0.13		
α	0°	15°	0°	15°	

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimension "b1" may be .023 (0.58 mm) for leads number 1, 14, 15, and 28 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus, and glass overrun.
5. The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within ± .010 (0.25 mm) of its exact longitudinal position relative to pins 1 and 28.
6. Applies to all four corners (leads number 1, 14, 15, and 28), and 5.2 shall apply.
7. Lead center when "a" is 0°. "E1" shall be measured at the centerline of the leads.
8. All leads: Increase maximum limit by .003 (0.08 mm) measured at the center of the flat, when lead "A" is applied.
9. Twenty-six spaces.
10. Dimensions are in inches.
11. Metric equivalents are given for general information only.

FIGURE 2. Case outline Y - Continued.

3.2.14 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.

3.2.14.1 Silver-filled glass die attach. The use of silver-filled glass die attach material is allowed, subject to requirements as outlined in DESC-EQM letter 87-2364, revision A, dated 1 March 89, entitled "Silver-Glass Die Attach Requirements MIL-M-38510, FSC 5962."

3.2.15 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510.

3.2.16 Electrical performance characteristics. Each manufacturer shall submit to the qualifying activity a data sheet defining the cell array family being qualified. The data sheet shall contain all dc parametric, ac functional and parametric data and any other data which is manufacturer dependent but would be considered required by a design engineer. Electrical performance characteristics shall be specified using the format of table I, herein. All electrical performance characteristics apply over the full recommended ambient operating temperature range. (The Standard Evaluation Circuit (SEC) see 4.3.2.2) electrical performance characteristics are as specified in the AID for each manufacturer's SEC.)

3.2.17 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups in table II herein. The electrical tests for each subgroup are described in the AID (for the user design) and in the AID for each manufacturer's SEC. When specified in the AID, electrical test requirements shall follow the format of either table I or table III, herein.

3.2.18 Marking. The marking shall be in accordance with MIL-M-38510. The altered item drawing number shall be added to the marking by the manufacturer. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container.

3.3 Additional line certification requirements. In addition to the requirements of MIL-STD-976, the following documentation shall be provided to the qualifying activity for review approval. This documentation will remain on file for internal Government use only.

a. Design/layout rules as a manufacturer's controlled document.

b. A list of the macros in the manufacturer's macrocell library, macrocell performance data and macrocell simulation verification data (see 4.3.2.3). A description of the process used by the manufacturer for adding new macrocells to the library shall also be provided.

c. Process control monitor design used by the manufacturer for qualification and wafer acceptance (see 4.3.2.1).

d. Standard evaluation circuit implementation in the form of an AID (see 4.3.2.2 for discussion of this circuit) used by the manufacturer for qualification and quality conformance inspection (SEC design details, test conditions, and all required information will be contained in the AID for each manufacturer's SEC).

e. Cell array benchmark set (see appendix and 4.3.2.4) delay simulation data (when applicable).

f. A list of the software packages (including names and current version) used by the manufacturer in the cell array design process.

g. A design rule check (DRC) and an electrical rule check (ERC) shall be performed by the manufacturer on all designs. If the DRC and/or ERC are done using an automated process, the effectiveness of the software must be demonstrated by running a design with known rule violations. The output shall be presented to the qualifying activity, and must show that the rule violations were flagged. If the DRC and/or ERC are done manually, the effectiveness of the manual procedure must be proven by submitting a document to the qualifying activity describing the manual DRC and/or ERC process.

h. A layout versus schematic (LVS) check must be performed by the manufacturer. If the LVS check is done using an automated process, the manufacturer must demonstrate the effectiveness of the LVS software as in 3.3g herein. If the LVS check is done manually, the effectiveness of the manual procedure must be shown as in 3.3g herein.

3.4 Functional cell-interaction simulation. Functional cell-interaction simulation shall be retained by manufacturer; simulation to be derived from each final application specific electrical design and layout (i.e., post-routed design). Simulation shall be done using actual interactions as computed from the placement and layout of the device as it will be fabricated. The simulation shall include the effects associated with the cell(s), as well as the effects from the actual metal capacitance and loading on the cell(s). The simulation will show that at the two worst case extremes of temperature, supply voltage, and process, the circuit will operate as specified, and all cells will interact properly.

3.5 Layout verification. The manufacturer shall retain the results of full, mask level design rule checks, electrical rule checks and connectivity checks for each application specific design. Rule checking will encompass the rules set provided under 3.3a herein. The manufacturer will explain any rules not checked and all error reports produced. The LVS check will ensure that the layout matches exactly the schematic simulated by the application specific integrated circuit (ASIC) designer.

3.6 Power routing simulation 4/. Power routing simulation shall be retained by the organization performing the simulation; derived from each final application specific electrical design and layout. The worst case simulation of power supply interconnects shall show that at no time will the localized current density for the internal conductors exceed specification for allowable current density for the internal conductor material as defined in MIL-M-38510. In addition, the voltage levels for the power supply interconnects shall not exceed recommended IR drop values from the respective supply. Power routing simulation must be based upon actual placement of cells within the array.

3.7 Procedure for updating certified software packages. Each manufacturer shall submit to the qualifying activity for review the procedure used for approval of updates and revisions of certified software packages (see 3.3f). This procedure shall outline the method and provide test descriptions regarding the process used to accept/reject updates and revisions to in-house or commercially supplied software packages. This requirement only applies to software packages used by the manufacturer in the cell array design process.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group assignment number 122 (see MIL-M-38510, appendix E).

TABLE I. DC electrical performance characteristics. 1/ 2/

Test	Symbol	Conditions	Limits		Unit
			Min	Max	

1/ This table supplies a minimum configuration for the respective table that is to be supplied in the AID (see 3.2.8 and 3.2.16).
2/ Limits apply for -55°C ≤ T_A ≤ +125°C.

4/ A manufacturer may take an alternate path for qualification of the specific cell array family members without accounting for specific uses of the array. Such a qualification would be a worst case simulation of each cell array family member by populating all cell positions with the worst case power consumption cells (100 percent utilization).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein.

4.1.1 Wafer lot acceptance procedure. Each manufacturer shall submit to the qualifying activity for approval a "Wafer lot acceptance procedure." This procedure shall outline and provide limits regarding the process used to accept/reject a wafer lot. The procedure shall include:

a. Physical measurements of wafer metallization, glassivation, and gold backing in accordance with method 5007 of MIL-STD-883.

b. Electrical measurements using the process monitor (PM) (Note: The PM may be a dedicated drop-in or a set of structures in the kerf or scribe line.)

c. Visual inspection to include:

(1) High magnification examination on a sample basis.

(2) Optical test structures to insure alignment, etc.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test conditions A and C using the circuit requirements shown on figure 1 for class S devices. For class B devices, test condition C using the circuit requirements shown on figure 1.

(2) T_A = +125°C minimum.

b. Interim and final electrical tests shall be as specified in table II herein, except interim electrical tests prior to burn-in are optional at the discretion of the manufacturer.

c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

4.3 Qualification inspection.

4.3.1 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510, and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). In addition, the five-phased qualification outlined as follows shall be performed through the use of the identified qualification vehicles.

4.3.2 Qualification phase and vehicles.

Qualification phase	Qualification vehicles
Process control and stability	Process monitor (PM)
Process reliability	Standard evaluation circuit (SEC)
Macrocell design and simulation	Macro test chip set
Post routing simulation	Cell array benchmark set
Design check verification	Manufacturer test case or design check procedure

Note: Qualification of the Macrocell design and simulation and CAD and post routing simulation will be based on the manufacturer's ability to design, place and route, and manufacture devices where actual measured performance characteristics (i.e., propagation delays, settling times, drive characterization, trigger levels, etc.) are within simulated device performance limits (see 4.3.2.4).

4.3.2.1 Process control and stability. Process control and stability of dc parameters must be demonstrated through the use of the manufacturer's process monitor (PM). The PM (either a dedicated drop-in or structures fabricated in the kerf) shall be designed so that the dc and ac process parameters (for class B, ac parameters may be included as a manufacturer's option) may be measured in wafer form or packaged device form. The PM design must be submitted to the qualifying activity for approval prior to use for qualification and must contain as a minimum the following structures:

a. npn and pnp minimum geometry device.

b. npn and pnp maximum geometry device.

c. Sheet resistance measurement structure.

d. Metal step coverage structure.

e. Intermetal oxide integrity structure.

f. Contact chains (to be of sufficient length to be representative of the contact resistance).

(1) Metal 1 to metal 2 (where applicable).

(2) Metal 2 to metal 3 (where applicable).

(3) Metal to poly (where applicable).

(4) Metal to diffusion (where applicable).

For qualification, PM's on a minimum of three different lots (minimum of 4 PM's per wafer) shall be measured to insure the establishment of a statistically valid data base on which a decision can be made as to whether the manufacturer's process is stable and under control. Recent lot history data can be used to satisfy this requirement. (For quality conformance inspection, measurement of PM parameters will be required in accordance with method 5007 of MIL-STD-883 for wafer lot acceptance, see 4.1.1.)

4.3.2.2 Process reliability. The process reliability is to be qualified using the manufacturer's SEC. The SEC design shall be submitted to the qualifying activity for approval prior to use in the form of a manufacturer's altered item drawing, and as such shall contain the basic information as detailed in sections 3.2.1 through 3.2.9. It shall be fabricated with the same process that will produce any application specific cell array device under this detail specification. The SEC design shall be configured in such a manner so as to evaluate the reliability of the underlayer designs (diffusions, etc.) and evaluate worst case design rule conditions on the personalization layers. The design should utilize library macrocells as well as test structures which will detect metal to metal shorting or opening, high via resistance and dielectric pinholes during reliability life testing. The SEC shall be implemented on the largest member (i.e., The device type with the largest number of cells and if applicable with the highest pin count package) of the cell array family. Smaller cell count members of the cell array family in the highest pin count package or in smaller pin count packages may be qualified by extension (see 4.3.3).

The SEC will also be the main qualification vehicle for the electrical testing which follows (see 4.4.1, 4.4.2, 4.4.3, and 4.4.4). Test limits appear in the AID for each manufacturer's SEC. The electrical test for each subgroup shall be described in the AID. The SEC shall be suitable for both static and dynamic biased aging, as life testing will be performed on this device (see 4.4.3).

4.3.2.3 Macrocell design and simulation qualification. The macrocell design and simulation qualification shall be accomplished in a two step procedure consisting of parameter verification/simulation verification and functional verification.

A chip set shall be designed to provide access to a set of macrocells to test performance characteristics. Macrocell substitutions are allowable only if the manufacturer does not offer a particular macrocell, and such substitutions must be approved by the qualifying activity. The set of macrocells shall include:

Macrocell	Description
MNIM	npn current mirror
MPCS	pnp current source
MPIS	pnp input stage
MPND	pnp/npn driver
MND	npn output driver
MGS	Basic gain stage
MOPA	Operational amplifier
MCMP	Comparator

The intent is to get a representative cross section of macrocell types. Chains shall be formed (when necessary to avoid response and settling time measurement problems) and actual performance data over the full operating range shall be taken. Delay versus metal wire length and fanout for the above macrocells shall be determined. The actual performance data shall be submitted to the qualifying activity along with computer simulation results. The actual performance data must be within the limits predicted by the simulation. If multipliers are used to extrapolate performance at the temperature extremes, such multipliers shall be verified as well.

In addition, for the above macrocells, a set of pins shall be provided on the test chip for observability. This will enable verification of functionality of the macrocells.

4.3.2.4 Post routing simulation. A chip or set of chips incorporating the cell array benchmark set shall be used to qualify the manufacturer's ability to perform routing and to accurately predict post routing performance. The manufacturer must submit to the qualifying activity:

a. The actual measured performance data for each function in the benchmark over temperature and voltage.

b. The computer performance simulation prediction. The two results will remain on file and the actual measured performance data values must fall between the two worst case (temperature and voltage) performance simulation prediction limits.

4.3.2.5 Design check verification. The manufacturer shall verify that the design checks (DRC, ERC and LVS check) are effective. If any or all of the design checks are done by an automated process, the manufacturer will run a design containing known rule violations through the appropriate checker, and show that the checker(s) flagged the errors. If any or all of the design checks are performed manually, the manufacturer will submit to the qualifying activity a document describing the appropriate check procedure(s).

4.3.2.6 Schematic circuits. The schematic circuits describing the unpersonalized cell array shall be submitted to the qualifying activity as a prerequisite for qualification. All qualified manufacturer's schematics shall be maintained by the agent activity (DESC-ECS) and will be available on request. The typical schematic shall be in terms of a qualifying activity approved standard.

4.3.3 Qualification extension. For qualification inspection if a manufacturer qualifies the SEC (i.e., the highest cell count array) in the highest pin count package type, then lower cell count arrays in that package type, that are manufactured identically (i.e., same line, same process) as the SEC may be part I qualified upon approval of the qualifying activity.

a. Lower cell count arrays in lower pin count packages that are manufactured identically (i.e., same line, same process) as the SEC may be part I qualified upon the approval of the qualifying activity using another die, provided the cell utilization is 60 percent or greater and by conducting group A electrical tests and any electrical subgroups, if required by the qualifying activity on lower pin count packages, added to group C tests in table II herein for the die extension.

b. Package extension may be achieved by performing subgroups 2, 3, and 5 of group B tests and all group D tests of method 5005 of MIL-STD-883 for the package extension. Data for qualification extension must be submitted in accordance with appendix D of MIL-M-38510.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 and 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

a. Test requirements shall be specified in the AID and as follows:

b. The vehicles to be used for the group A inspection are as follows:

   (1) Qualification: Standard evaluation circuit.

   (2) Quality conformance inspection: Actual user device (via the altered item drawing).

c. Subgroups 7 and 8 of table I of method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883. Electrical test requirements shall be as specified in table II herein, and as follows:

The vehicles to be used for the group B inspection are as follows:

   (1) Qualification: Standard evaluation circuit.

   (2) Quality conformance inspection: Actual user device (via the altered item drawing).

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

a. Qualification and quality conformance inspection shall be performed on the manufacturer's SEC.

b. End-point electrical parameters shall be specified in table II herein, with limits shown in the AID covering the manufacturer's SEC.

c. Steady-state life test (method 1005 of MIL-STD-883).

   (1) Use life-test condition C using the SEC and the circuit requirements shown on figure 1. The life test circuit schematic shall be submitted to the qualifying activity for approval prior to use.

   (2) Test duration 1,000 hours, except as permitted in appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

   (3) T_A = +125°C minimum.

d. The following sample plan shall be used in lieu of table III of method 5005 for all group C subgroups: A sample of 10 SEC devices shall be chosen and submitted to test with no failures allowed. If not more than one failure is found in the first sample of 10, a second sample of 10 SEC devices is permitted with no further failures allowed.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End point electrical parameters shall be as specified in table II herein. The SEC shall be used for group D inspection whenever practical; for a smaller package where the SEC cannot be used, another die may be used provided the cell utilization is 60 percent or greater. Group D inspection shall be performed in accordance with MIL-M-38510, 4.5.5.

TABLE II. Electrical test requirements.

MIL-M-38510 test requirements	Subgroups 1/	
	Class S	Class B
Interim electrical parameters (method 5004)	1	1
Final electrical test 2/ parameters (method 5004)	1,2,3,4,5,6, 9,10,11	1,2,3,4,9
Group A test requirements (method 5005)	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11
Group B test requirements (method 5005, subgroup 5)	1,2,3,4,5,6, 9,10,11	N/A
Group C end-point electrical parameters (method 5005)	N/A	1,2,3,4
Group D end-point electrical parameters (method 5005)	1,4	1,4
Additional electrical tests group C inspection	N/A	N/A

1/ Dynamic tests (subgroups 4, 5, and 6) and switching tests (subgroups 9, 10, and 11) will be performed when required by the customer Altered Item Drawing (AID).

2/ PDA applies to subgroups 1 and 4 (see 4.2c).

TABLE III. Group A inspection for all device types.

Subgroup	Test	Symbol	Test number	MIL-STD-883 method	Conditions	Measured terminal	Limit Min	Max
1/ 2/					3/	4/	3/	3/

1/ Static tests (comprising subgroups 1, 2, and 3) shall be conducted as required by table II of this specification.
2/ When applicable, dynamic tests (comprising subgroups 4, 5, and 6) and switching tests (comprising subgroups 9, 10, and 11) shall be conducted as required by table II of this specification.
3/ Conditions and limits appear in the AID.
4/ Particular terminal(s) to be measured are design specific and must appear in the applicable AID (see 3.2.17).

4.4.5 Constant acceleration. The constant acceleration tests of groups C and D shall be performed using test condition D.

4.5 Methods of inspection. Methods of inspection shall be specified as follows.

4.5.1 Voltage and current. All voltage values given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510. In addition, all devices shall be in contact with a conductive material which shorts all leads together to prevent electrostatic damage.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for use for Government microcircuit applications (original equipment), design applications, and logistic purposes.

6.2 Ordering data.

6.2.1 Acquisition requirements. Acquisition documents must specify the following:

a. Title, number, and date of the specification.

b. Issue of DODISS to be cited in the solicitation, and if required, the specific issue of individual documents referenced (see 2.1 and 2.2).

c. Complete part number (see 1.2).

d. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

e. Requirements for certificate of compliance, if applicable.

f. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.

g. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.

h. Requirements for product assurance options.

i. Requirements for special carriers, lead lengths, or lead forming, if applicable.

j. Requirements for "JAN" marking.

k. Requirements for altered item drawing provided to the manufacturer (see 3.2).

6.3 Logistic support. Lead material and finish (see 3.2.15), are interchangeable. Unless otherwise specified, microcircuits acquired for government logistic support will be acquired to device class B (see 1.2.2), and lead material and finish "C" (see 3.5). Longer length leads and lead forming shall not affect the part number.

6.4 Manufacturer's designations. Manufacturers of device types on this specification are designated in table IV herein. This does not imply qualification or certification; refer to QPL-38510 for information regarding qualified sources.

TABLE IV. Manufacturer's designations.

Device type	A Raytheon
01	RLA80
02	RLA120
03	RLA160
04	RLA40
05	Multichip

6.5 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Manufacturer specific generic-industry type
01, 02, 03, 04, and 05	See listed manufacturer data sheets (6.4)

6.6 PIN. The PIN shall be in accordance with MIL-M-38510, and as specified herein.

APPENDIX

Cell Array Benchmark Set

10. SCOPE

10.1 Scope. This appendix contains benchmark description numbers as required by 4.3.2.4 CAD routing and post routing simulation herein. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. REQUIREMENTS

30.1 Benchmark number description.

a. Track and hold amplifier

b. Analog switch

c. Operational amplifier

d. Comparator

e. 4-bit D/A converter

f. Voltage reference

g. Voltage-to-frequency converter

h. Analog multiplier

CONCLUDING MATERIAL

Custodians:
Air Force - 17
Navy - EC
Army - ER
NASA - NA

Review activities:
Army - AR, MI
Navy - OS, SH, TD
Air Force - 11, 19, 85, 99
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC

Preparing activity:
Air Force - 17

Agent:
DLA - ES

(Project 5962-1212)