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SAN3020
APPLICATION NOTE

SINGLE CHIP TELEPHONE POWER EXTRACTION FOR EXTERNAL LOADS

1 Scope

This application note describes a simple add-on circuit for extracting current to supply external loads. It also includes hardware description ,schematic and V_{out}/I_{out} curves.

2 Key Features

- Only few additional low-cost components necessary
- Can drive line currents up to I_{Line}-5mA (=15mA for 20mA line current)
- No influence in AC impedance or DC mask even when load is short circuited

Table of Contents

3 Other applicable documents and papers

1. Data Sheet SA2531, SA2532
2. Pin-out comparison SA2531/2

4 Revision status

SAN3020 Application Note (this document)
AN3020 Schematic Rev. B00

5 General description

Note: all further component references apply to the schematic shown in pt.9 of this application note !

When driving external loads by extracting power from the available line current, care must be taken not to affect both DC and AC impedance. The extracted voltage should be independent from line current (assuming a line current >20mA).
The application shown will shut off the external load when going on-hook and power-up the load when going off-hook.

The current driving capability depends on the available line current, higher line currents allow higher driving currents. At minimum line current (20mA), the maximum load current is ≈15mA (see pt.6 for further details).

6 Hardware configuration

Only 4 external components , shown in the dotted area (1 general purpose PNP transistor:B_{min}=250, 1 general purpose diode , 1 resistor and 1 pol. capacitor) must be added to the standard SA253x application to get a high efficiency power extraction for external loads with the features described in pt.5 above.

When updating an existing circuit, the connection from pin #25 (= CS, SA253x) to the shunt transistor's base (in most applications = Q3) must be opened and a diode (D5) installed. All further components are simply added to the circuit.

7 Circuit description

The shunt transistor (Q3) is regulating the voltage at LI (#27) to ≈ 4.5V. Consequently, the voltage at CS (#25) is V_{LI} - V_{BE}. When adding D5, the voltage drop between LI and CS is Vconst = 2x V_{BE}. This constant voltage provides the base current of the power extraction transistor Q5 via R22.

The maximum load current also depends on the gain (B= I_C / I_B) of the transistor used. The transistor used should have a B of ≥250 . Transistors with lower gain may also be used, but the maximum load current may be lower.

7.1 Minimum output voltage with high signals on line:

As shown in the diagram (pt. 9), the output voltage at high load currents will drop with high transmit or receive signals on line, since the load is not supplied during the negative half-wave of the line signal. The diagram shows the V_{out}/I_{Load} curves with no AC signal at line and with a constant AC line signal of $1V_{peak}$.

In practical use, an AC signal of $2V_{pp}$ is not present continuously, so the effective output voltage will be higher. It is also possible to buffer the voltage drop during line signal bursts by increasing the value of capacitor C19.

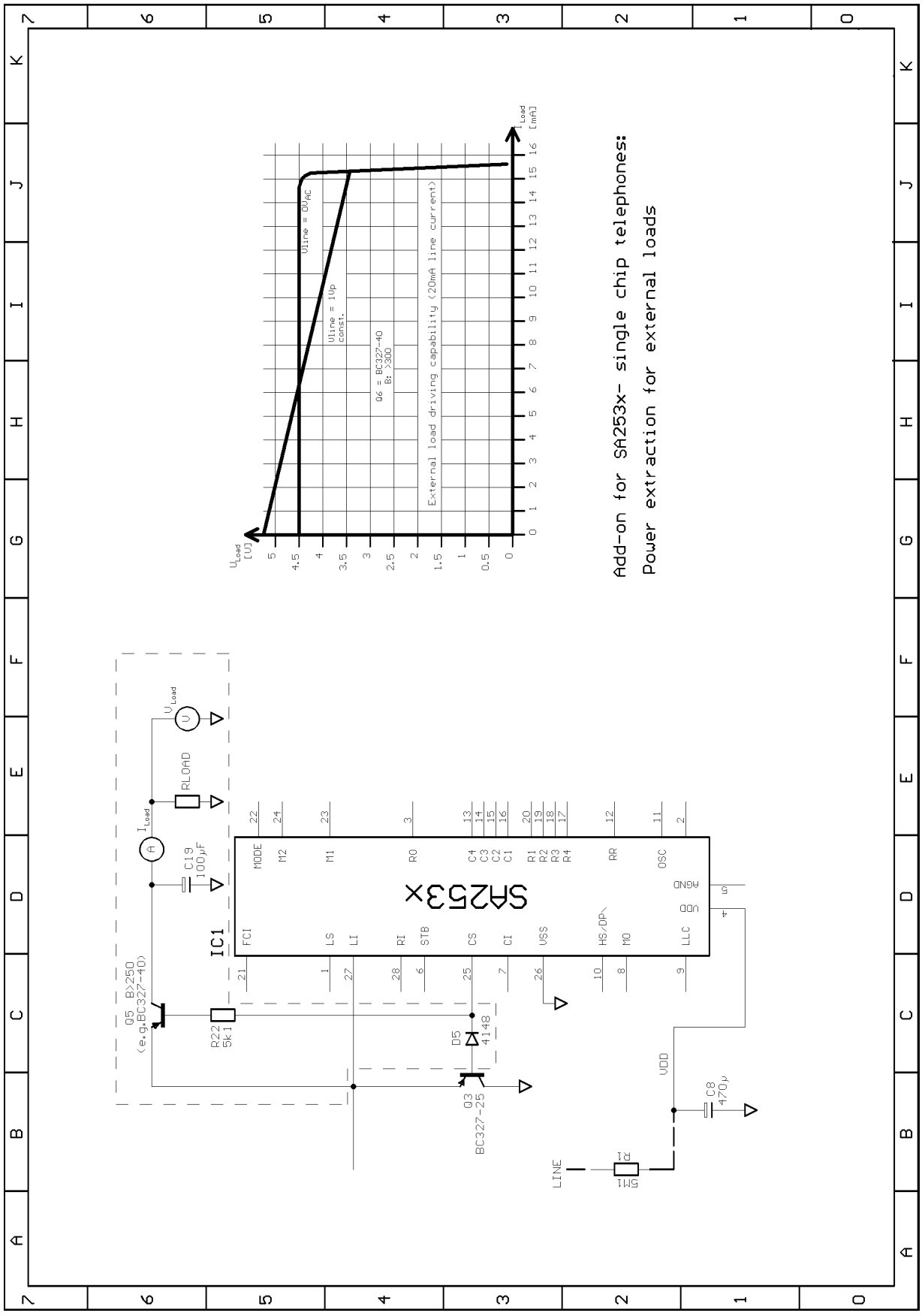
However, the voltage decrease with high signal bursts on line should be taken into consideration when the load voltage must not drop below a certain value.

8 Connecting loads at V_{DD}

Small loads can also be connected at V_{DD} directly, as long as the following rules are observed:

1. When on-hook, the load must only draw <1µA , because it is connected in parallel to the V_{DD} -cap, which maintains memory data retention in on-hook state, charged by a 5MΩ resistor . A higher load current would discharge this capacitor and erase the memory contents.
2. The load will also be supplied in ringing mode.
3. When off-hook, the load current can be <5mA, provided it does not exceed this current at any time.

9 Application schematic



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