Genesys Logic, Inc.

GL852

USB 2.0
MTT
HUB Controller

Datasheet
Revision 1.05
Mar. 29, 2006

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Office:

Genesys Logic, Inc.
12F, No. 205, Sec. 3, Beishin Rd., Shindian City,
Taipei, Taiwan
Tel: (886-2) 8913-1888
Fax: (886-2) 6629-6168

http ://www.genesyslogic.com

Revision History

Revision	Date	Description
1.00	07/07/2005	First release
1.01	09/07/2005	Modify Pin Description, table3.3 ,p.12
1.02	09/15/2005	Modify HUB Interface ,table3.3 Pin Description, p.12
1.03	12/28/2005	Modify Pin List and Pin Descriptions of EE_CS, EE_DI, EE_SK, p.11~12
1.04	01/19/2006	Add AC Characteristics, Ch6.5, p.26
1.05	03/29/2006	Add Input Voltage for digital I/O(Ovcur1-4,Pself,Reset) pins,p23

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1 GENERAL DESCRIPTION

GL852 is Genesys Logic's brand new Hub solutions which fully comply with Universal Serial Bus Specification Revision 2.0. This series includes GL852, and GL852-N.

GL852 embeds an 8-bit RISC processor to manipulate the control/status registers and respond to the requests from USB host. Firmware of GL852 will control its general purpose I/O (GPIO) to access the external EEPROM and then respond to the host the customized PID and VID configured in the external EEPROM. Default settings in the internal mask ROM is responded to the host without having external EEROM. GL852 is designed for customers with much flexibility. The more complicated settings such as PID, VID, and number of downstream ports settings are easily achieved by programming the external EEPROM (Ref. to Chapter 5).

Each downstream port of GL852 supports two-color (green/amber) status LEDs to indicate normal/abnormal status. Both GL852 and GL852-N also support both Individual and Gang modes (4 ports as a group) for power management. (Due to the pin-out limitation, the GL852-N only supports green LEDs. Please refer the table in the end of this chapter for more detail).

To fully meet the performance requirement, GL852 series is a multiple TT hub solution to provide every down stream port with a TT. With the dedicated TT in each down stream port, GL852 can provide the best performance even connect with several Full/Low-Speed devices and running heavy bandwidth-consuming operations concurrently.

*TT (transaction translator) is the main traffic control engine in an USB 2.0 hub to handle the unbalanced traffic speed between the upstream port and the downstream ports.

Product Name	Package type	Power mode	LED support
GL852	64LQFP	Individual/Gang	Green/Amber
GL852-N	48LQFP	Individual/Gang	Green

CHAPTER 2 FEATURES

- Compliant to *USB specification Revision 2.0*
  - 4 downstream ports
  - Upstream port supports both high-speed (HS) and full-speed (FS) traffic
  - Downstream ports support HS, FS, and low-speed (LS) traffic
  - 1 control pipe (endpoint 0, 64-byte data payload) and 1 interrupt pipe (endpoint 1, 1-byte data payload)
  - Backward compatible to *USB specification Revision 1.1*
- On-chip 8-bit micro-processor
  - RISC-like architecture
  - USB optimized instruction set
  - Dual cycle instruction execution
  - Performance: 6 MIPS @ 12MHz
  - With 64-byte RAM and 2K internal ROM
  - Support customized PID, VID by reading external EEPROM
  - Support downstream port configuration by reading external EEPROM
- Multiple Transaction translator (MTT)
  - MTT provides respective TT control logics for each downstream port. This is a performance better choice for USB 2.0 hub.
- Each downstream port supports two-color status indicator, with automatic and manual modes compliant to USB specification Revision 2.0 (GL852)
- Support both individual and gang modes of power management and over-current detection for downstream ports
- Support gang mode of power management and over-current detection for downstream ports
- Conform to bus power requirements
- Automatic switching between self-powered and bus-powered modes
- Integrate USB 2.0 transceiver
- PLL embedded with external 12 MHz crystal
- Operate on 3.3 Volts
- Embed serial resister for USB signals and integrate pull-up resister for upstream USB signal
- Improve output drivers with slew-rate control for EMI reduction
- Internal power-fail detection for ESD recovery
- 64-pin LQFP package (GL852), 48-pin LQFP package (GL852-N)
- Applications:
  - Stand-alone USB hub
  - Monitor hub
  - PC motherboard USB hub, Docking of notebook
  - Any compound device to support USB HUB function

CHAPTER 3 PIN ASSIGNMENT

3.1 Pinouts

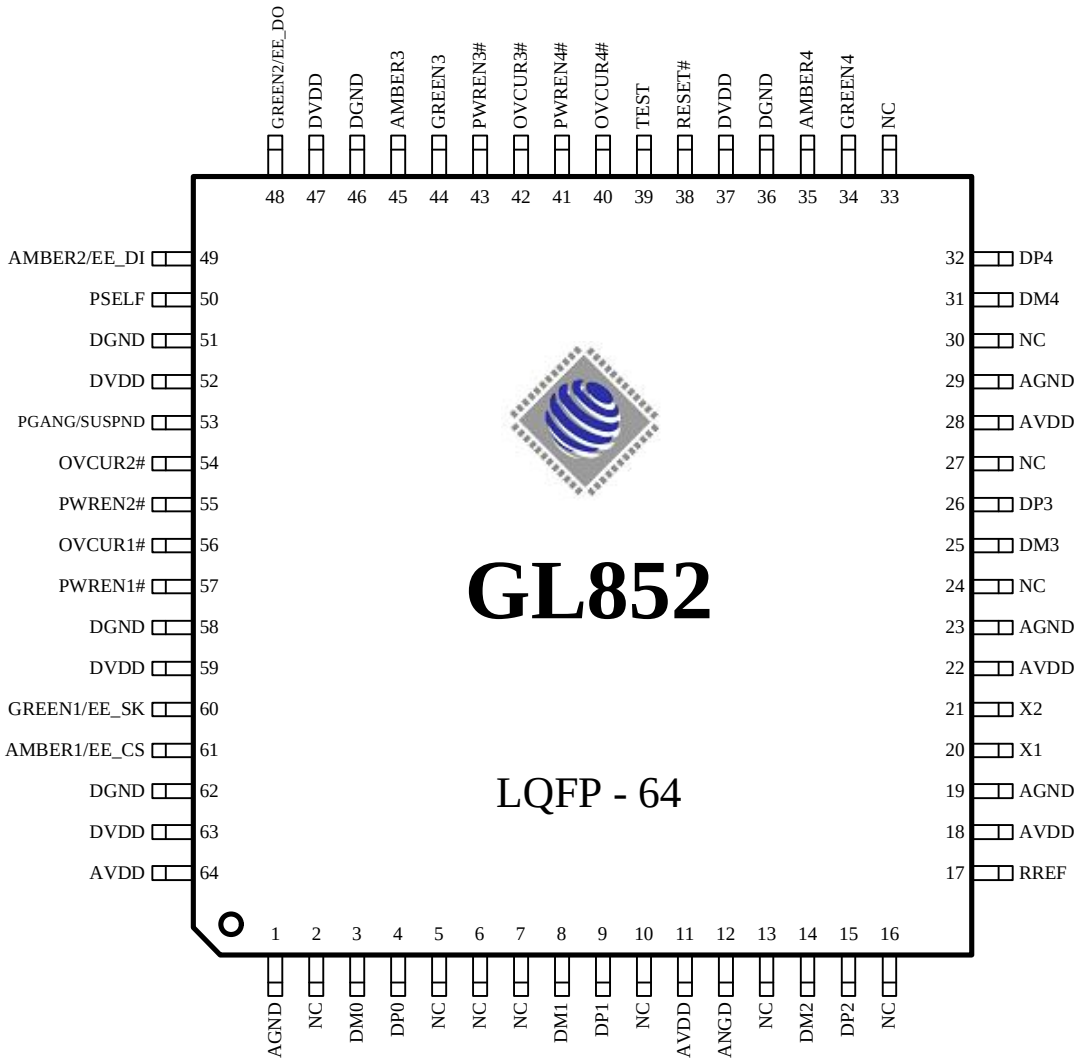


Figure 3.1－GL852 64 Pin LQFP Pinout Diagram

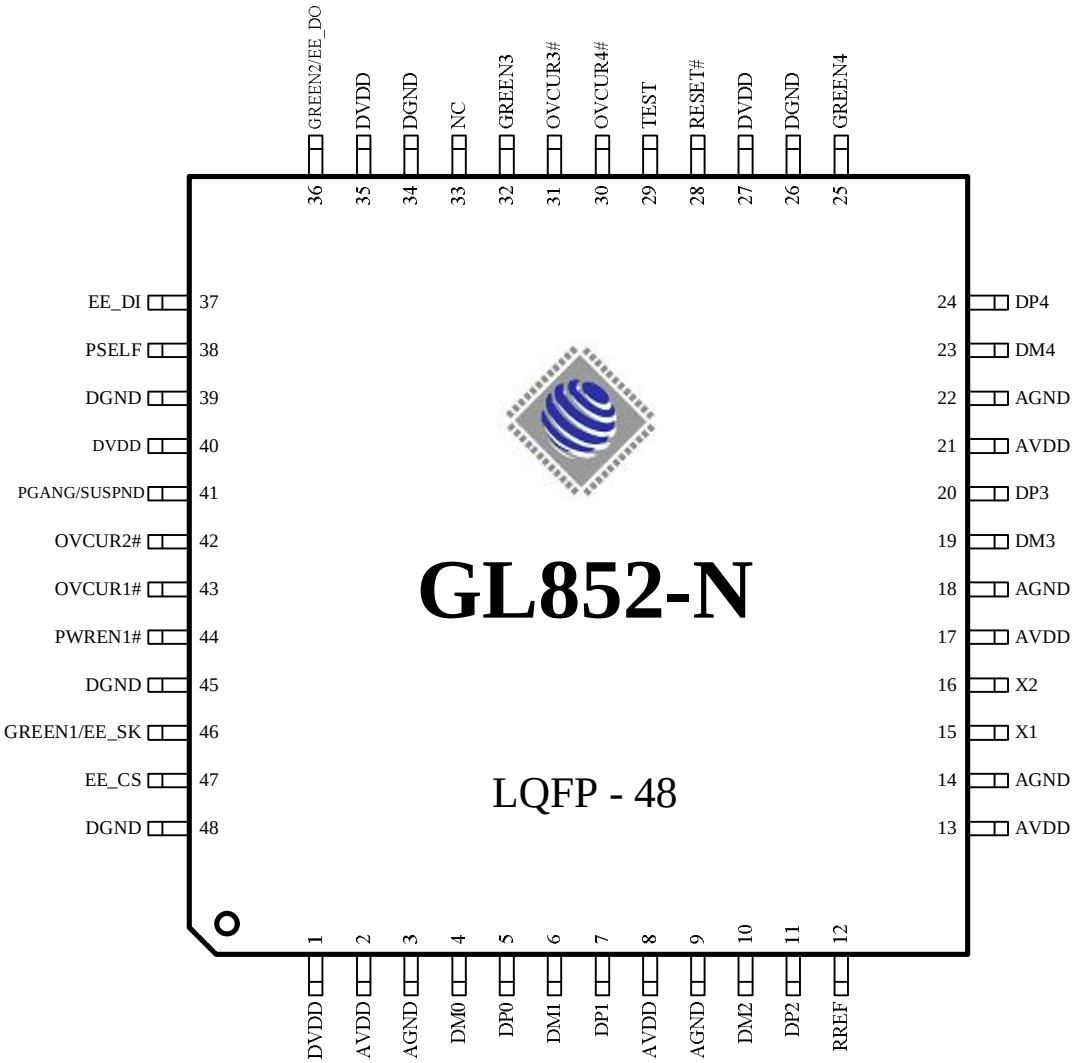


Figure 3.2－GL852-N 48 Pin LQFP Pinout Diagram

3.2 Pin List

Table 3.1－GL852 64 Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	AGND	P	17	RREF	B	33	NC	-	49	AMBER2/ EE_DI	O
2	NC	-	18	AVDD	P	34	GREEN4	O	50	PSELF	I
3	DM0	B	19	AGND	P	35	AMBER4	O	51	DGND	P
4	DP0	B	20	X1	I	36	DGND	P	52	DVDD	P
5	NC	-	21	X2	O	37	DVDD	P	53	PGANG/ SUSPND	B
6	NC	-	22	AVDD	P	38	RESET#	I	54	OVCUR2#	I
7	NC	-	23	AGND	P	39	TEST	I	55	PWREN2#	O
8	DM1	B	24	NC	-	40	OVCUR4#	I	56	OVCUR1#	I
9	DP1	B	25	DM3	B	41	PWREN4#	O	57	PWREN1#	O
10	NC	-	26	DP3	B	42	OVCUR3#	I	58	DGND	P
11	AVDD	P	27	NC	-	43	PWREN3#	O	59	DVDD	P
12	AGND	P	28	AVDD	P	44	GREEN3	O	60	GREEN1/ EE_SK	O
13	NC	-	29	AGND	P	45	AMBER3	O	61	AMBER1/ EE_CS	O
14	DM2	B	30	NC	-	46	DGND	P	62	DGND	P
15	DP2	B	31	DM4	B	47	DVDD	P	63	AVDD	P
16	NC	-	32	DP4	B	48	GREEN2/ EE_DO	B	64	AVDD	P

Table 3.2－GL852-N 48 Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	DVDD	P	13	AVDD	P	25	GREEN4	O	37	EE_DI	O
2	AVDD	P	14	AGND	P	26	DGND	P	38	PSELF	I
3	AGND	P	15	X1	I	27	DVDD	P	39	DGND	P
4	DM0	B	16	X2	O	28	RESET#	I	40	DVDD	P
5	DP0	B	17	AVDD	P	29	TEST	I	41	PGANG/ SUSPND	B
6	DM1	B	18	AGND	P	30	OVCUR4#	I	42	OVCUR2#	I
7	DP1	B	19	DM3	B	31	OVCUR3#	I	43	OVCUR1#	I
8	AVDD	P	20	DP3	B	32	GREEN3	O	44	PWREN1#	O
9	AGND	P	21	AVDD	P	33	NC	-	45	DGND	P
10	DM2	B	22	AGND	P	34	DGND	P	46	GREEN1/ EE_SK	O

11	DP2	B	23	DM4	B	35	DVDD	P	47	EE_CS	O
12	RREF	B	24	DP4	B	36	GREEN2/ EE_DO	B	48	DGND	P

3.3 Pin Descriptions

Table 3.3 - Pin Descriptions

USB Interface				
Pin Name	**GL852 64 Pin#**	**GL852-N 48Pin#**	**I/O Type**	**Description**
DM0,DP0	3,4	4,5	B	USB signals for USPORT
DM1,DP1	8,9	6,7	B	USB signals for DSPORT1
DM2,DP2	14,15	10,11	B	USB signals for DSPORT2
DM3,DP3	25,26	19,20	B	USB signals for DSPORT3
DM4,DP4	31,32	23,24	B	USB signals for DSPORT4
RREF	17	12	B	A 680Ω resister must be connected between RREF and analog ground (AGND).

Note: USB signals must be carefully handled in PCB routing. For detailed information, please refer to **GL852 Design Guideline**.

HUB Interface				
Pin Name	**GL852 64 Pin#**	**GL852-N 48Pin#**	**I/O Type**	**Description**
OVCUR1#~4	56,54, 42,40	43,42,31,30	I (pu)	Active low. Over current indicator for DSPORT1~4 OVCUR1# is the only over current flag for GANG mode.
PWREN1#~4	57,55, 43,41	44	O	Active low. Power enable output for DSPORT1~4 PWREN1# is the only power-enable output for GANG mode.
GREEN1~4	60,48, 44,34	46,36,32,25	1,3,4: O 2: B (pd)	Green LED indicator for DSPORT1~4 *GREEN[1~2] are also used to access the external EEPROM For detailed information, please refer to Chapter 5.
AMBER1~4	61,49, 45,35	-	O (pd)	Amber LED indicator for DSPORT1~4 *Amber [1~2] are also used to access the external EEPROM
EE_CS/ EE_DI	-	47,37	O	Used to access the external EEPROM. For detailed information, please refer to Chapter 5.
PSELF	50	38	I	0: GL852 is bus-powered. 1: GL852 is self-powered.
PGANG/ SUSPND	53	41	B	This pin is default put in input mode after power-on reset. Individual/gang mode is strapped during this period. After the strapping period, this pin will be set to output mode, and then output high for normal mode. When GL852 is suspended, this pin will output low. *For detailed explanation, please see Chapter 5 Gang input:1, output: 0@normal, 1@suspend Individual input:0, output: 1@normal, 0@suspend

Clock and Reset Interface				
Pin Name	GL852 48Pin#	GL852-N 48Pin#	I/O Type	Description
X1	20	15	I	12MHz crystal clock input.
X2	21	16	O	12MHz crystal clock output.
RESET#	38	28	I	Active low. External reset input, default pull high 10KΩ. When RESET# = low, whole chip is reset to the initial state.

System Interface				
Pin Name	GL852 64 Pin#	GL852-N 48Pin#	I/O Type	Description
TEST	39	29	I (pd)	0: Normal operation. 1: Chip will be put in test mode.

Power / Ground				
Pin Name	GL852 64 Pin#	GL852-N 48Pin#	I/O Type	Description
AVDD	11,18,22, 28,64	2,8,13,17,21	P	3.3V analog power input for analog circuits.
AGND	1,12,19, 23,29	3,9,14,18,22	P	Analog ground input for analog circuits.
DVDD	37,47, 52,59	1,27,35,40	P	3.3V digital power input for digital circuits
DGND	36,46, 51,58,62	26,34,39,45, 48	P	Digital ground input for digital circuits.
NC	2,5~7,10, 13,16,24, 27,30,33	33	-	No connection

Note: Analog circuits are quite sensitive to power and ground noise. PCB layout must take care the power routing and the ground plane. For detailed information, please refer to **GL852 Design Guideline**.

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	B/I	Bi-directional, default input
	B/O	Bi-directional, default output
	P	Power / Ground
	A	Analog
	SO	Automatic output low when suspend
	pu	Internal pull up
	pd	Internal pull down
	odpu	Open drain with internal pull up

CHAPTER 4 BLOCK DIAGRAM

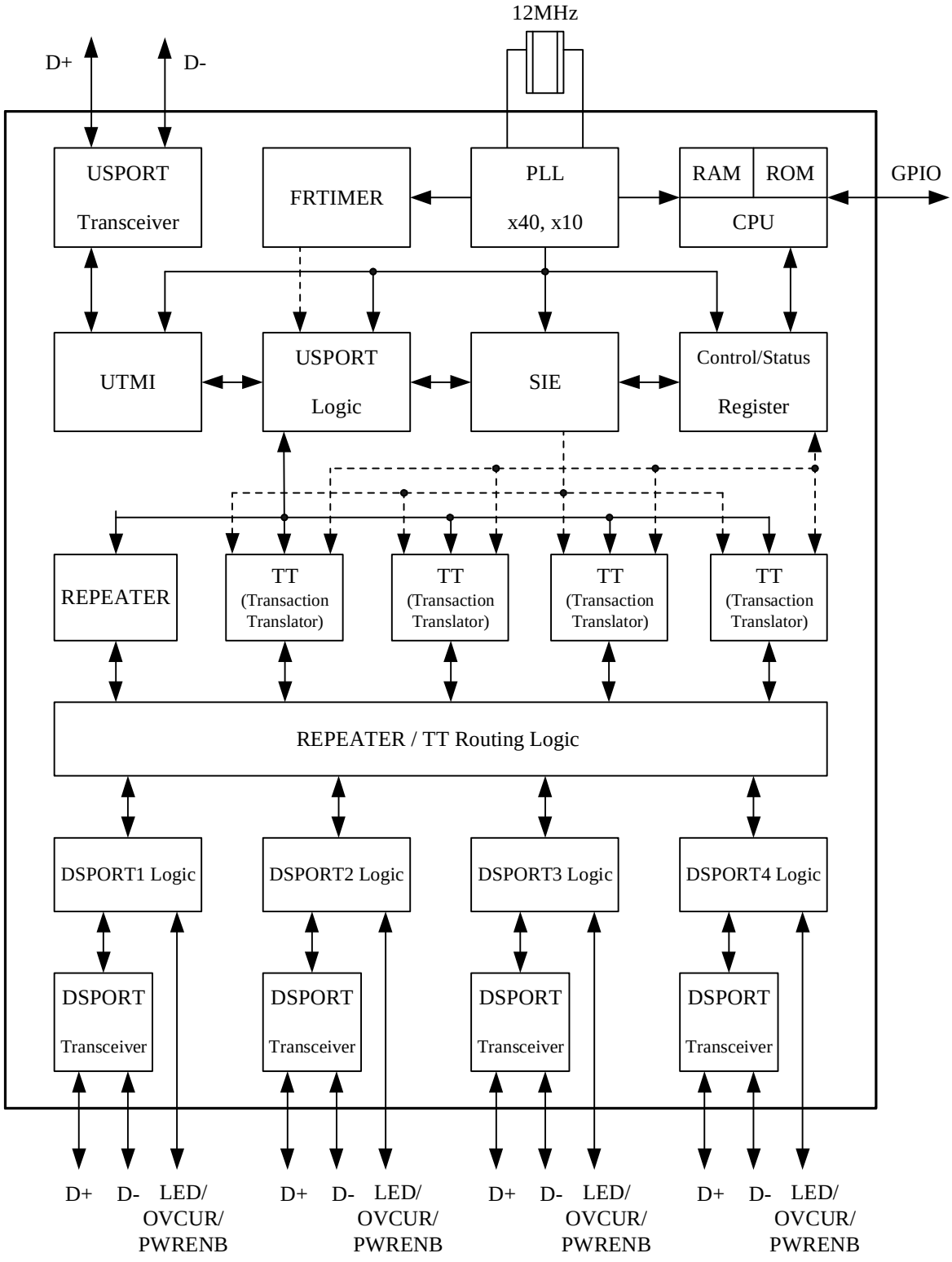


Figure 4.1 - GL852 Block Diagram (multiple TT)

CHAPTER 5 FUNCTION DESCRIPTION

5.1 General

5.1.1 USPORT Transceiver

USPORT (upstream port) transceiver is the analog circuit that supports both full-speed and high-speed electrical characteristics defined in chapter 7 of *USB specification Revision 2.0*. USPORT transceiver will operate in full-speed electrical signaling when GL852 is plugged into a 1.1 host/hub. USPORT transceiver will operate in high-speed electrical signaling when GL852 is plugged into a 2.0 host/hub.

5.1.2 PLL (Phase Lock Loop)

GL852 contains a 40x PLL. PLL generates the clock sources for the whole chip. The generated clocks are proven quite accurate that help in generating high speed signal without jitter.

5.1.3 FRTIMER

This module implements hub (micro)frame timer. The (micro)frame timer is derived from the hub's local clock and is synchronized to the host (micro)frame period by the host generated Start of (micro)frame (SOF). FRTIMER keeps tracking the host's SOF such that GL852 is always safely synchronized to the host. The functionality of FRTIMER is described in section 11.2 of *USB Specification Revision 2.0.*

5.1.4 µC

µC is the micro-processor unit of GL852. It is an 8-bit RISC processor with 2K ROM and 64 bytes RAM. It operates at 6MIPS of 12Mhz clock to decode the USB command issued from host and then prepares the data to respond to the host. In addition, µC can handle GPIO (general purpose I/O) settings and reading content of EEPROM to support high flexibility for customers of different configurations of hub. These configurations include self/bus power mode setting, individual/gang mode setting, downstream port number setting, device removable/non-removable setting, and PID/VID setting.

5.1.5 UTMI (USB 2.0 Transceiver Macrocell Interface)

UTMI handles the low level USB protocol and signaling. It's designed based on the Intel's UTMI specification 1.01. The major functions of UTMI logic are to handle the data and clock recovery, NRZI encoding/decoding, Bit stuffing /de-stuffing, supporting USB 2.0 test modes, and serial/parallel conversion.

5.1.6 USPORT logic

USPORT implements the upstream port logic defined in section 11.6 of *USB specification Revision 2.0*. It mainly manipulates traffics in the upstream direction. The main functions include the state machines of Receiver and Transmitter, interfaces between UTMI and SIE, and traffic control to/from the REPEATER and TT.

5.1.7 SIE (Serial Interface Engine)

SIE handles the USB protocol defined in chapter 8 of *USB specification Revision 2.0*. It co-works with µC to play the role of the hub kernel. The main functions of SIE include the state machine of USB protocol flow, CRC check, PID error check, and timeout check. Unlike USB 1.1, bit stuffing/de-stuffing is implemented in UTMI, not in SIE.

5.1.8 Control/Status register

Control/Status register is the interface register between hardware and firmware. This register contains the information necessary to control endpoint0 and endpoint1 pipelines. Through the firmware based architecture, GL852 possesses higher flexibility to control the USB protocol easily and correctly.

5.1.9 REPEATER

Repeater logic implements the control logic defined in section 11.4 and section 11.7 of *USB specification Revision 2.0.* REPEATER controls the traffic flow when upstream port and downstream port are signaling in the same speed. In addition, REPEATER will generate internal resume signal whenever a wakeup event is issued under the situation that hub is globally suspended.

5.1.10. TT (Transaction Translator)

TT implements the control logic defined in section 11.14 ~ 11.22 of *USB specification Revision 2.0*. TT basically handles the unbalanced traffic speed between the USPORT (operating in HS) and DSPORTS (operating in FS/LS) of hub. GL852 adopts multiple TT architecture to provide the most performance effective solution. Multiple TT provides control logics for each downstream port respectively.

5.1.11 REPEATER/TT routing logic

REPEATER and TT are the major traffic control machines in the USB 2.0 hub. Under situation that USPORT and DSPORT are signaling in the same speed, REPEATER/TT routing logic switches the traffic channel to the REPEATER. Under situation that USPORT is in the high speed signaling and DSPORT is in the full/low speed signaling, REPEATER/TT routing logic switches the traffic channel to the TT.

5.1.11.1 Connected to 1.1 Host/Hub

If an USB 2.0 hub is connected to the downstream port of an USB 1.1 host/hub, it will operate in USB 1.1 mode. For an USB 1.1 hub, both upstream direction traffic and downstream direction traffic are passing through REPEATER. That is, the REPEATER/TT routing logic will route the traffic channel to the REPEATER.

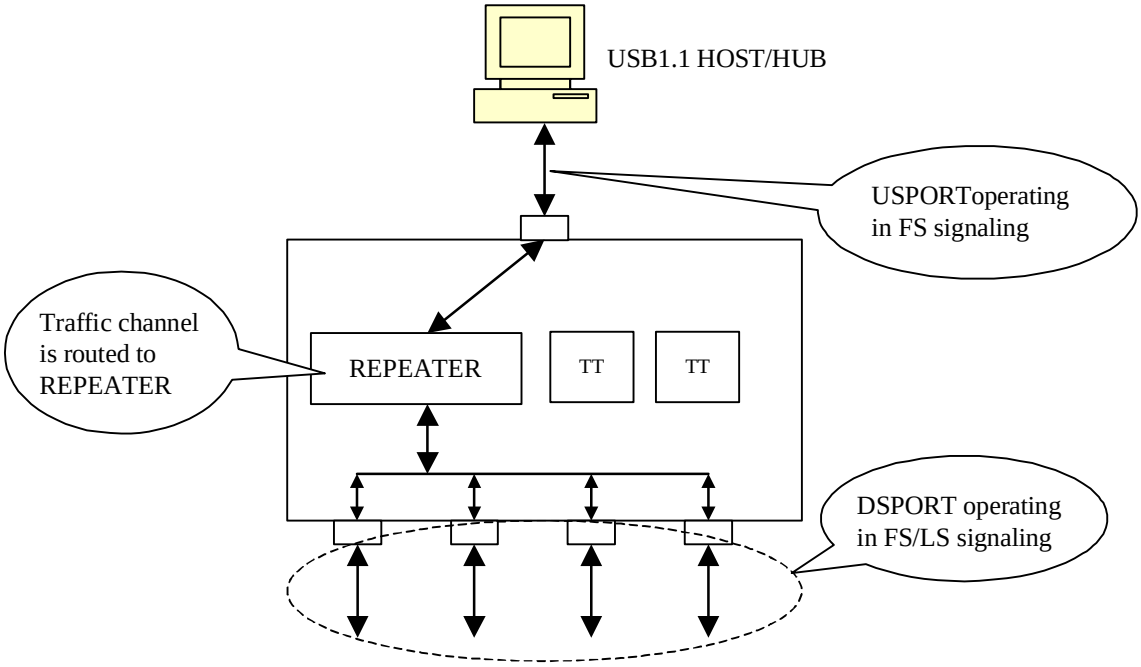


Figure 5.1 - Operating in USB 1.1 scheme

5.1.11.2 Connected to USB 2.0 Host/Hub

If an USB 2.0 hub is connected to an USB 2.0 host/hub, it will operate in USB 2.0 mode. The upstream port signaling is in high speed with bandwidth of 480 Mbps under this environment. The traffic channel will then be routed to the REPEATER when the device connected to the downstream port is signaling also in high speed. On the other hand, the traffic channel will then be routed to TT when the device connected to the downstream port is signaling in full/low speed.

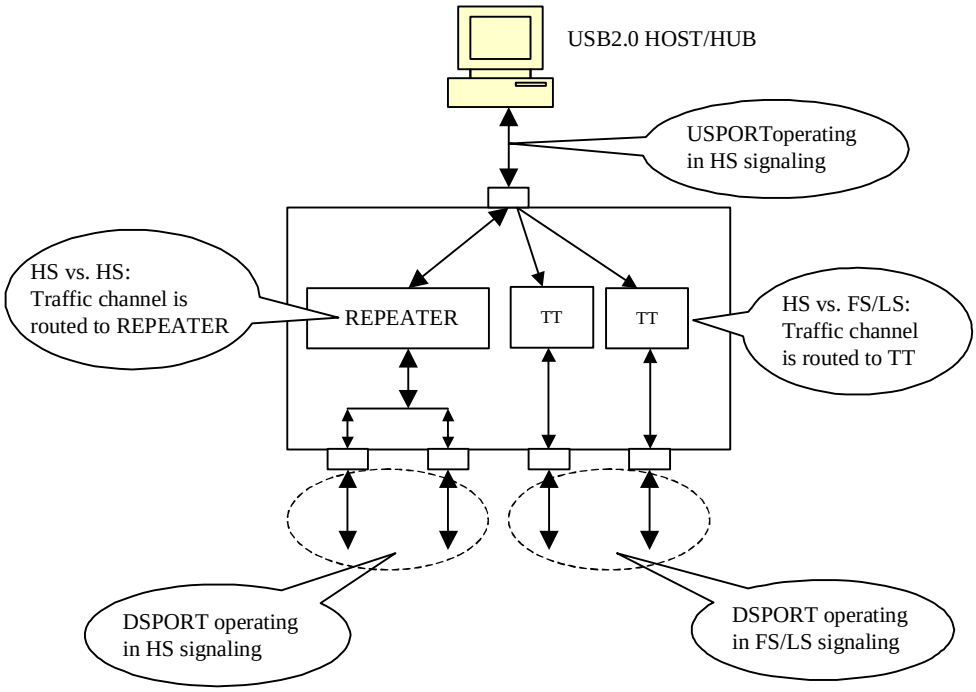


Figure 5.2 - Operating in USB 2.0 scheme

5.12 DSPORT logic

DSPORT (downstream port) logic implements the control logic defined in section 11.5 of *USB specification Revision 2.0*. It mainly manipulates the state machine, the connection/disconnection detection, over current detection and power enable control, and the status LED control of the downstream port. Besides, it also output the control signals to the DSPORT transceiver.

5.13 DSPORT Transceiver

DSPORT transceiver is the analog circuit that supports high-speed, full-speed, and low-speed electrical characteristics defined in chapter 7 of *USB specification Revision 2.0*. In addition, each DSPORT transceiver accurately controls its own squelch level to detect the detachment and attachment of devices.

5.2 Configuration and I/O Settings

5.2.1 RESET# Setting

GL852 integrates in the pull-up 15KΩ resister of the upstream port. When RESET# is enabled, the internal 15KΩ pull-up resister will be disconnected to the 3.3V power. To meet the requirement (p.141) of the USB 2.0 specification, pull-up resister should be disconnected while lacking of USB cable power (Vbus). Therefore, we suggest designing the RESET# circuit as following figure to meet the requirement mentioned above.

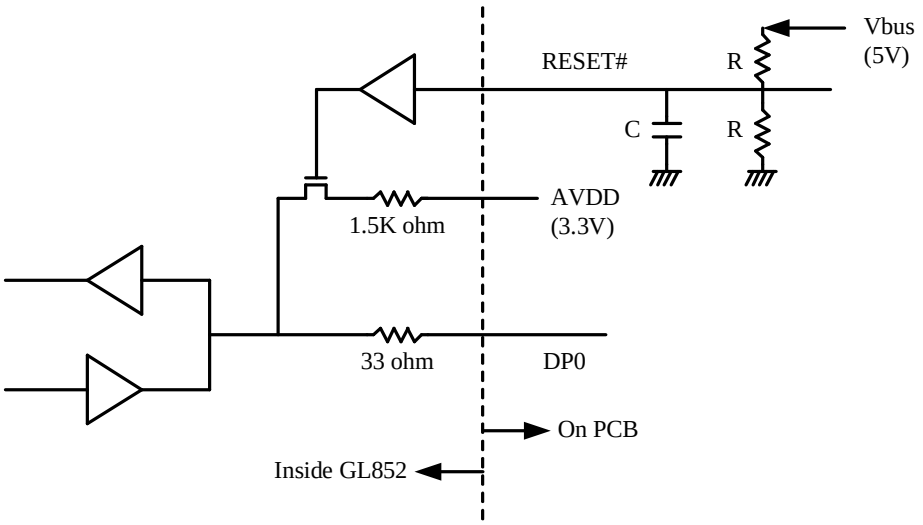


Figure 5.3 - RESET# (External Reset) setting and application

GL852 internally contains a power on reset circuit. The power on sequence is depicted in the next picture. To fully control the reset process of GL852, we suggest the reset time applied in the external reset circuit should longer than that of the internal reset circuit.

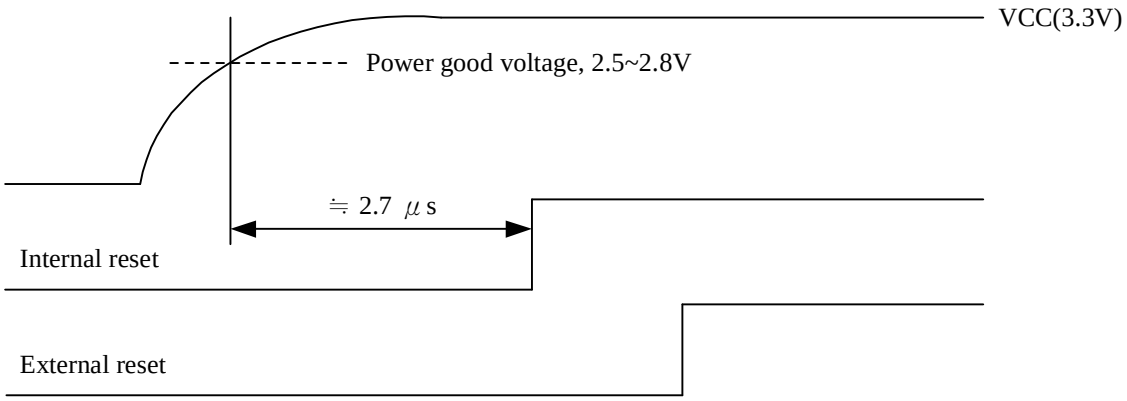


Figure 5.4 - Power on sequence of GL852

5.2.2 PGANG/SUSPND Setting

To save pin count, GL852 uses the same pin to decide individual/gang mode as well as to output the suspend flag. The individual/gang mode is decided in the period of 1ms after power on reset. After that period of time, this pin is changed to output mode. GL852 outputs the suspend flag once it is globally suspended. For individual mode, a pull low resister greater than 100KΩ should be placed. For gang mode, a pull high resister which greater than 100KΩ should be placed. In figure 5.6, we also depict the suspend LED indicator schematics. It should be noticed that the polarity of LED must be followed, otherwise the suspend current will be over than the current limitation (2.5mA).

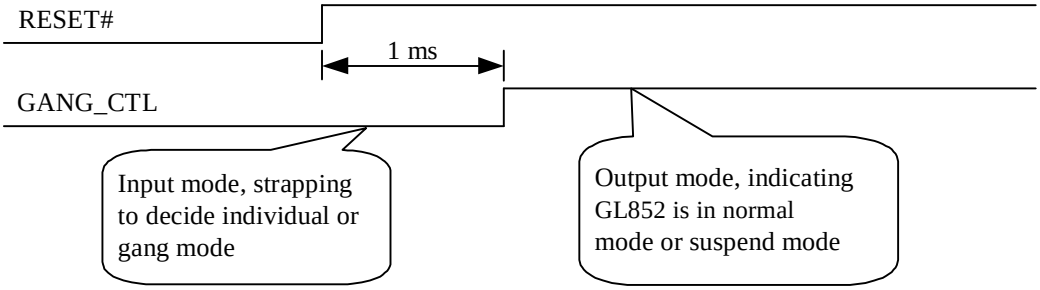


Figure 5.5 - Timing of PGANG/SUSPND strapping

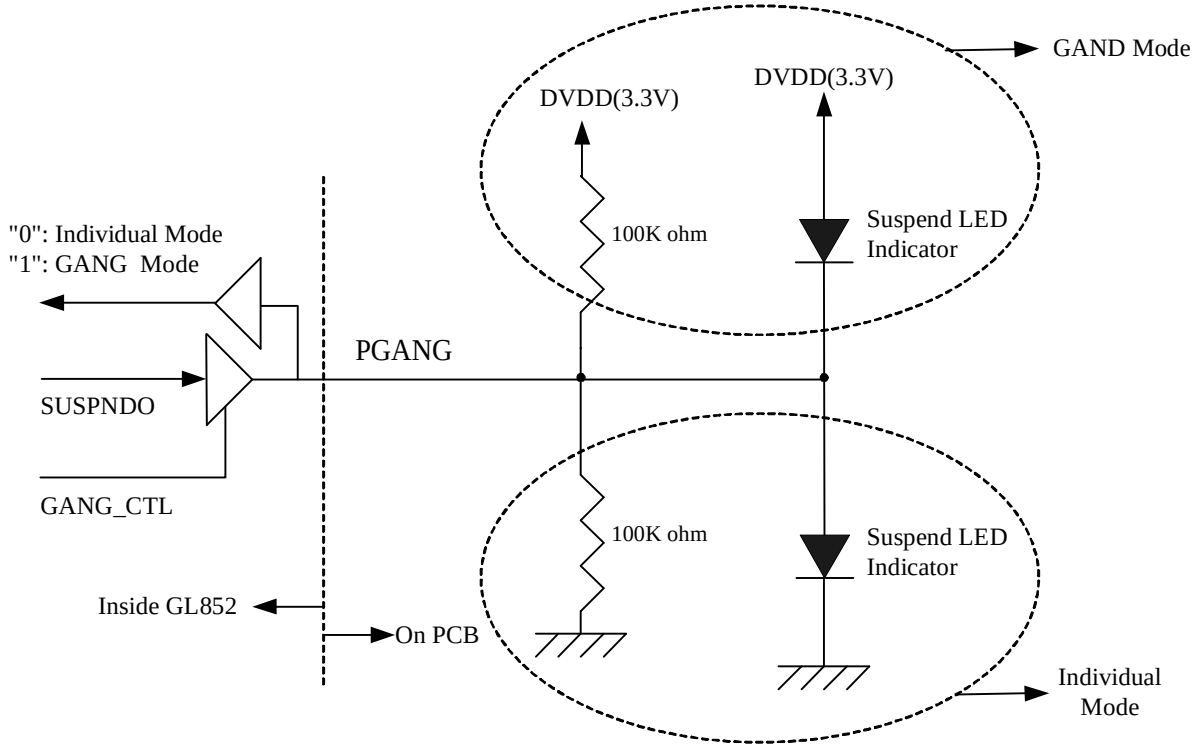


Figure 5.6 - GANG Mode Setting

5.2.3 SELF/BUS Power Setting

GL852 can operate under bus power and conform to the power consumption limitation completely (suspend current < 2.5 mA, normal operation current < 100 mA). By setting PSELF, GL852 can be configured as a bus-power or a self-power hub.

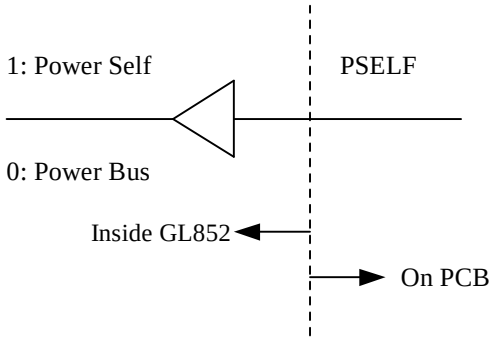


Figure 5.7 - SELF/BUS Power Setting

5.2.4 LED Connections

GL852 controls the LED lighting according to the flow defined in section 11.5.3 of *Universal Serial Bus Specification Revision2.0*. Both manual mode and Automatic mode are supported in GL852. When GL852 is globally suspended, GL852 will turn off the LED to save power.

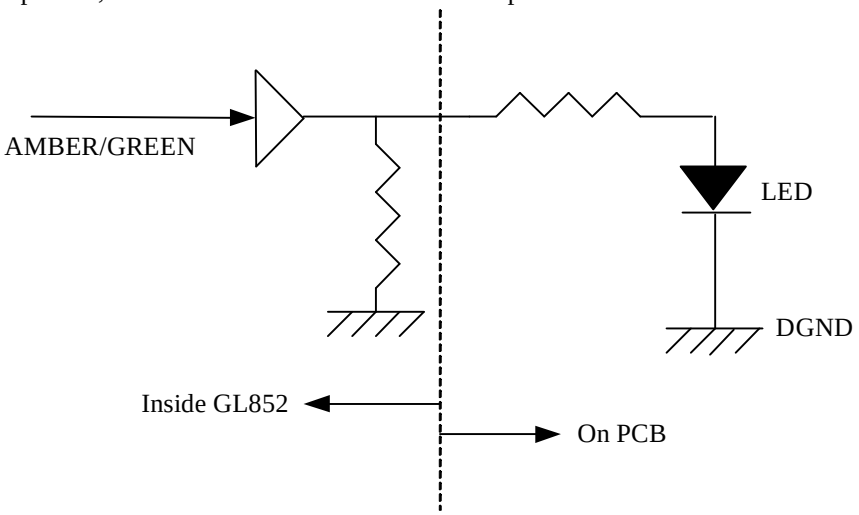


Figure 5.8 - LED Connection

5.2.5 EEPROM Setting

GL852 replies to host commands by the default settings in the internal ROM. GL852 also offers the ability to reply to the host according to the settings in the external EEPROM(93C46). The following table shows the configuration of 93C46.

Table 5.1 - 93C46 Configuration

	00h		01h		02h		03h		04h		05~07h
00	VID_H	VID_L	PID_H	PID_L	CHKSUM	FF	PORT_NO	DEVICE REMOVABLE	FF	MaxPower	FF
08	VENDOR LENGTH	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
10	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
18	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
20	PRODUCT LENGTH	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
28	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
30	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
38	SERIAL NUMBER LENGTH	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
40	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
48	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX

Note: 1. VID_H/VID_L: high/low byte of VID value
2. PID_H/PID_L: high/low byte of PID value
3. CHKSUM: CHKSUM must equal to VID_H + VID_L + PID_H + PID_L + 1,otherwise firmware will ignore the EEPROM settings.
4. PORT_NO: port number, value must be 1~4.
5. DEVICE REMOVALBE:

-	-	-	PORT4 REMOVABLE	PORT3 REMOVABLE	PORT2 REMOVABLE	PORT1 REMOVABLE	-

0: Device attached to this port is removable.
1: Device attached to this port is non-removable.

6. MaxPower: describe the maximum power consumption , range=0mA~500mA
Value **à** 00h~FAh(unit = 2m A)
7. VENDOR LENGTH: offset 08h contains the length of the vendor string. Values of vendor string is contained from 09h~1fh.
8. PRODUCT LENGTH: offset 20h contains the length of product string. Values of product string is contained from 21h~37h.
9. SERIAL NUMBER LENGTH: offset 38h contains the value of serial number string. Values of serial number string is contained after offset 39h.

The schematics between GL852 and 93C46 is depicted in the following figures:

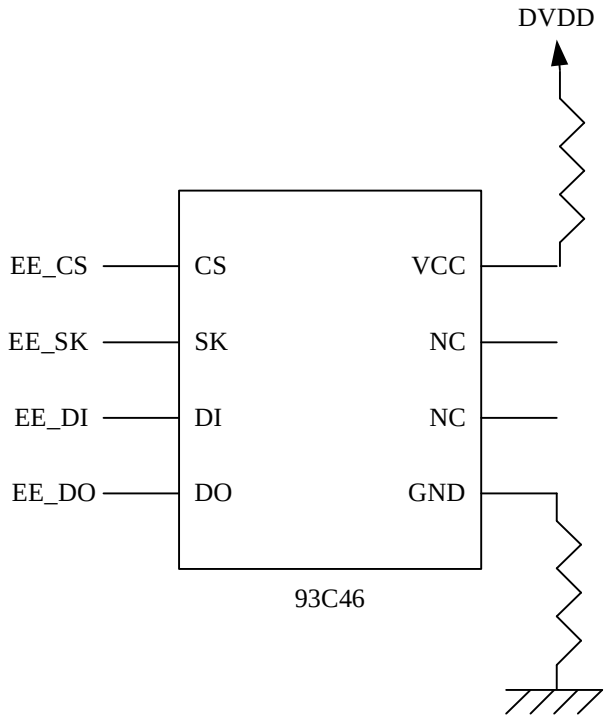


Figure 5.9 - Schematics Between GL852 and 93C46

GL852 firstly verifies the check sum after power on reset. If the check sum is correct, GL852 will take the configuration of 93C46 as part of the descriptor contents. To prevent the content of 93C46 from being over-written, amber LED will be disabled when 93C46 exists.

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Maximum Ratings

Table 6.1 - Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Power Supply	-0.5	+3.6	V
V_{IN}	Input Voltage for digital I/O(EE_DO) pins	-0.5	+3.6	V
V_{IN}	Input Voltage for digital I/O(Ovcur1-4,Pself,Reset) pins	-0.5	+5.25	V
V_{INUSB}	Input Voltage for USB signal (DP, DM) pins	-0.5	+3.6	V
T_S	Storage Temperature under bias	-60	+100	°C
F_{OSC}	Frequency	12 MHz ± 0.005%		

6.2 Operating Ranges

Table 6.2 - Operating Ranges

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply	3.0	3.3	3.6	V
V_{IND}	Input Voltage for digital I/O pins	-0.5	3.3	3.6	V
V_{INUSB}	Input Voltage for USB signal (DP, DM) pins	0.5	3.3	3.6	V
T_A	Ambient Temperature	0	-	70	°C

6.3 DC Characteristics

Table 6.3 - DC Characteristics Except USB Signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
P_D	Power Dissipation	70	-	190	mA
V_{DD}	Power Supply Voltage	3	3.3	3.6	V
V_{IL}	LOW level input voltage	-	-	0.9	V
V_{IH}	HIGH level input voltage	2.0	-	-	V
V_{TLH}	LOW to HIGH threshold voltage	1.36	1.48	1.62	V
V_{THL}	HIGH to LOW threshold voltage	1.36	1.48	1.62	V
V_{OL}	LOW level output voltage when I_{OL}=8mA	-	-	0.4	V
V_{OH}	HIGH level output voltage when I_{OH}=8mA	2.4	-	-	V
I_{OLK}	Leakage current for pads with internal pull up or pull down resistor	-	-	30	µA
R_{DN}	Pad internal pull down resister	81K	103K	181K	Ω
R_{UP}	Pad internal pull up resister	81K	103K	181K	Ω

Table 6.4 - DC Characteristics of USB Signals Under FS/LS Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	DPF/DMF static output LOW(R_L of 1.5K to 3.6V)	0	-	0.3	V
V_{OH}	DPF/DMF static output HIGH (R_L of 15K to GND)	2.8	-	3.6	V
V_{DI}	Differential input sensitivity	0.2	-	-	V
V_{CM}	Differential common mode range	0.8	-	2.5	V
V_{SE}	Single-ended receiver threshold	0.2	-	-	V
C_{IN}	Transceiver capacitance	-	-	20	pF
I_{LO}	Hi-Z state data line leakage	-10	-	+10	µA
Z_{DRV}	Driver output resistance	28	-	43	Ω

Table 6.5 - DC Characteristics of USB Signals Under HS Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	DPH/DMH static output LOW(R_L of 1.5K to 3.6V)	-	-	0.1	V
C_{IN}	Transceiver capacitance	4	4.5	5	pF
I_{LO}	Hi-Z state data line leakage	-5	0	+5	µA
Z_{DRV}	Driver output resistance for USB 2.0 HS	48	45	42	Ω

6.4 Power Consumption

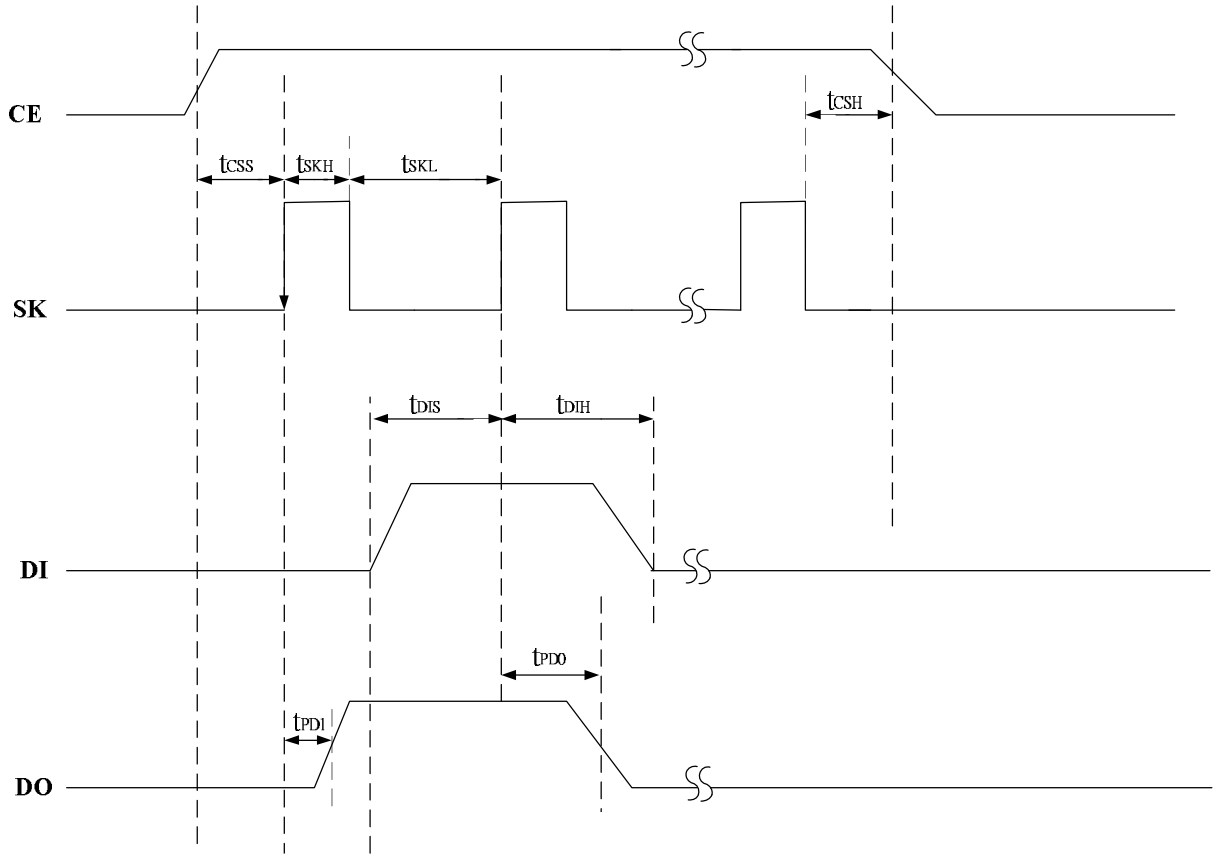
Table 6.6 - DC Supply Current

Symbol	Condition			Typ.	Unit
	Active ports	Host	Device		
I_{SUSP}	Suspend			510/800[*1]	μA
I_{CC}	4	F[*2]	F	83	mA
		H	H	187	mA
		H	F	107	mA
	3	F	F	82	mA
		H	H	170	mA
		H	F	106	mA
	2	F	F	81	mA
		H	H	147	mA
		H	F	105	mA
	1	F	F	79	mA
		H	H	124	mA
		H	F	104	mA
	No Active	F		78	mA
		H		102	mA

*1: 48/64-pin package types

*2: F: Full-Speed, H: High-Speed

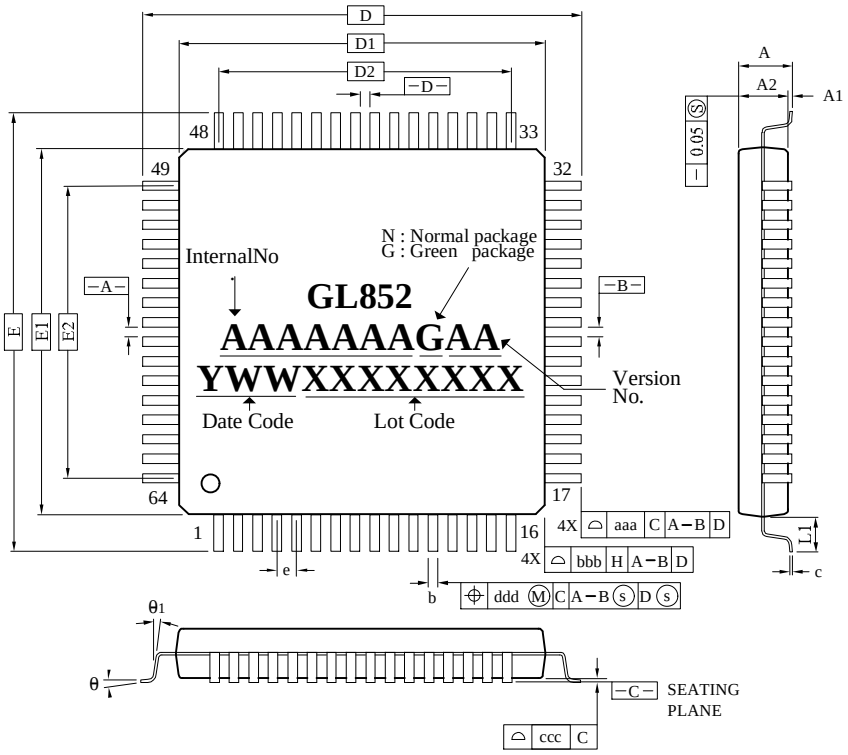
6.5 AC Characteristics

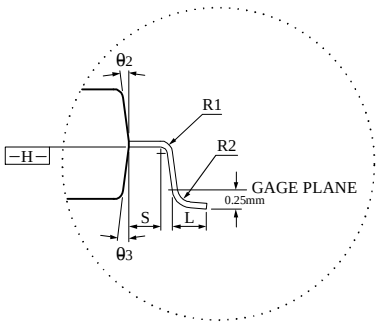


Symbol	Parameter	Min	Typ	Max	Units
t_{CSS}	CS Setup Time	3.0			us
t_{CSH}	CS Hold Time	3.0			
t_{SKH}	SK High Time	1.0			
t_{SKL}	SK Low Time	2.2			
t_{DIS}	DI Setup Time	1.8			
t_{DIH}	DI Hold Time	2.4			
t_{PD1}	Output Delay to “1”			1.8	
t_{PD0}	Output Delay to “0”			1.8	

Table 6.7 - AC Characteristics of EEPROM Interface

CHAPTER 7 PACKAGE DIMENSION





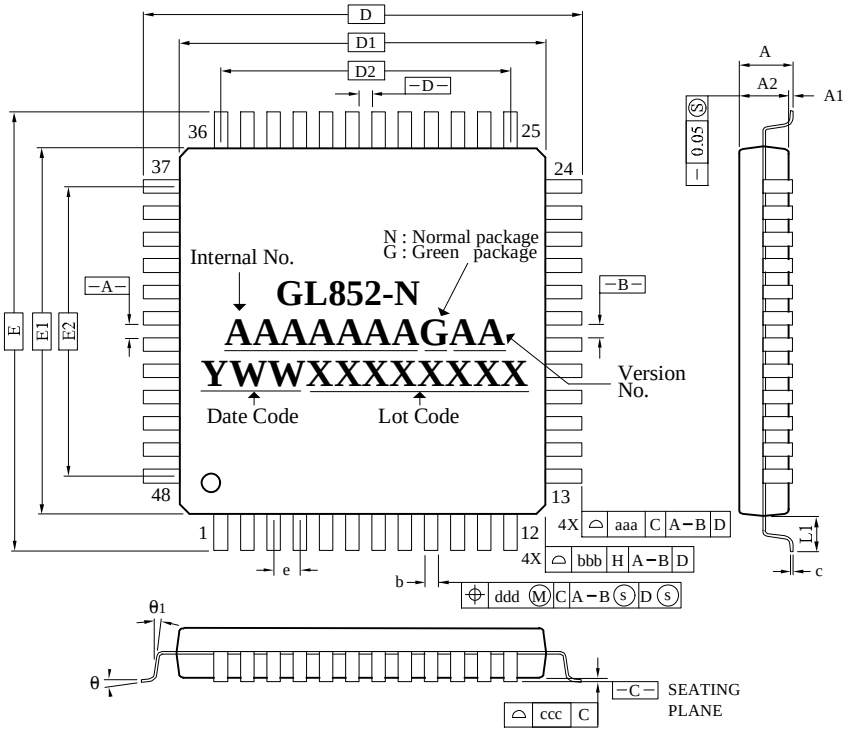
NOTES :

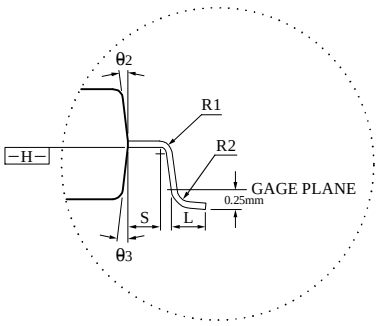
1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	12.00 BASIC			0.472 BASIC		
E	12.00 BASIC			0.472 BASIC		
D1	10.00 BASIC			0.393 BASIC		
E1	10.00 BASIC			0.393 BASIC		
D2	7.50 BASIC			0.295 BASIC		
E2	7.50 BASIC			0.295 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0	3.5	7	0	3.5	7
θ1	0	—	—	0	—	—
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Figure 7.1 - GL852 64 Pin LQFP Package





CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BASIC			0.354 BASIC		
E	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E1	7.00 BASIC			0.276 BASIC		
D2	5.50 BASIC			0.217 BASIC		
E2	5.50 BASIC			0.217 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

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Figure 7.2 – GL852-N 48 Pin LQFP Package

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Normal/Green	Version	Status
GL852-MSNXX	64-pin LQFP	Normal Package	XX	Available
GL852-N-MNNXX	48-pin LQFP	Normal Package	XX	Available
GL852-MSGXX	64-pin LQFP	Green Package	XX	Available
GL852-N-MNGXX	48-pin LQFP	Green Package	XX	Available

