Preliminary

OKI semiconductor

MSM67620/67P620

OKI'S ORIGINAL nX HIGH PERFORMANCE CMOS 16-BIT SINGLE CHIP MICROCONTROLLER

GENERAL DESCRIPTION

MSM67620 is a high-performance 16-bit single-chip microcontroller that employs Oki's original nX-16 CPU core, and integrates memory as well as peripheral functions on-chip. With a minimum instruction execution time of 200 ns (10MHz clock), the MSM67620 is capable of high-speed processing, and includes 16 K words (16 x 16 K) of program memory, 256 words (16 x 256) of data memory, 8-bit timers, 16-bit timers, capture input/compare output, a serial port, and other functions on chip. Also available is the MSM67P620, which replaces the on-chip program memory with one-time PROM.

FEATURES

CPU

- 16-bit CPU using Oki original architecture
- General Register Machine
  Four banks of eight 16-bit registers
- Data Types
  Bit*, byte (8 bits), word (16 bits), double word** (32 bits)
  * Bit operation instructions
  ** Multiplication/division instructions
- High-Speed Data Processing (10 MHz Clock)
  16-bit addition and subtraction 200 ns
  16-bit multiplication 2.3 µs
  32 ÷ 16 bit division 2.3 µs
- 3-Words Instruction Queue
- Highly Orthogonal Instruction Set
- Bit Operation Instructions
- Easy-To-Use I/O Access Instruction
- Address Space
  Program Memory: 64 K words
  Data Memory: 64 K bytes

Peripheral Functions

- 8-bit auto reload timer x 2
- 16-bit auto reload timer x 3
- 4-channel capture input/compare output
- Serial port with 8-bit baud rate generator
  Asynchronous mode/Synchronous mode
- 8-bit parallel port x 7
  Bit-by-bit Input/Output specification

Interrupts

- 3 external interrupts (NMI, INT0, INT1)
- 10 internal interrupt factors
- 4 priority level settings

On-Chip Memory

- 256 words data memory
- 16K words program memory
  Mask ROM --- MSM67620
  One-time PROM --- MSM67P620

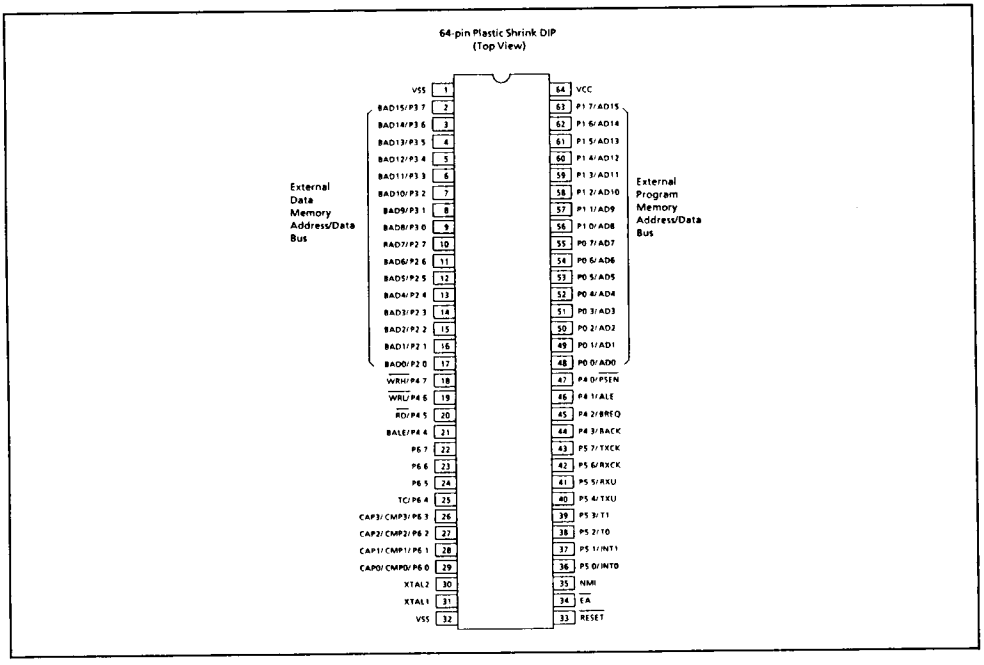
Power Down Modes

- Halt mode
  Terminates instruction execution but peripheral functions keep operating
- Stop mode
  Stop system clock oscillation

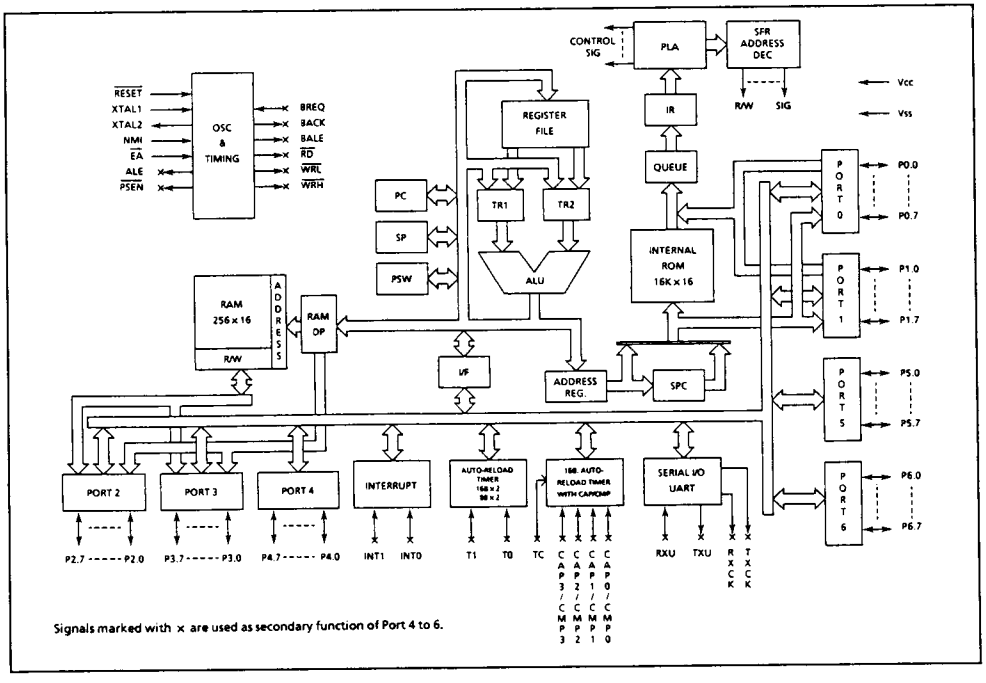
Packages

- 64 pin plastic shrink DIP (SDIP64-P-750)
- 64 pin plastic QFP (T.B.D)
- 68 pin PLCC (QFJ68-P-S950)

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

Type	Pin Name	I/O	Description
Port	P0.0~P0.7 (port 0)	I/O	8-bit bidirectional port that allows bit-by-bit specification for I/O. Secondary function of port 0 is external program memory address/data but.
	P1.0~P1.7 (port 1)	I/O	8-bit bidirectional port that allows bit-by-bit specification for I/O. Secondary function of port 1 is external program memory address/data bus.
	P2.0~P2.7 (port 2)	I/O	8-bit bidirectional port that allows bit-by-bit specification for I/O. Secondary function of port 2 is external data memory address/data bus.
	P3.0~P3.7 (port 3)	I/O	8-bit bidirectional port that allows bit-by-bit specification for I/O. Secondary function of port 3 is external data memory address/data bus.
	P4.0~P4.7 (port 4)	I/O	8-bit bidirectional port that allows bit-by-bit specification for I/O. Secondary functions of port 4 are external address/data bus control signal I/O pins.
	P5.0~P5.7 (port 5)	I/O	8-bit bidirectional port that allows bit-by-bit specification for I/O. Secondary functions of port 5 are on-chip timer clock input pins, serial port I/O pins; external interrupt input pins.
	P6.0~P6.7 (port 6)	I/O	8-bit bidirectional port that allows bit-by-bit specification for I/O. Secondary function of port 6 are capture input/compare output I/O pins.
System Control	$\overline{\text{RESET}}$	Input	System reset input pin. "L" level input performs system reset; pulled up to V_{CC} by resistance.
	$\overline{\text{EA}}$	Input	Program memory select input pin. "L" level input for external program memory; "H" level input for internal program memory. High impedance input.
	XTAL1	Input	System clock input pin. Quartz oscillator or ceramic oscillator is connected between XTAL1 and XTAL2. For external clock, input at XTAL1, leaving XTAL2 open.
	XTAL2	Output	System clock output pin.
Interrupt	NMI	Input	Non-maskable interrupt input pin. High impedance input.
Power Supply	V_{CC}	Input	+ 5V power supply pin.
	V_{SS}	Input	GND pins. Connect both to power supply (0 V).

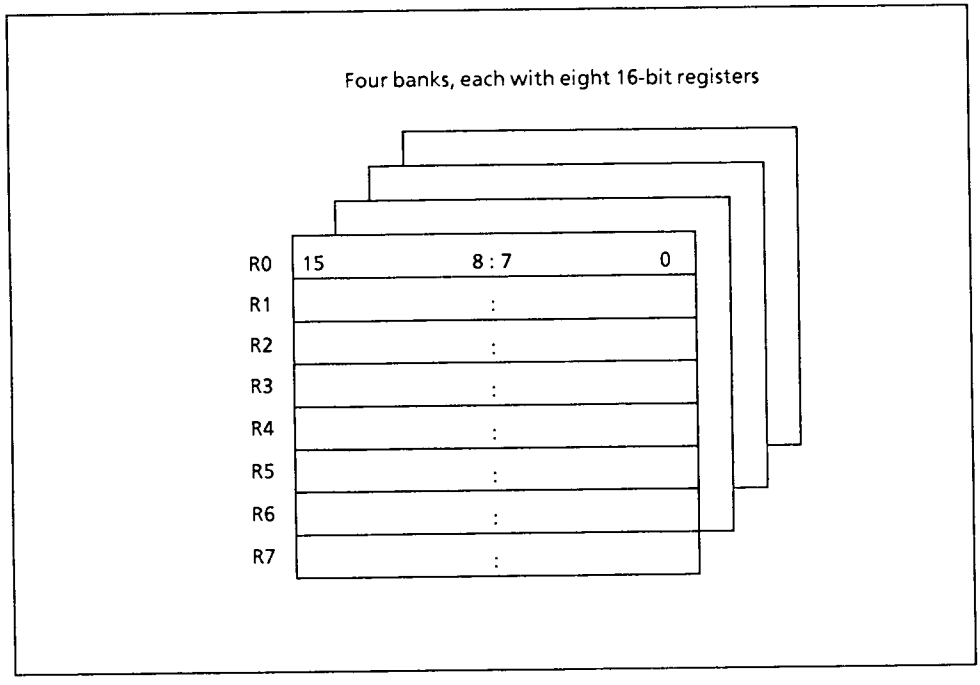
SECONDARY FUNCTIONS OF PORTS

Type	Pin Name	I/O	Description
Bus and Bus Control	AD0~AD7	I/O	Lower 8 bits of external program memory address/data bus. Port 0 secondary function (P0.0 to P0.7).
	AD8~AD15	I/O	Upper 8 bits of external program memory address/data bus. Port 1 secondary function (P1.0 to P1.7).
	$\overline{\text{PSEN}}$	Output	External program memory read strobe output pin; low active output. P4.0 secondary function.
	ALE	Output	External program memory address latch signal output pin. ALE latches address from multiplexed address/data bus AD0 through AD15. P4.1 secondary function.
	BAD0~BAD7	I/O	Lower 8 bits of external data memory address/data bus. Port 2 secondary function (P2.0 to P2.7).
	BAD8~BAD15	I/O	Upper 8 bits of external data memory address/data bus. Port 3 secondary function (3.0 to P3.7).
	BALE	Output	External data memory address latch signal output pin. BALE latches address from multiplexed address/data bus BAD0 through BAD15. P4.4 secondary function.
	$\overline{\text{RD}}$	Output	External data memory read strobe output pin; low active output. P4.5 secondary function.
	$\overline{\text{WRL}}$	Output	External data memory lower byte write strobe output pin; low active output. Secondary function of P4.6.
	$\overline{\text{WRH}}$	Output	External data memory upper byte write strobe output pin; low active output. Secondary function of P4.7.
	BREQ	Input	Bus request input pin. "H" level input opens address/data bus to external device. P4.2 secondary function.
	BACK	Output	Bus acknowledge output pin. High active output that indicates address/data bus is open to external device. P4.3 secondary function.

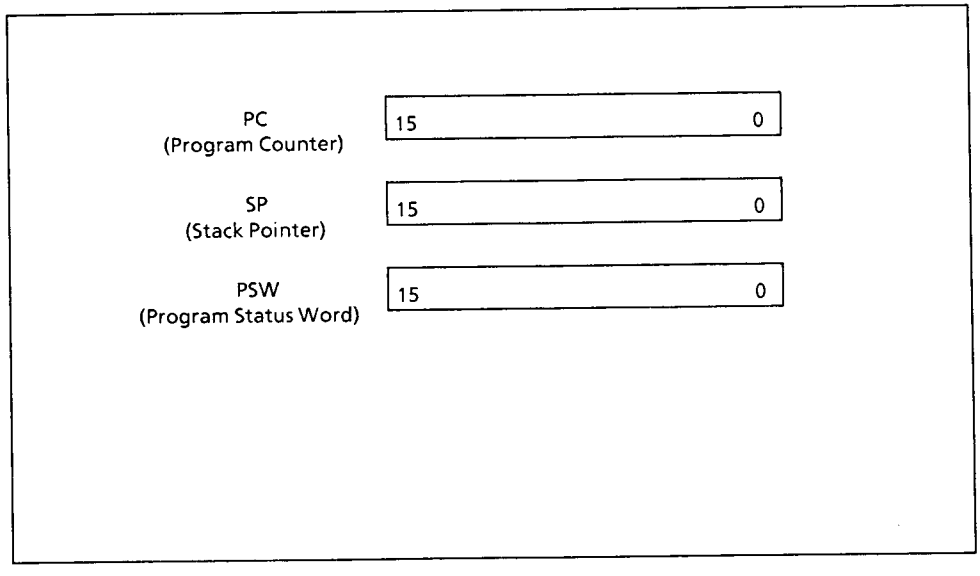
Type	Pin Name	I/O	Description
Interrupt	INT0	Input	External interrupt 0 input pin. P5.0 secondary function.
	INT1	Input	External interrupt 1 input pin. P5.1 secondary function.
Timer	T0	Input	Timer 0 external clock input pin. P5.2 secondary function.
	T1	Input	Timer 1 external clock input pin. P5.3 secondary function.
	TC	Input	Capture timer external clock input pin. P6.4 secondary function.
Serial Port	TXU	Output	Serial port data transmit pin. P5.4 secondary function.
	RXU	Input	Serial port data receive pin. P5.5 secondary function.
	RXCK	Output	Serial port receive synchronizing clock output pin. P5.6 secondary function.
	TXCK	Output	Serial port transmit synchronizing clock output pin. P5.7 secondary function.
Capture Input / Compare Output	CAP0/ CMP0	I/O	Capture input/compare output channel 0 input/output pin. Capture trigger input pin in capture input mode, output pin when compare match is generated in compare output mode. P6.0 secondary function.
	CAP1/ CMP1	I/O	Capture input/compare output channel 1 input/output pin. Capture trigger input pin in capture input mode, output pin when compare match is generated in compare output mode. P6.1 secondary function.
	CAP2/ CMP2	I/O	Capture input/compare output channel 2 input/output pin. Capture trigger input pin in capture input mode, output pin when compare match is generated in compare output mode. P6.2 secondary function.
	CAP3/CMP3	I/O	Capture input/compare output channel 3 input/output pin. Capture trigger input pin in capture input mode, output pin when compare match is generated in compare output mode. P6.3 secondary function.

REGISTERS

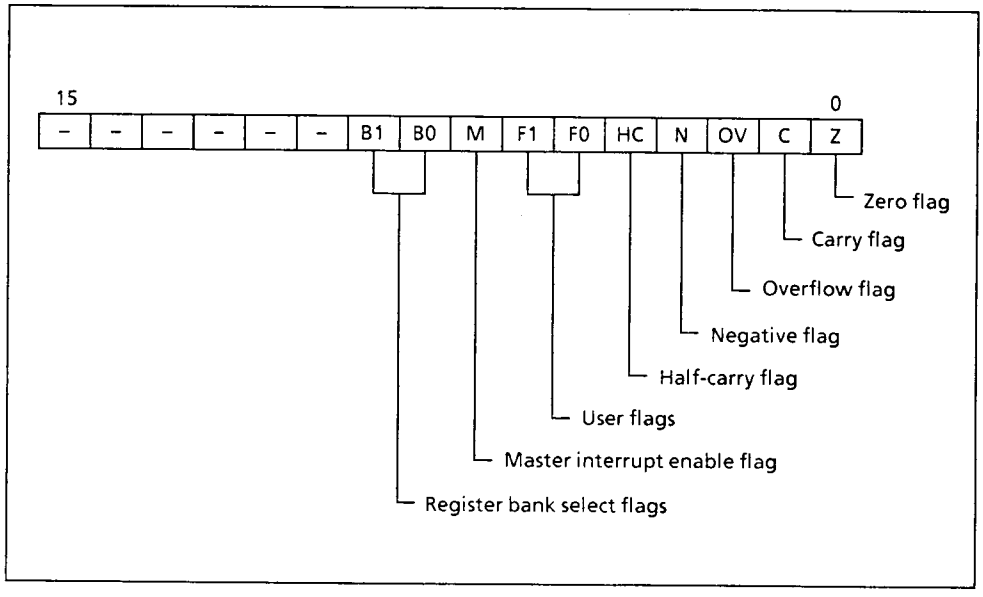
- General Purpose Registers (used as data registers and address registers)



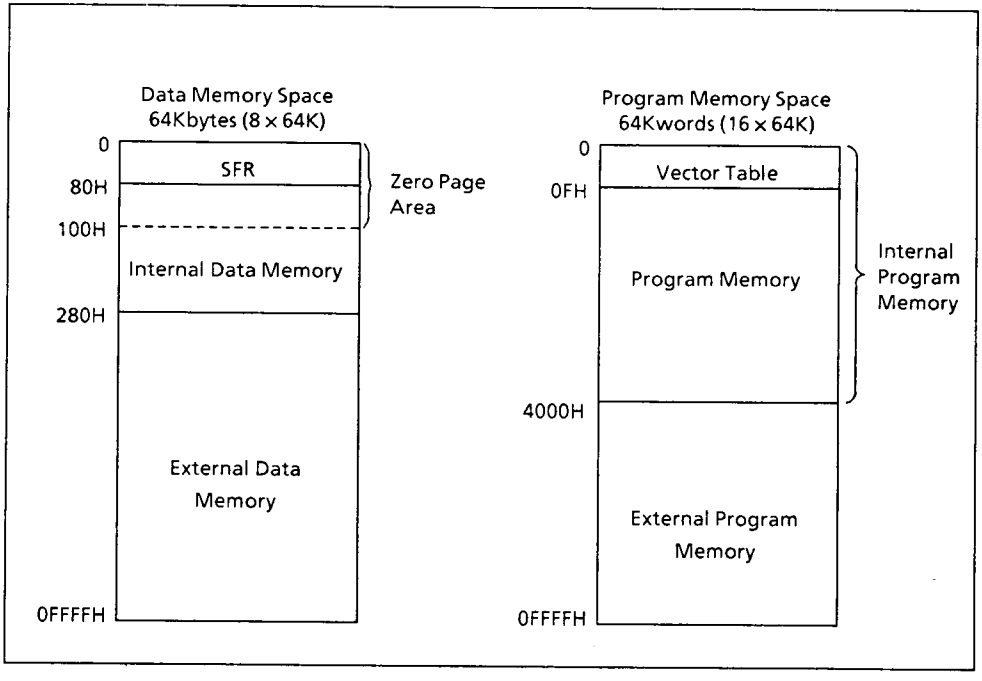
- Special Purpose Registers



• PSW Configuration



MEMORY MAP



SFR TABLE

Address (HEX)	Name	Symbol	Read/ Write	Word/ Byte	Reset
0000	Port 0	P0	R/W	B	undefined
0001	Port 0 direction register	P0DIR			00H
0002	Port 1	P1			undefined
0003	Port 1 direction register	P1DIR			00H
0004	Port 2	P2			undefined
0005	Port 2 direction register	P2DIR			00H
0006	Port 3	P3			undefined
0007	Port 3 direction register	P3DIR			00H
0008	Port 4	P4			0FXH
0009	Port 4 direction register	P4DIR			0F0H
000A	Port 5	P5			undefined
000B	Port 5 direction register	P5DIR			00H
000C	Port 6	P6			undefined
000D	Port 6 direction register	P6DIR			00H
000E	Port 4 mode register	P4MOD			0F3H
000F	Port 5 mode register	P5MOD			00H
0010	Interface control register	IFCON			0BBH
0011	External interrupt control register	XICON			0E0H
0012	Program status word	PSWL		W/B	00H
0013	* PSW during word operation	PSWH			0FCH
0014	Stack pointer	SPL			undefined
0015	* SP during word operation	SPH			undefined
0016	Interrupt priority register	IPL			0FFH
0017	* IP during word operation	IPH			0FFH
0018	Interrupt enable register	IEL			00H
0019	* IE during word operation	IEH			0F0H
001A	In-service priority register	ISPR	R	B	0F0H
001B	Serial port transmit/receive buffer	SBUF	R/W		undefined
001C	Serial port control register	SCON			00H
001D	Serial port status register	SSTAT			0E0H
001E	Baud rate counter	BRC			00H
001F	Baud rate register	BRR			00H
0020	Baud rate control register	BCON			0F0H
0021	Oscillation start control register	OSCON	W		undefined
0022	Timer 0 control register	T0CON	R/W		0E0H
0023	Timer 1 control register	T1CON			0E0H

R/W ; Read/write
R ; Read only
W ; Word only

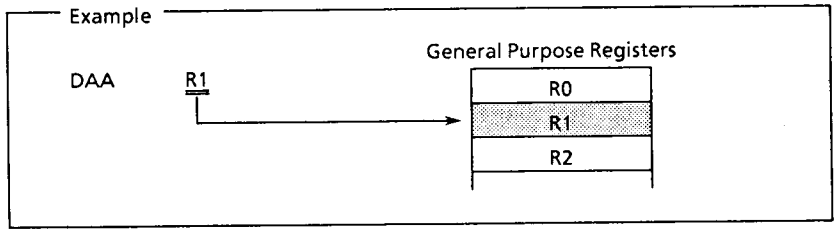
W/B ; Word/byte access
W ; Write access only
B ; Byte access only

Address (HEX)	Name	Symbol	Read/ Write	Word/ Byte	Reset
0024	Timer 2 control register	T2CON	R/W	B	0E2H
0025	Timer 3 control register	T3CON			0E2H
0026	Capture timer control register	CTCON			0E0H
002A	System control register	SYSCON			0F3H
002B	Port 6 mode register	P6MOD			0E0H
0030	Capture control register	CAPCON			00H
0031	Capture interrupt flag register	CAPINT			0F0H
0032	Compare output 0 buffer	CMP0BF	W		0FEH
0033	Compare output 1 buffer	CMP1BF			0FEH
0034	Compare output 2 buffer	CMP2BF			0FEH
0035	Compare output 3 buffer	CMP3BF			0FEH
0060	Capture register 0	CAPR0	R/W	W	0000H
0062	Capture register 1	CAPR1			0000H
0064	Capture register 2	CAPR2			0000H
0066	Capture register 3	CAPR3			0000H
0070	Timer 0 counter	T0C			0000H
0072	Timer 0 register	T0R			0000H
0074	Timer 1 counter	T1C			0000H
0076	Timer 1 register	T1R			0000H
0078	Timer 2 counter	T2C		B	00H
0079	Timer 2 register	T2R			00H
007A	Timer 3 counter	T3C			00H
007B	Timer 3 register	T3R			00H
007C	Capture timer counter	CTC		W	0000H
007E	Capture timer register	CTR			0000H

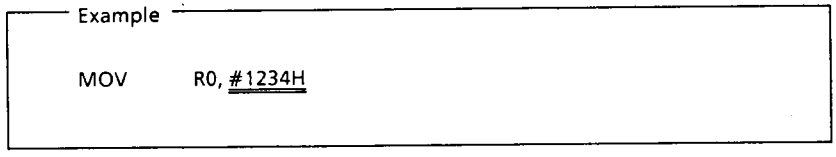
ADDRESSING MODES

MSM67620's instruction set allows use of eight addressing modes.

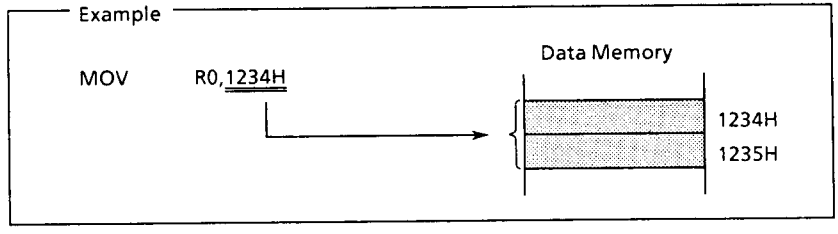
1. Register Direct Addressing Rm



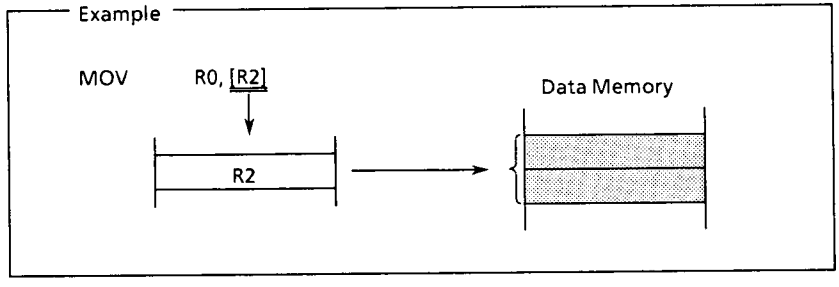
2. Immediate Addressing #n



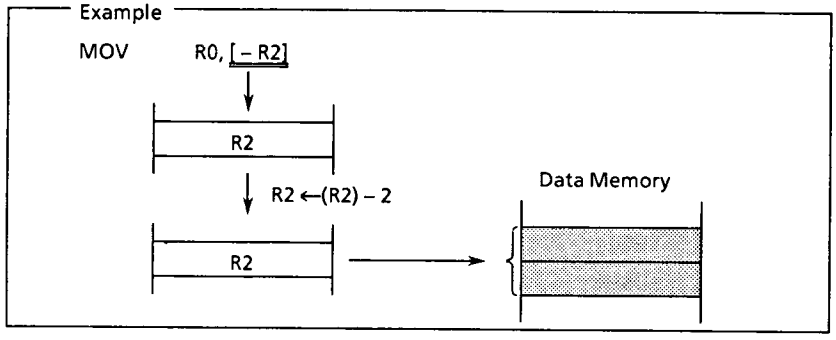
3. Direct Addressing adrs



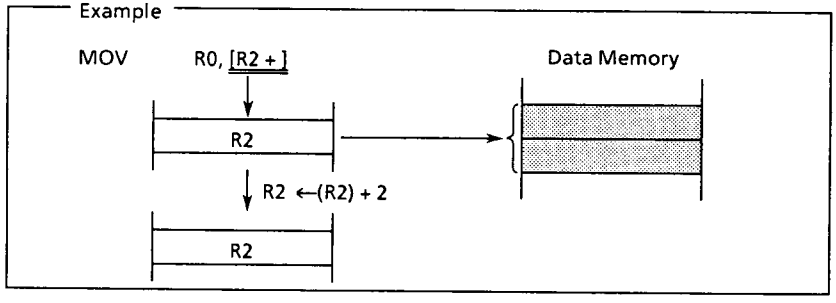
4. Indirect Addressing [Rm]



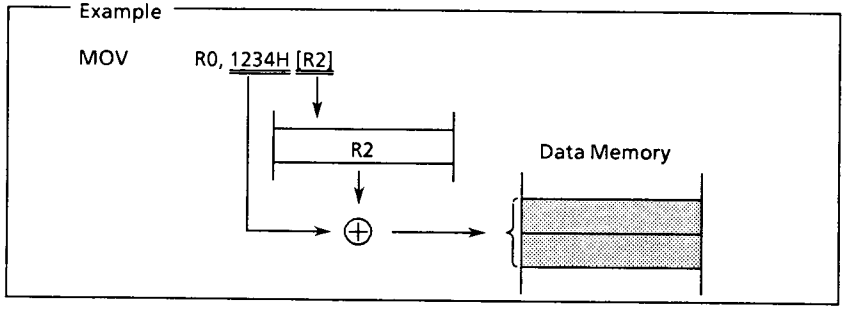
5. Pre-Decrement Addressing [– Rm]



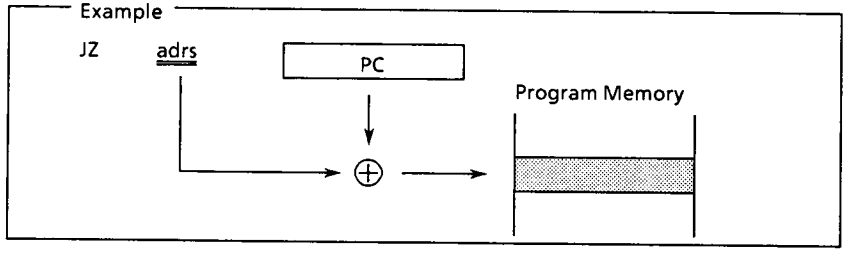
6. Post-Increment Addressing [Rm +]



7. Index Addressing adrs [Rm]



8. PC Relative Addressing adrs



INSTRUCTION TABLE

- Arithmetic Operations

Mnemonic		Function
ADD	ADDB	Data addition
ADDS	ADDSB	Short data addition (#1 to #8 addition)
ADC	ADCB	Data addition with carry
SUB	SUBB	Data subtraction
SUBS	SUBSB	Short data subtraction (#1 to #8 subtraction)
SBC	SBCB	Data subtraction with carry
MUL	MULB	Multiplication
DIV	DIVB	Division
DIVQ		Word quick division (16-bit quotient)
NEG	NEGB	Two's complement
DAA		Register decimal adjust after addition
DAS		Register decimal adjust after subtraction
CMP	CMPB	Comparison
TST	TSTB	Test (comparison with zero)
EXTS		Signed word extension
EXTU		Unsigned word extension

- Logical Operations

Mnemonic		Function
AND	ANDB	Logical AND
ANDZ	ANDZB	Zero page area immediate logical AND
OR	ORB	Logical OR
ORZ	ORZB	Zero page area immediate logical OR
XOR	XORB	Exclusive OR
XORZ	XORZB	Zero page area immediate exclusive OR
NOT	NOTB	Data complement

- Data Transfer Instructions

Mnemonic		Function
MOV	MOVB	Data transfer
MOVS	MOVSB	Short immediate transfer (#1 to #8 transfer)
MOVZ Rm	MOVZB Rm	Zero page area data transfer
MOVZ #n	MOVZB #n	Immediate data transfer to zero page area
MOVR		Data transfer between register banks
MOVC		Code data transfer
XCH		Data swap
SWAP		High byte and low byte swap
CLR	CLRB	Clear

- Rotate and Shift

Mnemonic		Function
ROL	ROLB	Register rotate left
ROR	RORB	Register rotate right
RLC	RLCB	Register and carry flag rotate left
RRC	RRCB	Register and carry flag rotate right
SLL	SLLB	Register shift left
SRL	SRLB	Register shift right
SRA	SRAB	Register shift right arithmetic

- Bit Operations

Mnemonic	Function
BSET	Bit set
BCLR	Bit clear
BNOT	Bit complement
BTST	Bit test
BAND	Carry and bit logical AND
BOR	Carry and bit logical OR
BXOR	Carry and bit exclusive OR
BMOV	Carry and bit transfer
SC	Carry flag set
RC	Carry flag reset
NC	Carry flag complement

- Jumps

Mnemonic	Function
J	Jump
SJ	Short jump
J [Rm]	Indirect jump
JCC	Conditional jump
JB JNB	Zero page area bit condition jump
DJNZ	Decrement register, and jump if not 0

- Subroutines

Mnemonic	Function
PUSH Rm	Register push
PUSH PSW	PSW push
POP Rm	Register pop
POP PSW	PSW pop
CAL	Subroutine call
SCAL	Subroutine short call
CAL [Rm]	Indirect call according to register Rm contents
RET	Return from subroutine
RETI	Return from interrupt
RETNMI	Return from NMI

- CPU Control

Mnemonic	Function
EI	Interrupt enable
DI	Interrupt disable
HALT	Halt (instruction execution halt)
STOP	Stop (clock oscillation stop)
BRK	System reset by software