**ELPAQ** ELPAQ **EMS256K8C**

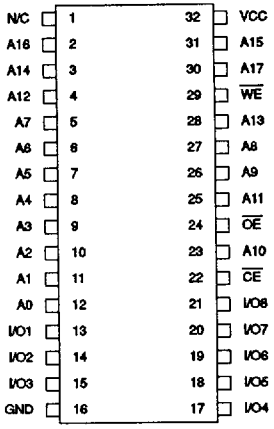
*A division of* **ELMO** *Semiconductor Corp.* ***70 - 100ns***

# 2Mb CMOS STATIC SRAM

## FEATURES

- **High density SRAM module**
- **Organized as 262,144 x 8**
- **Access time 70 - 100ns**
- **Low power consumption**
  Standby: 25µW(typ.)
  Operating: 200mW(typ.)
- **Power supply voltage 5V±10%**
- **TTL compatible inputs and outputs**
- **Fully static operation**
- **32 pin DIP package**
- **JEDEC standard pinout**
- **MIL or commercial temperature range**

## Pin Configuration




## Pin Description

| | |
|---|---|
| **A0 - A17** | Address Inputs |
| **I/O1 - I/O8** | Data Inputs/Outputs |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $\overline{WE}$ | Write Enable |
| VCC | Power Supply |
| GND | Ground |

## GENERAL DESCRIPTION

The ELPAQ EMS256Kx8C is a high performance 2Mb CMOS SRAM module organized as 262,144 bytes of 8 bits each, using two 1Mb SRAMs and a decoder. The EMS256Kx8C is packaged in a 32 lead 600 mil wide ceramic or plastic DIP package. The module is offered in a variety of temperature and speed combinations.

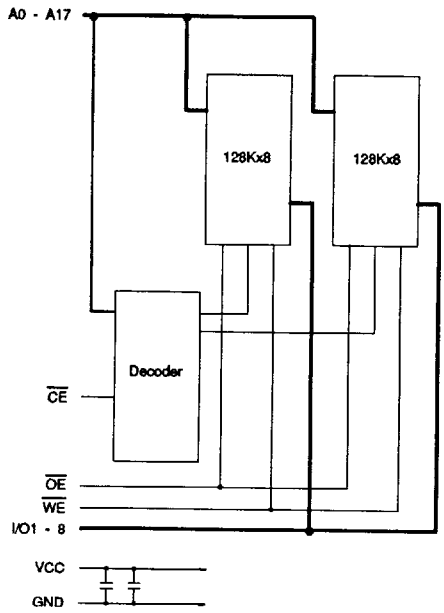
All inputs and outputs are TTL compatible and the module operates from a single 5V power supply. The EMS256Kx8C is a fully asynchronous SRAM and requires no clocks for operation. The module is also available in Low Power and Low Power with Data Retention versions for applications where low current and low stand-by voltages are required.

Writing data to the module is accomplished by bringing the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data present on the eight I/O pins ($I/O_1$ - $I/O_8$) of the device is then written into the memory location specified by the address inputs ($A_0$ - $A_{18}$). Reading data from the device is accomplished by bringing chip enable ($\overline{CE}$) and ($\overline{OE}$) LOW while write enable remains inactive or HIGH. The data in the location specified by the address inputs will the appear on the I/O pins.

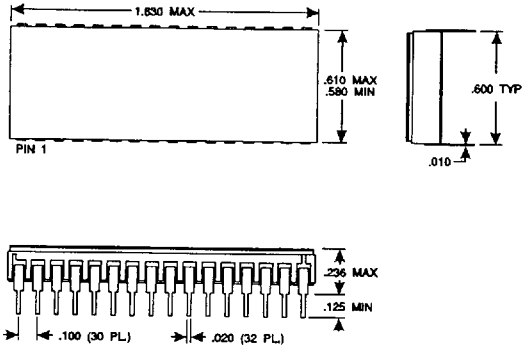
**ELPAQ** ELPAQ **EMS256K8C**

*A division of* **ELMO** *Semiconductor Corp.* ***70 - 100ns***

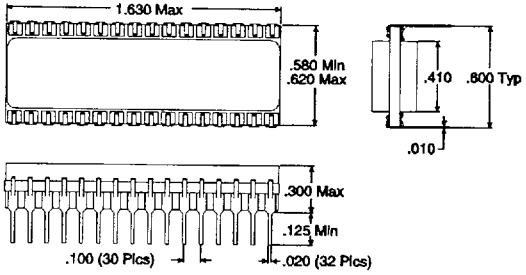
## BLOCK DIAGRAM




## PACKAGE OUTLINE




Package Type MO2, 32 Lead .600" Sidebrazed DIP




Package Type MO6, 32 Lead .600" Plastic DIP

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| **Storage Temperature** | |
| Ceramic Packages | -65°C to +150°C |
| Plastic Packages | -55°C to +125°C |
| **Voltage and Current** | |
| Supply Voltage | -0.5 to +7.0V |
| Input Voltage | -0.5 to Vcc+0.5V |
| Input/Output Voltage | -0.5 to Vcc+0.5V |
| Allowable Power Dissipation | 1W |
| Soldering Temperature*Time | 260°C * 10s |

## OPERATING RANGES

| | |
|---|---|
| **Operating Temperature** | |
| Commercial | 0°C to +70°C |
| Industrial | -40°C to +85°C |
| Military | -55°C to +125°C |
| **Voltage and Current** | |
| Supply Voltage | 4.5 to 5.5V |
| Input High Voltage | 2.2 to Vcc+0.3V |
| Input Low Voltage | -0.3 to 0.8V |

## FUNCTIONAL TRUTH TABLE

| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | Mode | I/O1 - 8 | Vcc Current |
|---|---|---|---|---|---|
| H | X | X | Not Selected | High Z | ISB1, ISB2 |
| L | H | H | Output Disable | High Z | ICC |
| L | L | H | Read | Data Out | ICC |
| L | X | L | Write | Data In | ICC |

## CAPACITANCE (Ta=25°C, f=1MHz)

| Item | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | VIN = 0V | | 15 | 25 | pF |
| Input/Output Capacitance | $C_{I/O}$ | VI/O = 0V | | 20 | 25 | pF |

**Note:** This parameter is sample tested and not 100% tested.

## DC CHARACTERISTICS (Vcc=5V±10%, Ta=Topr)

| Item | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input Leakage Current | IIL | VIN=GND or VCC | -10 | | 10 | μA |
| Output Leakage Current | IOL | VI/O=GND or VCC, $\overline{CE}$=VIH<br>$\overline{OE}$=VIH or $\overline{WE}$=VIL | -10 | | 10 | μA |
| Average Operating Current | ICC | Min. Cycle, Iout=0mA | | 40 | 70 | mA |
| Standby Current | ISB1 | $\overline{CE}$≥VCC-0.2V, VIN≥VCC-0.2V | | 0.005 | 1.5 | mA |
| | ISB2 | $\overline{CE}$=VIH, VIN=VIL or VIH | | 2 | 5 | mA |
| Output High Voltage | VOH | IOH=-1.0mA | 2.4 | | | V |
| Output Low Voltage | VOL | IOL=2.1mA | | | 0.4 | V |

## AC CHARACTERISTICS (Vcc=5V±10%, Ta=Topr)

### AC Test Conditions

| Item | Condition |
|---|---|
| Input Pulse High Level | VIH=3V |
| Input Pulse Low Level | VIL=0V |
| Input Pulse Rise Time | tr=5ns |
| Input Pulse Fall Time | tf=5ns |
| Input and Output Timing Level | 1.5V |
| Output Load | Fig. 1 |

### Output Load

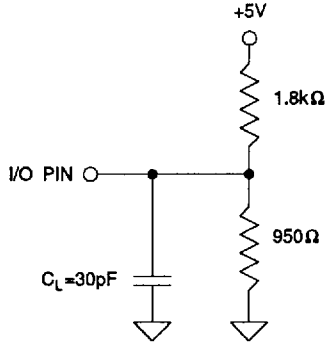



Fig. 1

## Read Cycle

| Item | Symbol | -70 | | -85 | | -100 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Read Cycle Time | TAVAV | 70 | | 85 | | 100 | | ns |
| Address Access Time | TAVQV | | 70 | | 85 | | 100 | ns |
| Chip Enable Access Time | TELQV | | 70 | | 85 | | 100 | ns |
| Output Enable to Output Valid | TGLQV | | 40 | | 45 | | 50 | ns |
| Chip Enable to Output in High Z | TEHQZ | | 30 | | 30 | | 35 | ns |
| Chip Enable to Output in Low Z | TELQX | 15 | | 15 | | 15 | | ns |
| Output Disable to Output in High Z | TGHQZ | | 25 | | 25 | | 35 | ns |
| Output Enable to Output in Low Z | TGLQX | 5 | | 5 | | 5 | | ns |
| Output Hold from Address Change | TAVQX | 10 | | 10 | | | 15 | ns |

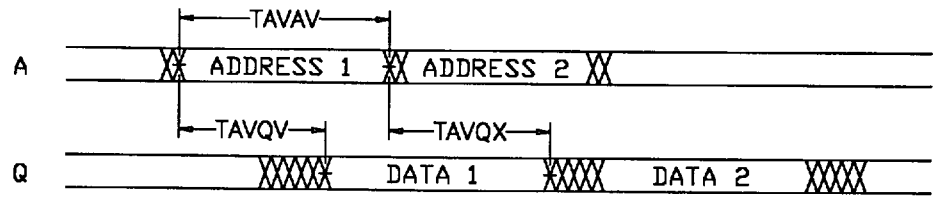
## Write Cycle

| Item | Symbol | -70 | | -85 | | -100 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Write Cycle Time | TAVAV | 70 | | 85 | | 100 | | ns |
| Address Valid to End of Write | TAVWH | 60 | | 75 | | 75 | | ns |
| Chip Enable to End of Write | TELWH | 65 | | 75 | | 75 | | ns |
| | TWLEH | 65 | | 75 | | 75 | | ns |
| Data to Write Time Overlap | TDVWH | 30 | | 30 | | 40 | | ns |
| | TDVEH | 30 | | 30 | | 40 | | ns |
| Data Hold Time from Write | TWHDX | 0 | | 0 | | 0 | | ns |
| | TEHDX | 0 | | 0 | | 0 | | ns |
| Write Pulse Width | TWLWH | 50 | | 60 | | 70 | | ns |
| | TELEH | 50 | | 60 | | 70 | | ns |
| Address Set-up Time | TAVWL | 0 | | 0 | | 0 | | ns |
| | TAVEL | 0 | | 0 | | 0 | | ns |
| Write Recovery Time | TWHAX | 5 | | 5 | | 5 | | ns |
| | TEHAX | 5 | | 5 | | 5 | | ns |
| Write to Output in High Z | TWLQZ | | 25 | | 30 | | 30 | ns |
| Output Active from End of Write | TWHQX | 5 | | 5 | | 10 | | ns |

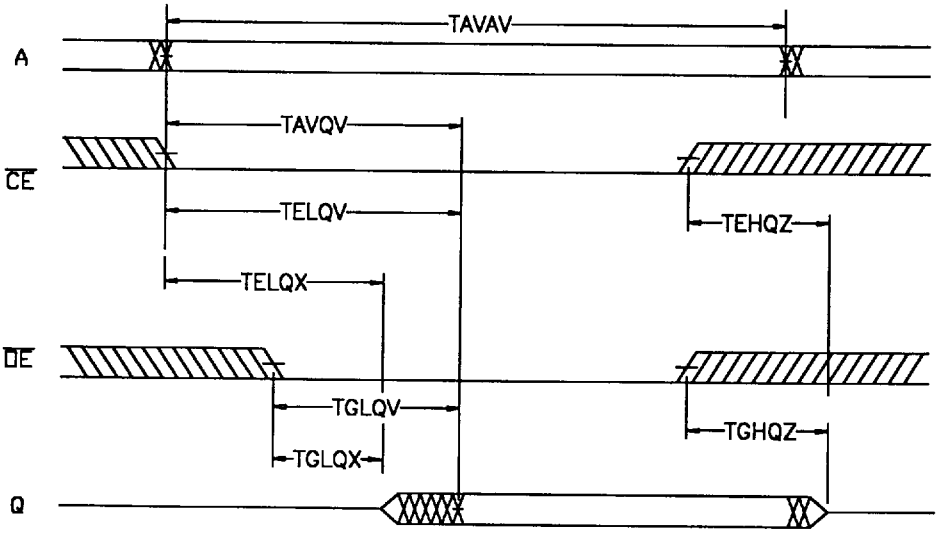
## Timing Diagrams

### Read Cycle Timing

**Read Cycle 1: $\overline{CE}$=$\overline{OE}$=VIL, $\overline{WE}$=VIH**

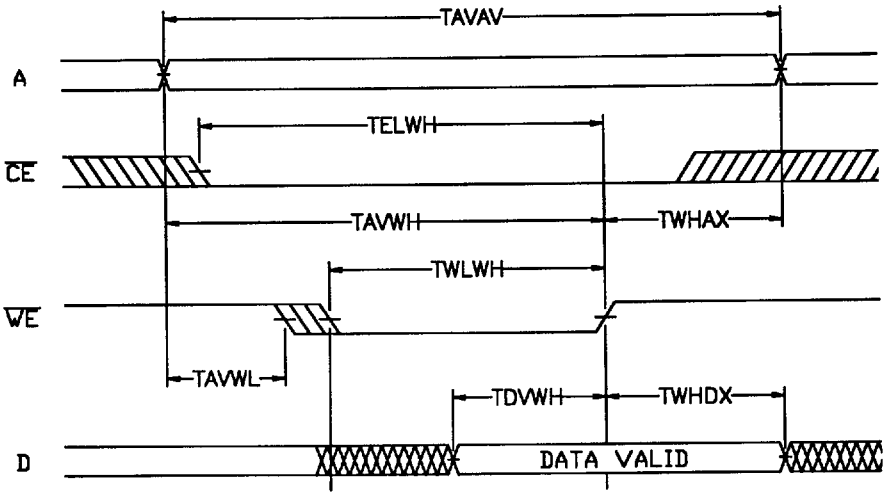



**Read Cycle 2: $\overline{WE}$=VIH**

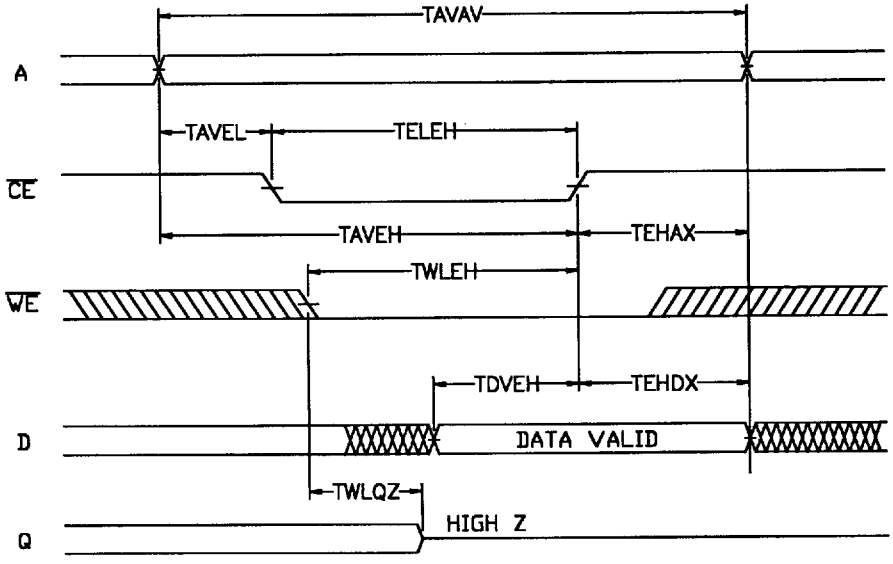


## Write Cycle Timing

### Write Cycle 1: $\overline{WE}$ Control




### Write Cycle 2: $\overline{CE}$ Control



## NOTES:

## ORDERING INFORMATION

**EMS256K8C** *MO2* *-70* *C*

**Temperature Range**

C = Commercial (0 - 70°C)
I = Industrial (-40 - +85°C)
D = MIL Temp (-55 - +125°C)
M = MIL Screen (-55 - +125°C)

**Speed**

-70 = 70ns Access Time
-85 = 85ns Access Time
-100 = 100ns Access Time

**Package**

MO2 = .600" 32 Lead Ceramic DIP
MO6 = .600" 32 Lead Plastic DIP