VME 1210/1220

June 1990

Slot 1 and Non-Slot 1 VMEbus Master Controllers

Distinctive Features

- **VME 1210 provides two device chip set for slot 1 master bus controller and single level arbiter**
- **VME 1220 provides two device chip set for non-slot 1 master bus controller**
- **Integrates 48ma and 64ma VMEbus signals:AS*,DS0*,DS1*,WRITE*,BR*,BBSY***
- **Integrates input hysteresis buffers**
- **Supports Release When Done (RWD) and Release On Request (ROR) protocols**
- **Supports address pipelining, block transfers, and early BBSY* release**
- **Available in Commercial, Industrial and Military temperature ranges**

Programmable Version Available

If the VME 1210/1220 does not match the requirements of the design, a programmable version is available (the PLX 464) which allows the user to customize all inputs, outputs and logic. Programming is performed using industry standard tools such as ABEL™ and CUPL™ software and commonly available PLD programming hardware. Contact PLX for a data sheet on the PLX 464 and other PLX products.

Applications

- VMEbus masters residing in slot 1 boards (VME 1210)
- VMEbus masters residing in non-slot 1 boards (VME 1220)

General Description

The VME 1210: The VME 1210 is comprised of the VME 1210A and the VME 1210B for slot 1 applications. The devices are CMOS and packaged in 24 pin 300 mil wide DIPs or 28 pin J-type LCCs. The VME 1210A provides bus requesting, local arbitration, and single level system arbitration. The VME 1210B functions as the VMEbus controller. The requester initiates a VMEbus request from the local master's bus request for a data or interrupt cycle. The bus controller controls the bus after initiation of a bus cycle and relinquishes the bus at the end of the bus cycle. The bus controller supervises the handshaking between the local master CPU and the slave modules.

The VME 1220: The VME 1220 is comprised of the VME 1220A and the VME 1220B for non-slot 1 applications. The devices are CMOS and packaged in 24 pin 300 mil wide DIPs or 28 pin J-type LCCs. The VME 1220A provides bus requesting and local arbitration. The VME 1220B functions as the VMEbus controller. The requester initiates a VMEbus request from the local master's bus request for a data or interrupt cycle. The bus controller controls the bus after initiation of a bus cycle and relinquishes the bus at the end of the bus cycle. The bus controller supervises the handshaking between the local master CPU and the slave modules.

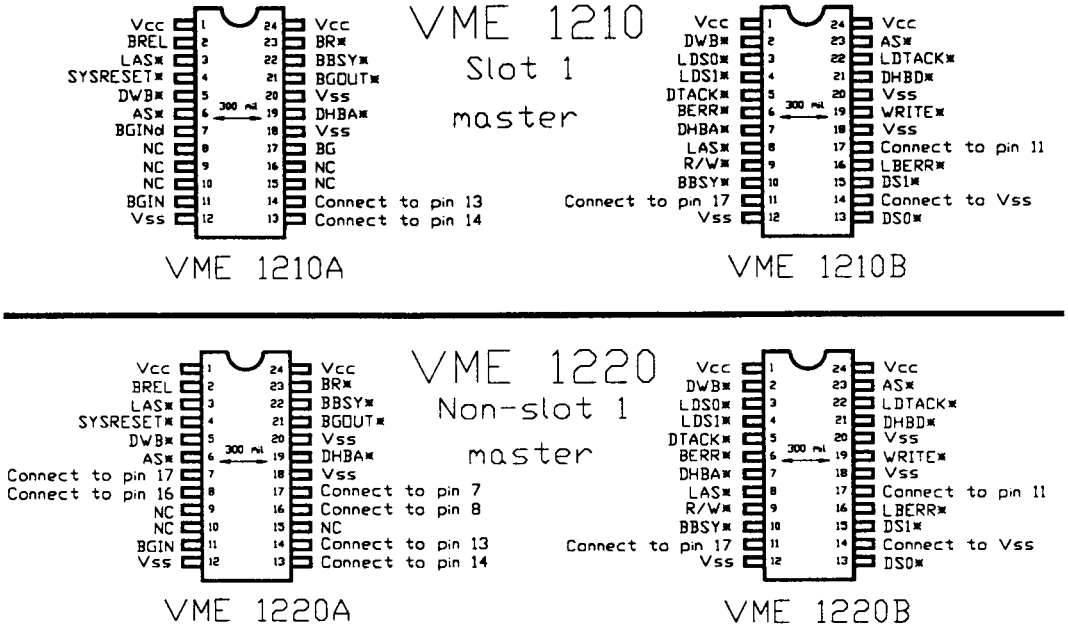

Figure 1. Pinout of VME 1210/1220 (DIPs)

Patent Pending
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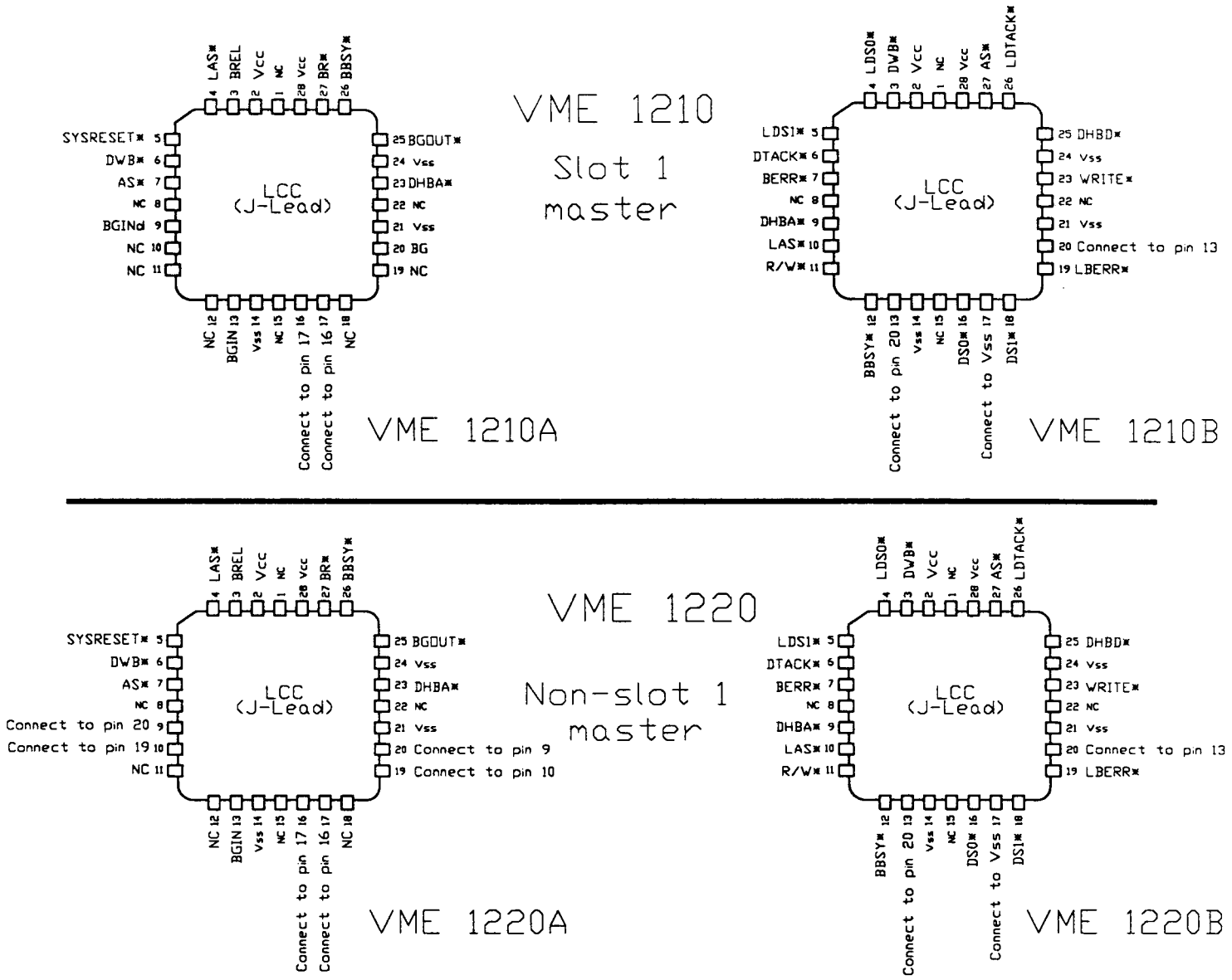


Figure 2. Pinout of VME 1210/1220 (LCCs)

Pin Description

VME 1210A

Pin # LCC	Pin # DIP	Signal	Type	Function
3	2	BREL	I	Active high; Bus release signal indicating BBSY* can be released.
4	3	LAS*	I	Active low; Address strobe from local master.
5	4	SYSRESET*	I	Active low; VMEbus System Reset.
6	5	DWB*	I	Active low; Device wants bus, local master requests control of bus.
7	6	AS*	I	Active low; VMEbus Address Strobe.
9	7	BGINd	I	Active high; Delayed BG output via delay line.
10	8	NC	I	No Connect.
11	9	NC	I	No Connect.
12	10	NC	I	No Connect.
13	11	BGIN	I	Active high; Inverted VMEbus Bus Grant In signal, BGIN*.
14,21, 24	12,18, 20	Vss		Chip Ground
16	13	-	O	Connect to Pin 14 (DIP) or Pin 17 (LCC).
17	14	-	I	Connect to Pin 13 (DIP) or Pin 16 (LCC).
18	15	NC	O	No Connect.
19	16	NC	O	No Connect.
20	17	BG	O	Active high; Bus grant output from arbiter.
23	19	DHBA*	O	Active low; Device has bus address, address buffer enable.
25	21	BGOUT*	O	Active low; VMEbus Bus Grant Out signal.
26	22	BBSY*	I/O	Active low, 48 mA open collector; VMEbus Bus Busy signal.
27	23	BR*	O	Active low, 48 mA open collector; VMEbus Bus Request signal.
2,28	1,24	Vcc		+5 V Chip Power
1,8, 15,22	-	NC	-	No Connect.

Pin Description

VME 1220A

Pin # LCC	Pin # DIP	Signal	Type	Function
3	2	BREL	I	Active high; Bus release signal indicating BBSY* can be released.
4	3	LAS*	I	Active low; Address strobe from local master.
5	4	SYSRESET*	I	Active low; VMEbus System Reset.
6	5	DWB*	I	Active low; Device wants bus, local master requests control of bus.
7	6	AS*	I	Active low; VMEbus Address Strobe.
9	7	-	I	Connect to pin 17 (DIP) or pin 20 (LCC).
10	8	-	I	Connect to pin 16 (DIP) or pin 19 (LCC).
11	9	NC	I	No Connect.
12	10	NC	I	No Connect.
13	11	BGIN	I	Active high; Inverted VMEbus Bus Grant In signal, BGIN*.
14,21, 24	12,18, 20	Vss		Chip Ground.
16	13	-	O	Connect to Pin 14 (DIP) or Pin 17 (LCC).
17	14	-	I	Connect to Pin 13 (DIP) or Pin 16 (LCC).
18	15	NC	O	No Connect.
19	16	-	O	Connect to pin 8 (DIP) or pin 10 (LCC).
20	17	-	O	Connect to pin 7 (DIP) or pin 9 (LCC).
23	19	DHBA*	O	Active low; Device has bus address, address buffer enable.
25	21	BGOUT*	O	Active low; VMEbus Bus Grant Out signal.
26	22	BBSY*	I/O	Active low, 48 mA open collector; VMEbus Bus Busy signal.
27	23	BR*	O	Active low, 48 mA open collector; VMEbus Bus Request signal.
2,28	1,24	Vcc		+5 V Chip Power
1,8, 15,22	-	NC	-	No Connect.

Pin Description

VME 1210B and VME1220B

Pin # LCC	Pin # DIP	Signal	Type	Function
3	2	DWB*	I	Active low; Device wants bus, local master wants control of VMEbus.
4	3	LDS0*	I	Active low; Lower data strobe from local master.
5	4	LDS1*	I	Active low; Upper data strobe from local master.
6	5	DTACK*	I	Active low; VMEbus Data Transfer Acknowledge, data is valid during a read cycle or data has been accepted from the bus during a write cycle.
7	6	BERR*	I	Active low; VMEbus Error signal.
9	7	DHBA*	I	Active low; Device has bus address, address buffer enable.
10	8	LAS*	I	Active low; Address strobe from local master.
11	9	R/W*	I	Active high/low; Read or write cycle from local master.
12	10	BBSY*	I	Active low; VMEbus Busy, local master controls bus.
13	11	-	I	Connect to pin 17 (DIP) or pin 20 (LCC).
14,21, 24	12,18, 20	Vss		Chip Ground.
16	13	DS0*	O	Active low; 64ma VMEbus lower Data Strobe signal, indicates valid data on bus.
17	14	-	I	Connect to Vss.
18	15	DS1*	O	Active low; 64ma VMEbus upper Data Strobe signal, indicates valid data on bus.
19	16	LBERR*	O	Active low; Open collector signal, bus error to local master.
20	17	-	O	Connect to pin 11 (DIP) or pin 13 (LCC).
23	19	WRITE*	O	Active low; 48ma VMEbus Write signal, indicates bus read or write cycle.
25	21	DHBD*	O	Active low; Device has bus data, data buffer enable.
26	22	LDTACK*	O	Active low; Open collector signal, data acknowledge to local master.
27	23	AS*	O	Active low; 64mA VMEbus Address Strobe signal, indicates valid address on bus.
2,28	1,24	Vcc		+5 V Chip Power
1,8, 15,22	-	NC	-	No Connect.

Detailed Description

The VME 1210/1220 initiates, executes, and terminates VMEbus data transfer cycles. The VME 1210 integrates a single level system arbiter to function as a slot 1 master. The VME 1220 handles local bus arbitration to function as a non-slot 1 master. The following section describes how the VME 1210/1220 performs in a data transfer cycle.

Initiating a Bus Request

The local master (CPU, DMA controller, or interrupt handler for example) can initiate a bus request by asserting DWB* and LAS*. After receiving DWB* and LAS* asserted, the VME 1210/1220 will drive BR* (VMEbus request signal) low provided that the VME 1210/1220 itself is not driving BBSY* low. Note that BR* may be connected to any arbitration level (0-3).

Arbitration

The VME 1210 integrates a single level system arbiter. The arbiter monitors the local master's bus request or other master's bus requests via BR*. If the bus is free, BBSY* is high, the arbiter will assert a bus grant, BG, which is connected to the BGIN input of the local arbiter. The VME 1210 suppresses the BBSY* glitch.

If the user implements the non-slot 1 VME 1220, the VME 1220A daisy chains the VMEbus grants. The daisy chained BGIN* from the adjacent master must be inverted and connected to the BGIN input of the VME 1220A's local arbiter. The local arbiters of both the VME 1210A and VME 1220A function in the same manner.

After the VME 1210 asserts BGIN, or receives BGIN from the daisy chain in the case of the VME 1220, the local arbiter portion of the modules arbitrates between DWB* and BGIN. If DWB* wins the arbitration (i.e. DWB* occurs before BGIN) then the VME 1210/1220 will drive BBSY* low, signifying that the local master has won and now controls the bus. If, however, BGIN wins the arbitration, then the VME 1210/1220 will drive BGOUT*, which passes the bus grant down the daisy chain to the adjacent master in the system.

The VME 1210A/20A delay samples the asynchronous inputs, BGIN and DWB*. The VME 1210A requires an external delay line for the synchronization between the output of BG and the input of BGINd. This delay line is also used to meet the 90ns minimum assertion time required for BBSY*. The VME 1220A does not require an external delay line under some conditions since the time delay is integrated internally (see note in Timing Specifications).

Data Transfer

The local master does not access the bus until the previous master has relinquished control of the bus. This occurs when AS*, DTACK* and BERR* are deasserted. The bus controller function of the VME 1210/1220 then controls the proper sequencing of the address and data buffer enable signals and strobe signals. The VME 1210/1220 ensures that the VMEbus minimum address and data set up times of 35ns are met. DSO* and DS1* are not asserted until both the data buffer enable signal, DHBD*, and the address strobe, AS*, are active.

Two separate address and data enable signals are used to support address pipelining. The VME protocol provides for strobing of address and data separately to improve data transfer rates. The master can broadcast the address of the next cycle while the data transfer of the current cycle is occurring. Under these conditions, DHBA* is enable as soon as AS* is disabled. The address for the next cycle can be broadcast while DTACK* and DSn* are still low from the current data cycle. When DTACK* goes high, signifying the end of the current data cycle, DHBD* enables the data buffers for the next data cycle.

For block transfer cycles, the VME 1210/1220 holds AS* low and the data strobes, DSO* and DS1*, and DTACK* will strobe after every read or write. The block move cycle will continue as long as DWB*, LAS* and AS* are active.

For a Read-Modify-Write cycle, AS* will be kept low for two data cycles, a read cycle followed by a write cycle. Again, the cycle will be negated through DWB*, LAS* and AS* de-assertion.

WRITE* is latched during block moves and address pipelining to hold its level. WRITE* meets the VMEbus minimum hold time of 10ns.

Bus Release

The VME 1210/1220 supports release when done (RWD), release on request (ROR), and early BBSY* release protocols via the bus release signal, BREL.

For RWD operation, BREL will be held low during the data transfer cycle. At the end of the cycle, when the local master wants to release the bus, BREL is asserted thus releasing BBSY*.

For ROR operation, the external release on bus request logic can be tied to BREL. An external bus request will assert BREL to release BBSY* at the end of the current data transfer. If no bus requests are pending, then BREL can be kept de-asserted and the local master can maintain BBSY* low to perform continuous VMEbus data transfer cycles.

For early BBSY* release operation, BREL is asserted always. BBSY* will be negated immediately after BGIN is negated by the system arbiter. This allows for overlapping of the next bus arbitration with the current VMEbus data transfer.

With address pipelining and continual single cycling, BREL must be held de-asserted until the final data transfer. BREL can be asserted anytime after the local master asserts LAS* for the last data transfer.

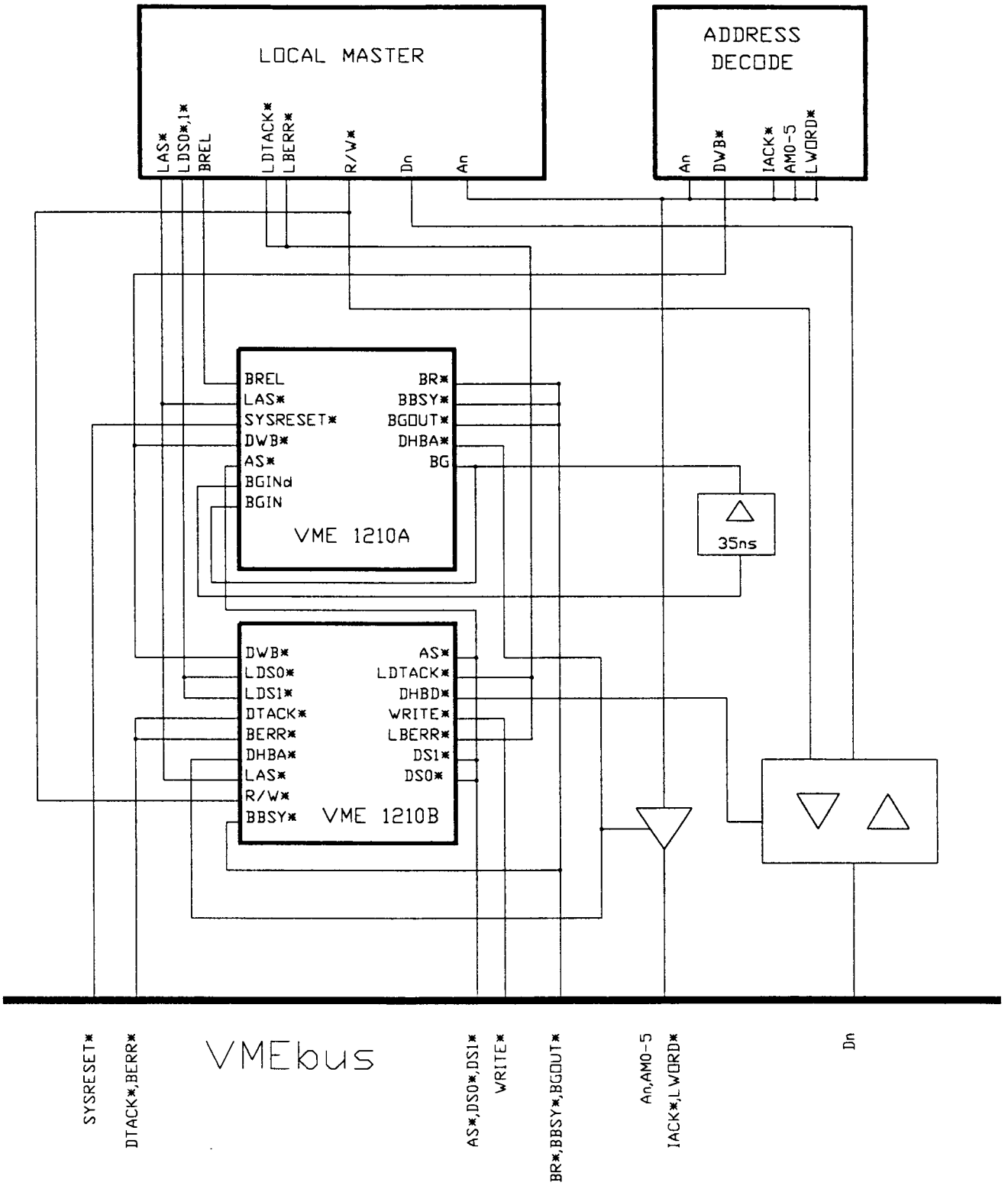


Figure 3. VME 1210 Configuration (Slot 1 master)

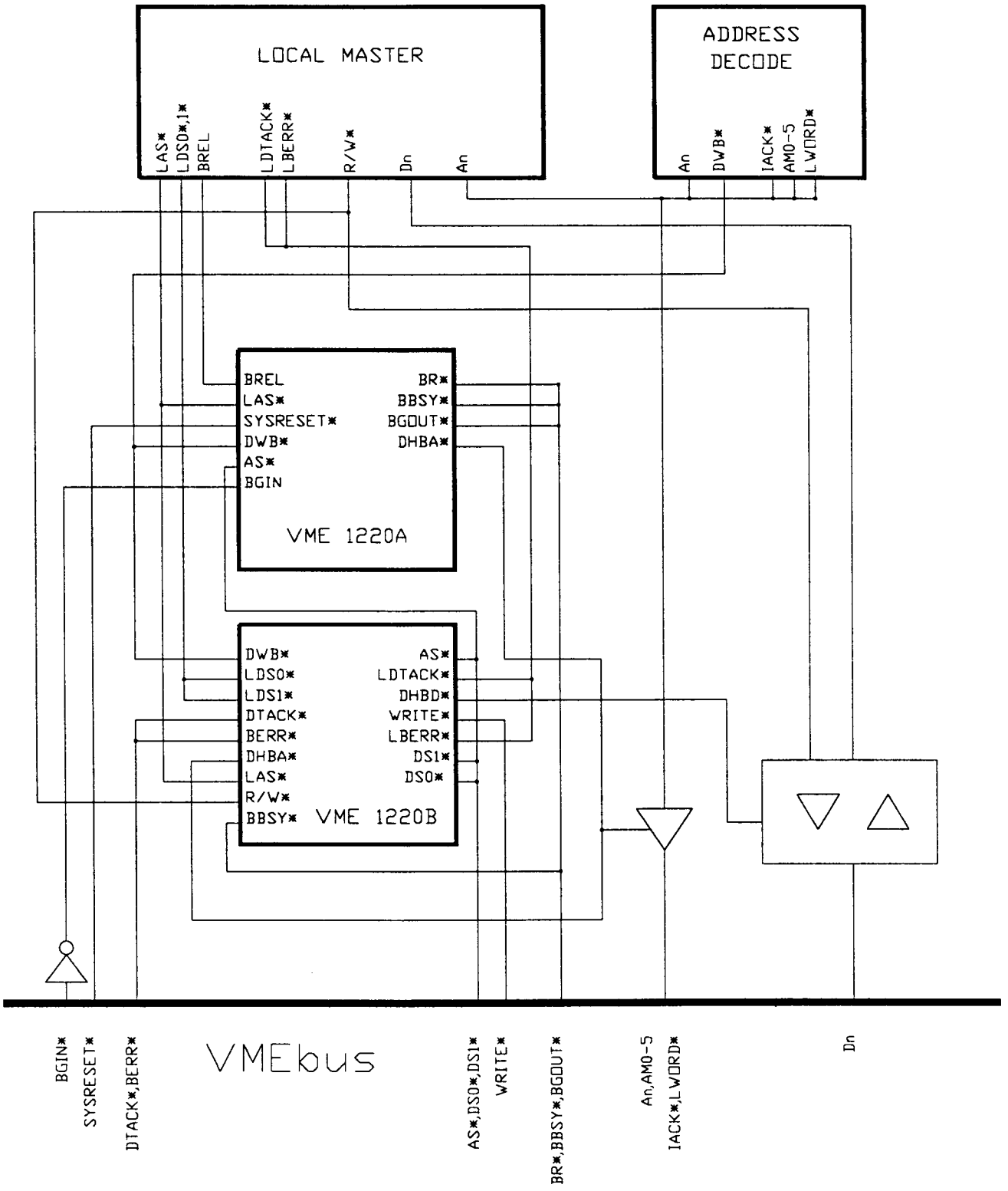


Figure 4. VME 1220 Configuration (Non-slot 1 master)

VME 1210/1220 Timing Waveforms

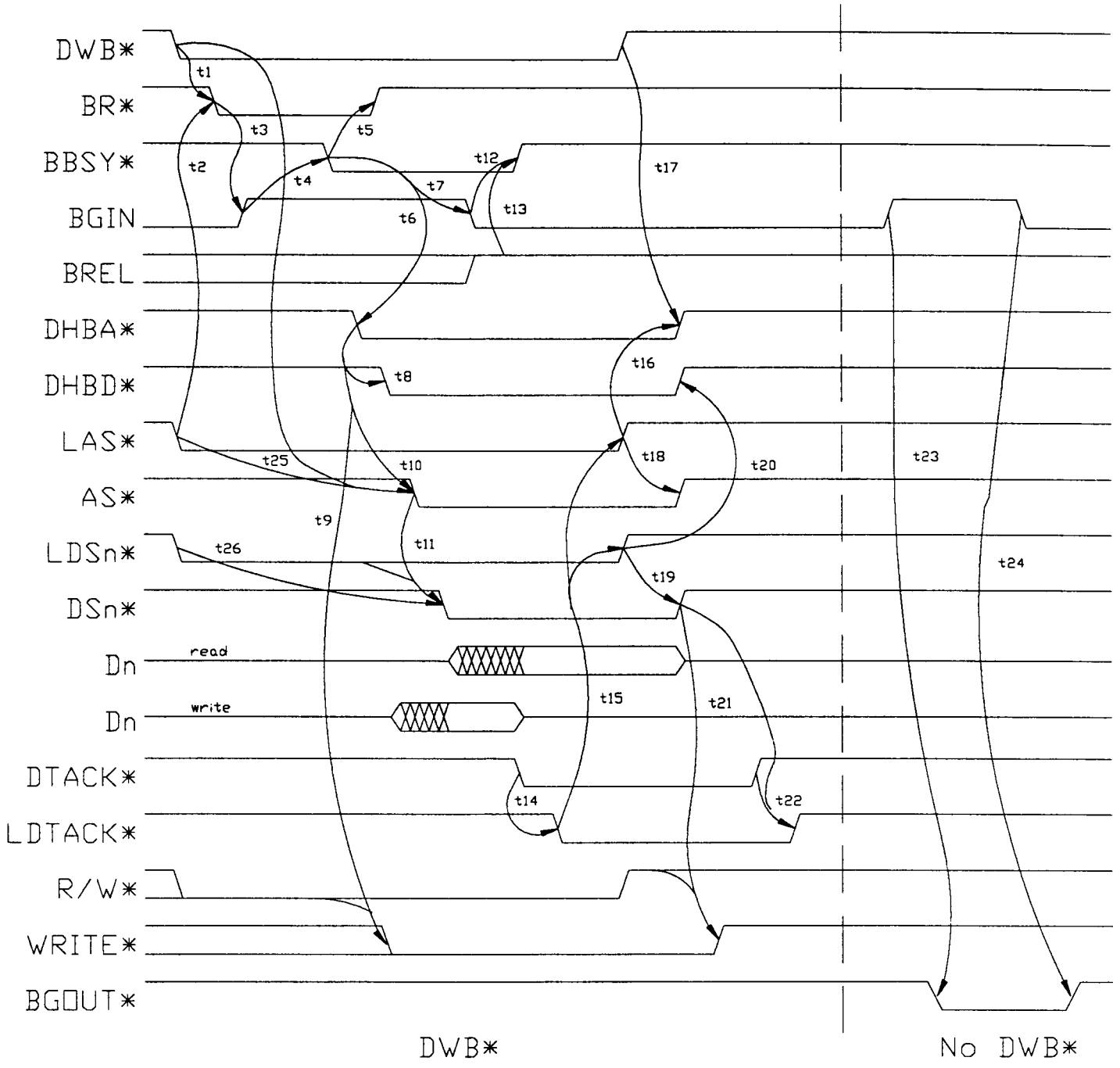


Figure 5. Timing Diagram

Timing Specifications

Timing Parameters	Signals	Max. Time(ns) unless otherwise specified		Description
		C-45	M-65	
t1	DWB* to BR* asserted	90	130	If DWB* is asserted after LAS*
t2	LAS* to BR* asserted	90	130	If LAS* is asserted after DWB*
t3	BR* to BG asserted	0	0	VME 1210 only when internal BR* generated (BG connected to BGIN)
		45	65	VME 1210 only when external BR* received (BG connected to BGIN)
		System arbiter time	System arbiter Time	VME 1220 only
t4	BGIN to BBSY* asserted	125	185	VME 1210 only, includes delay line: 55ns for M-65, 45ns for M-55, 35ns for C-45, 40ns for C-35, 60ns for C-25 part
		135	195	VME 1220 only
t5	BBSY* to BR* negated	45	65	
t6	BBSY* to DHBA* asserted	45	65	
t7	BBSY* to BGIN negated	45 max	65	VME 1210 only
		35 min	55 min	
		System arbiter time	System arbiter time	VME 1220 only
t8	DHBA* to DHBD* asserted	45	65	
t9	DHBA* to WRITE* asserted	45	65	Conditional upon R/W* value
t10	DHBA* to AS* asserted	90 70 (min.)	130	Ensures 35ns minimum address to AS* and data to DSn* set up times
t11	AS* to DSn* asserted	45	65	
t12	BGIN to BBSY* negated	80 max	120 max	VME 1210 only;
		70 min	110 min	VME 1210 only; t7min + t12min ≥ 90 ns min. BBSY* assertion
		135 max	195 max	VME 1220 only
		105 min	165 min	VME 1220 only. (see note below)
t13	BREL to BBSY* negated	45	65	Valid only when BREL is asserted after BGIN is negated
t14	DTACK* to LDTACK* asserted	45	65	
t15	LDTACK* to LAS*/LDSn* negated	@ Local master	@ Local master	Local master's time to negate strobes
t16	LAS* to DHBA* negated	45	65	If DWB* already negated
t17	DWB* to DHBA* negated	45	65	If LAS* already negated
t18	LAS* to AS* negated	50	72	
t19	LDSn* to DSn* negated	50	72	
t20	LDSn* to DSn* negated	50	72	
t21	DSn* to WRITE* negated	45	65	Ensures 10ns hold time
t22	DSn*/DTACK* to LDTACK* negated	45	65	Earliest negation of DSn* or DTACK* causes LDTACK* to be negated.
t23	BGIN to BGOUT* asserted	90	130	VME 1220 only
		25+d,35+d,45+d	55+d,65+d	VME 1210 only
t24	BGIN to BGOUT* negated	45	65	
t25	Latest of LAS*/DWB* to AS* asserted	135	195	Assertion time when already have bus (BBSY* asserted).
t26	Latest of DHBD*/LDS* to DS* asserted	45	65	Assertion time when already have bus (BBSY* asserted)

Note:

1. BBSY* is guaranteed to be asserted for a minimum of 90 ns in the VME 1210A devices and the C-45 device of the VME 1220A, even if BGIN is negated immediately after BBSY* is asserted. For the C-35 and C-25 VME 1220A devices, the sum of the system arbiter "BBSY* asserted to BGIN* negated" time and the t12 minimum time on the VME 1220A must be greater than 90 ns. Generally, this time will be taken up completely by the system arbiter time, however, if not, a delay line can be connected between pins 8 and 16 (DIP) or pins 10 and 19 (LCC) on the VME 1220A device to guarantee the 90 ns minumum. For example, if the system arbiter "BBSY* asserted to BGIN* negated" time was 35ns (min), no delay line would be needed for the C-35 VME 1220A device, since 35 + 75 > 90. However, a 10 ns delay line would be required for the C-25 VME 1220A.

Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground (pin 24 to pins 12, 18, & 20 DIP)	-0.5V to +7.0V
DC Voltage to Outputs in High Z State	-0.5V to +7.0V
UV Exposure	7000 Wsec/cm^2
DC Programming Voltage	14.0V

Operating Ranges

	Ambient Temperature	Supply Voltage (Vcc)
Commercial	0°C to +70°C	5V ± 5%
Industrial	-40°C to +85°C	5V ± 10%
Military	-55°C to +125°C	5V ± 10%

Electrical Characteristics Tested over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
V_{OH}	Output HIGH Voltage	V_{cc}=Min, $V_{IN}=V_{IH}$ or V_{IL}	I_{OH} = -3.0mA	2.4		V
V_{OL}	Output LOW Voltage	V_{cc}=Min, $V_{IN}=V_{IH}$ or V_{IL}	Pins (1210A/1220A), 16,17, 19,21 (DIP) (COM'L) I_{OL} = 24mA		0.5	V
			(MIL)		0.6	V
			Pins (1210A/1220A) 13,15 22,23 (DIP) (COM'L) I_{OL} = 48mA		0.5	V
			(MIL)		0.6	V
			Pins (1210B/1220B), 16,17, 19,21 (DIP) (COM'L) I_{OL} = 48mA		0.5	V
			(MIL)		0.6	V
			Pins (1210B/1220B) 13,15 22,23 (DIP) (COM'L) I_{OL} = 64mA		0.5	V
			(MIL)		0.6	V
V_{IH}	Input HIGH Level			2.0		V
V_{IL}	Input LOW Level				0.8	V
I_{IX}	Input Leakage Current	V_{SS} <= V_{IN} <= V_{CC}, V_{CC} = Max		-10	10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{SS} <= $V_{OU}T$ <= V_{CC}		-40	40	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_{OUT} = 0.5V		-30	-90	mA
I_{CC}	Power Supply Current	V_{CC} = Max, V_{IN} = GND Outputs Open (COM'L)			80	mA
		V_{CC} = Max, V_{IN} = GND Outputs Open (MIL)			90	mA

Capacitance (sample tested only)

Parameter	Test Conditions	Pins (DIP)	Typ	Units
C_{IN}	V_{IN} = 2.0V @ f = 1 MHz	2-11,14	5	pF
		13,15-17, 19,21-23	10	pF
C_{OUT}	V_{IN} = 2.0V @ f = 1 MHz	13,15-17, 19,21-23	10	pF

Hysteresis

Parameter	Description	Typ	Units
V_{T+}	Positive-going threshold	1.5	V
V_{T-}	Negative-going threshold	1.3	V
ΔV_T	Hysteresis (V_{T+} - V_{T-})	0.2	V

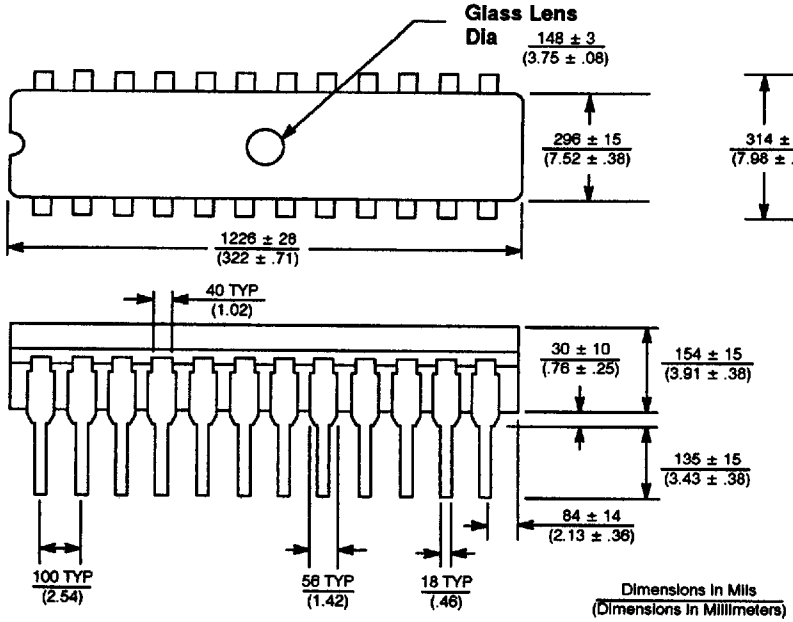
Packaging Information

The devices are available in a 24 pin slimline DIP (300 mil wide) or 28 pin LCC.

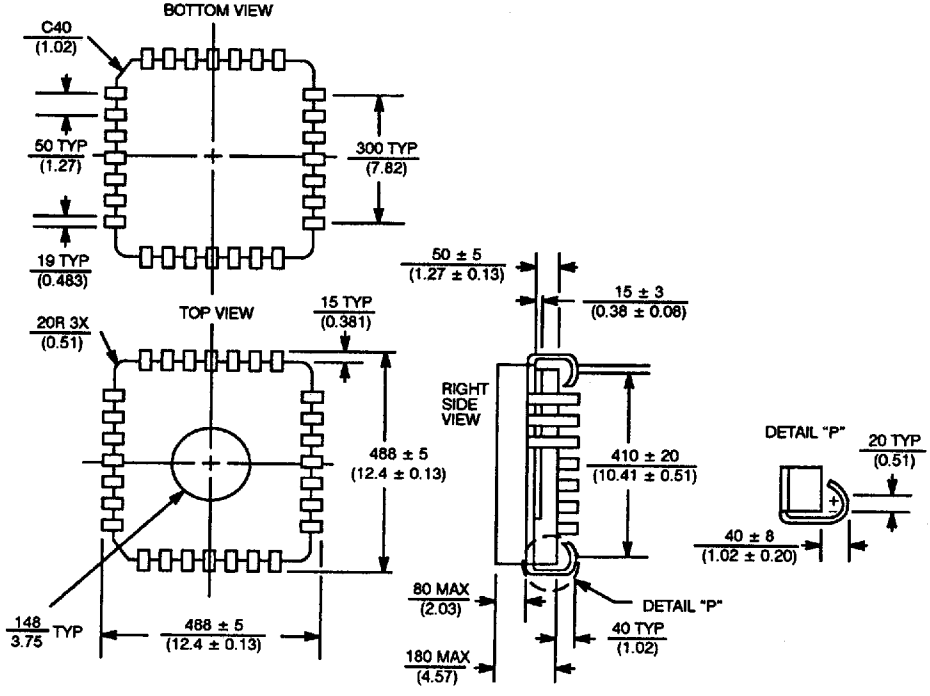
See PLX 448 or PLX 464 data sheets for package dimensions.

Contact PLX for further packaging information.

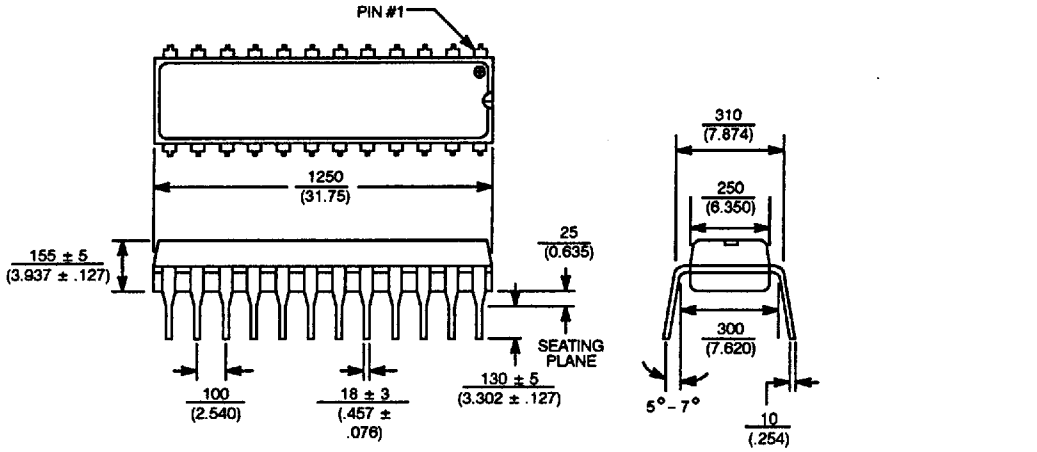
24-Lead Ceramic Dual In-line Package (CERDIP)



28-Pin J Lead Ceramic Chip Carrier



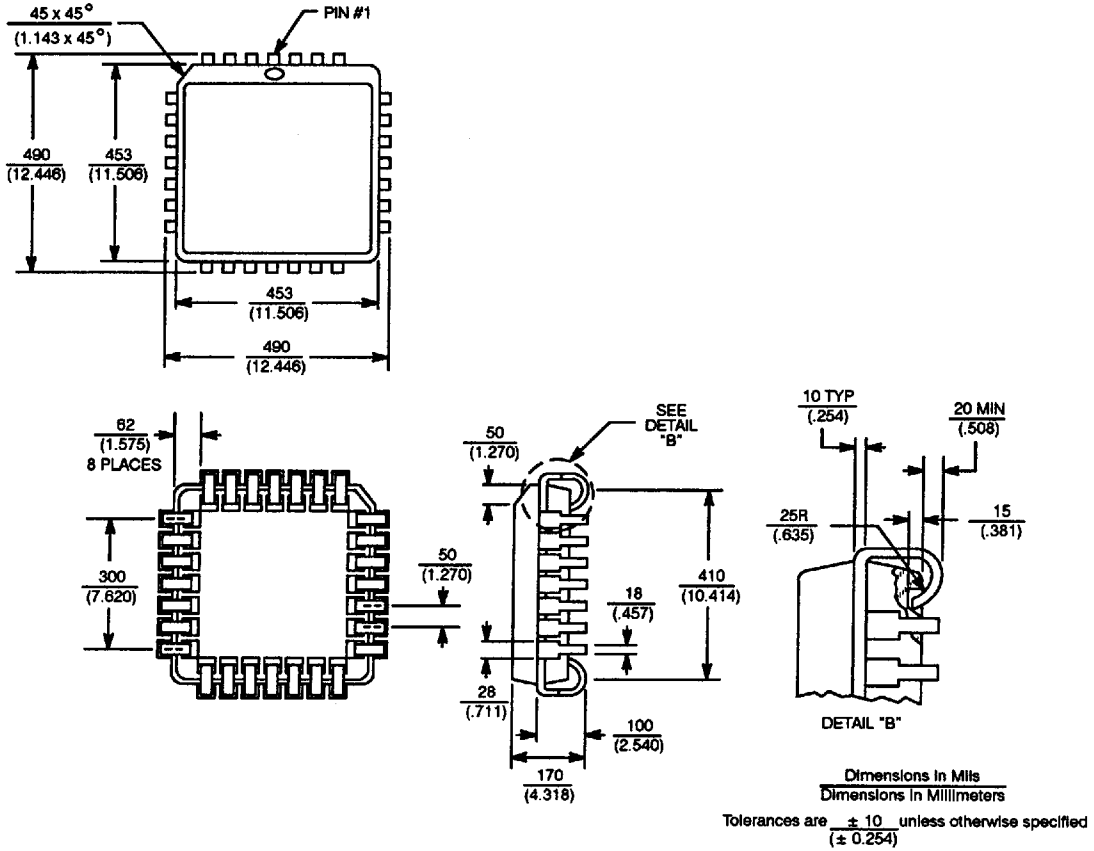
24-Pin DIP Plastic



Dimensions in Mils
Dimensions in Millimeters

Tolerances are ± 10 (± 0.254) unless otherwise specified

28-Pin LCC Plastic



Dimensions in Mils
Dimensions in Millimeters

Tolerances are ± 10 (± 0.254) unless otherwise specified