

100314

Low Power Quint Differential Line Receiver

General Description

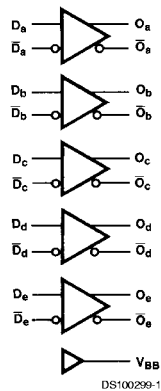
The 100314 is a monolithic quint differential line receiver with emitter-follower outputs. An internal reference supply (V_{BB}) is available for single-ended reception. When used in single-ended operation the apparent input threshold of the true inputs is 25 mV to 30 mV higher (positive) than the threshold of the complementary inputs. Unlike other F100K ECL devices, the inputs do not have input pull-down resistors.

Active current sources provide common-mode rejection of 1.0V in either the positive or negative direction. A defined output state exists if both inverting and non-inverting inputs are at the same potential between V_{EE} and V_{CC} . The defined state is logic HIGH on the $\bar{O}_a-\bar{O}_e$ outputs.

Features

- 35% power reduction of the 100114
- 2000V ESD protection
- Pin/function compatible with 100114
- Voltage compensated operating range = $-4.2V$ to $-5.7V$
- Standard Microcircuit Drawing (SMD) 5962-9162901

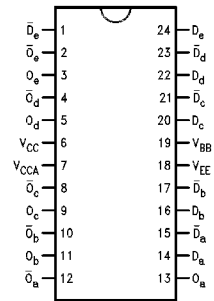
Logic Symbol



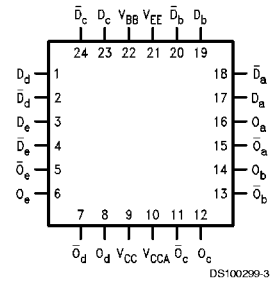
Pin Names	Description
D_a-D_e	Data Inputs
$\bar{D}_a-\bar{D}_e$	Inverting Data Inputs
O_a-O_e	Data Outputs
$\bar{O}_a-\bar{O}_e$	Complementary Data Outputs

Connection Diagrams

24-Pin DIP



24-Pin Quad Cerpak



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Above which the useful life may be impaired (Note 1)	
Storage Temperature (T_{STG})	-65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Pin Potential to Ground Pin (V_{EE})	-7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	-50 mA

ESD (Note 2)

≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Military	-55°C to +125°C
Supply Voltage (V_{EE})	-5.7V to -4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Military Version DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$ (Note 5)

Symbol	Parameter	Min	Typ	Max	Units	T_C	Conditions	Notes
V_{OH}	Output HIGH Voltage	-1025		-870	mV	0°C to +125°C	$V_{IN} = V_{IH}$ (Max) or V_{IL} (Min) Loading with 50Ω to -2.0V	(Notes 3, 4, 5)
		-1085		-870	mV	-55°C		
V_{OL}	Output LOW Voltage	-1830		-1620	mV	0°C to +125°C		
		-1830		-1555	mV	-55°C		
V_{OHC}	Output HIGH Voltage	-1035			mV	0°C to +125°C	$V_{IN} = V_{IH}$ (Max) or V_{IL} (Min) Loading with 50Ω to -2.0V	(Notes 3, 4, 5)
		-1085			mV	-55°C		
V_{OLC}	Output LOW Voltage			-1610	mV	0°C to +125°C		
				-1555	mV	-55°C		
V_{BB}	Output Reference Voltage			-1260	mV	0°C to +125°C	$I_{VBB} = 0 \mu A$, $V_{EE} = 4.2V$	(Notes 3, 4, 5)
		-1380		-1260	mV	0°C to +125°C	$I_{VBB} = -250 \mu A$, $V_{EE} = -5.7V$	(Notes 3, 4, 5)
		-1396			mV	-55°C	$I_{VBB} = -350 \mu A$, $V_{EE} = -5.7V$	
V_{DIFF}	Input Voltage Differential	150			mV	-55°C to +125°C	Required for Full Output Swing	(Notes 3, 4, 5)
V_{CM}	Common Mode Voltage	$V_{CC} - 2.0$		$V_{CC} - 0.5$	V	-55°C to +125°C		(Notes 3, 4, 5)
V_{IH}	Single-Ended Input High Voltage	-1165		-870	mV	-55°C to +125°C	Guaranteed HIGH Signal for All Inputs (with \overline{D}_n tied to V_{BB})	(Notes 3, 4, 5, 6)
V_{IL}	Single-Ended Input Low Voltage	-1830		-1475	mV	-55°C to +125°C	Guaranteed LOW Signal for All Inputs (with \overline{D}_n tied to V_{BB})	(Notes 3, 4, 5, 6)
I_{IH}	Input HIGH Current			50	μA	0°C to +125°C	$V_{IN} = V_{IH}$ (Max), $D_a - D_e = V_{BB}$, $\overline{D}_a - \overline{D}_e = V_{IL}$ (Min)	(Notes 3, 4, 5)
				70	μA	-55°C		
I_{CBO}	Input Leakage Current	-10			μA	-55°C to +125°C	$V_{IN} = V_{EE}$, $D_a - D_e = V_{BB}$, $\overline{D}_a - \overline{D}_e = V_{IL}$ (Min)	(Notes 3, 4, 5)
I_{EE}	Power Supply Current	-65		-25	mA	-55°C to +125°C	$D_a - D_e = V_{BB}$, $\overline{D}_a - \overline{D}_e = V_{IL}$ (Min)	(Notes 3, 4, 5)

Note 3: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 4: Screen tested 100% on each device at -55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 5: Sample tested (Method 5005, Table I) on each manufactured lot at -55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 6: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH}	Propagation Delay	0.40	2.30	0.60	2.20	0.60	2.70	ns	Figures 1, 2	(Notes 7, 8, 9)
t_{PHL}	Data to Output									
t_{TLH}	Transition Time	0.20	1.40	0.20	1.40	0.20	1.40	ns		(Note 10)
t_{THL}	20% to 80%, 80% to 20%									

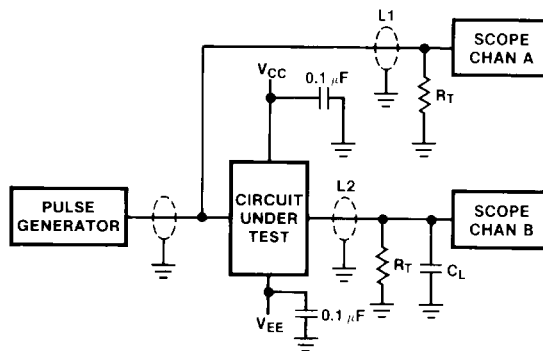
Note 7: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 8: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.

Note 9: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 10: Not tested at $+25^\circ C$, $+125^\circ C$ and $-55^\circ C$ temperature (design characterization data).

Test Circuit



DS100259-5

Note: V_{CC} , $V_{CCA} = +2V$, $V_{EE} = -2.5V$
 $L1$ and $L2 =$ equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 $C_L =$ Fixture and stray capacitance $\leq 3 pF$

FIGURE 1. AC Test Circuit

Switching Waveforms

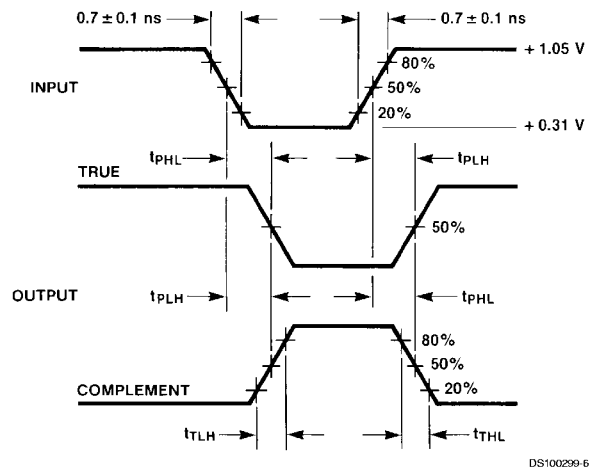
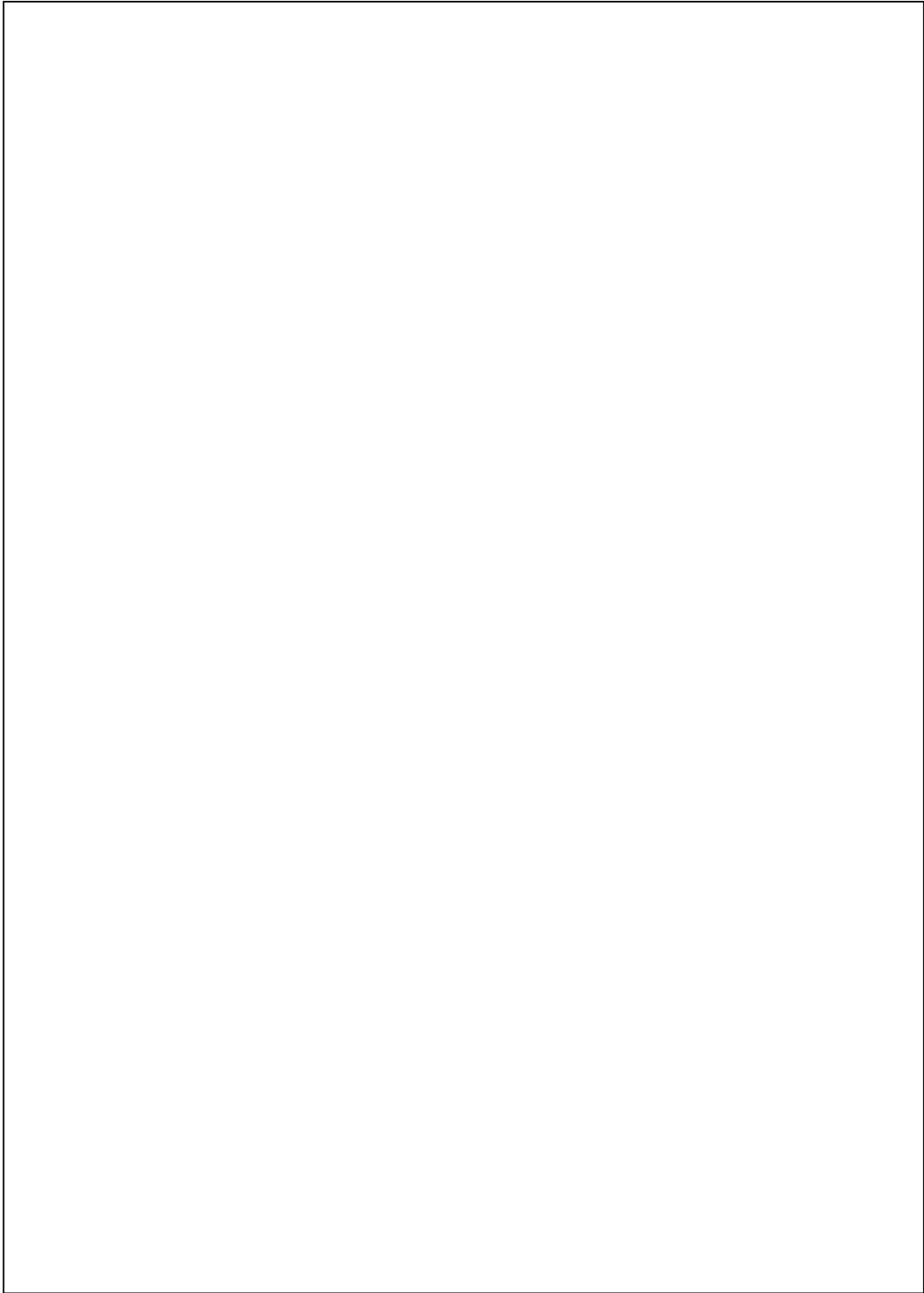
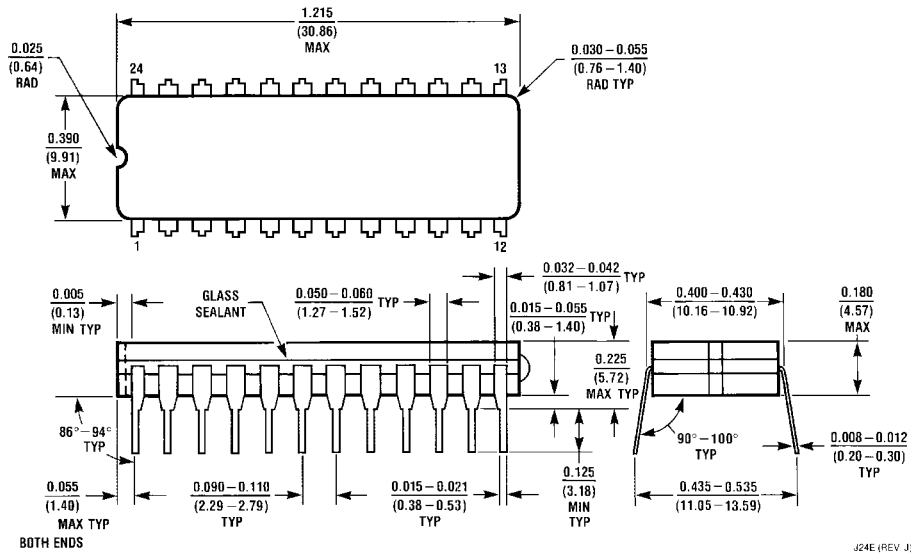


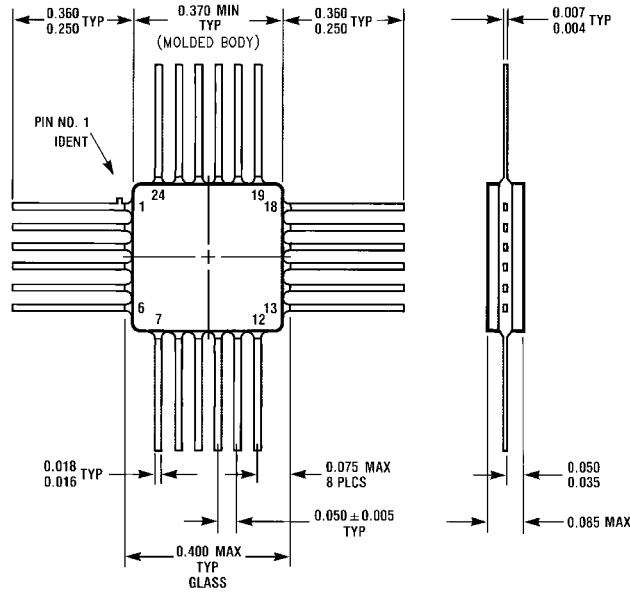
FIGURE 2. Propagation Delay and Transition Times



Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
NS Package Number J24E



24-Lead Quad Cerpak (F)
NS Package Number W24B