

### Features

- Operating voltage 2.7V~5.5V
- Low power consumption
  - Operation: 25mA max. ( $V_{CC}=5V$ )  
10mA max. ( $V_{CC}=3V$ )
  - Standby: 30 $\mu$ A max. ( $V_{CC}=5V$ )  
10 $\mu$ A max. ( $V_{CC}=3V$ )
- Access time: 150ns max. ( $V_{CC}=5V$ )  
250ns max. ( $V_{CC}=3V$ )
- 32768×8 bits of mask ROM
- Mask options: chip enable  $\overline{CE}/\overline{CE}/\overline{OE1}/\overline{OE1}$  and output enable  $\overline{OE}/\overline{OE}/\overline{NC}$
- TTL compatible inputs and outputs
- Tristate outputs
- Fully static operation
- Package type: 28-pin DIP/SOP

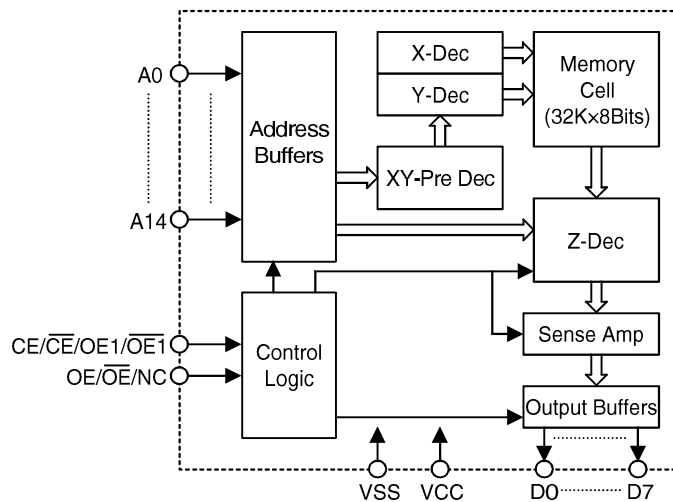
### General Description

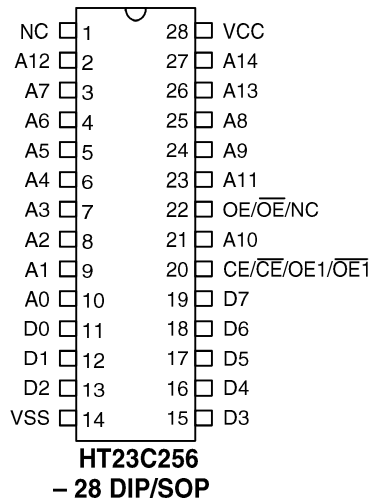
The HT23C256 is a read-only memory with high performance CMOS storage device whose 256K of memory is arranged into 32768 words by 8 bits.

For application flexibility, the chip enable and output enable control pins can be selected as active high or active low. This flexibility not only allows easy interface with most microproc-

essors, but also eliminates bus contention in multiple bus microprocessor systems. An additional feature of the HT23C256 is its ability to enter the standby mode whenever the chip enable ( $\overline{CE}/\overline{CE}$ ) is inactive, thus reducing current consumption to below 30 $\mu$ A. The combination of these functions makes the chip suitable for high density low power memory applications.

### Block Diagram



**Pin Assignment**

**Pin Description**

Pin Name	I/O	Description
A0~A14	I	Address inputs
D0~D7	O	Data outputs
CE/ $\overline{\text{CE}}$ /OE1/ $\overline{\text{OE1}}$	I	Chip enable/Output enable input
OE/ $\overline{\text{OE}}$ /NC	I	Output enable input
VSS	I	Negative power supply
VCC	I	Positive power supply
NC	—	No connection

**Operation Truth Table**

Mode	CE/ $\overline{\text{CE}}$	OE/ $\overline{\text{OE}}$	A0~A14	D0~D7
Read	H/L	H/L	Valid	Data Out
Deselect	H/L	L/H	X	High Z
Standby	L/H	X	X	High Z

Note: H= $V_{IH}$ , L= $V_{IL}$ , X= $V_{IH}$  or  $V_{IL}$

**Absolute Maximum Ratings\***

Supply Voltage ..... -0.3V to 6V      Storage Temperature ..... -50°C to 125°C  
 Input Voltage ..... -0.3V to  $V_{CC}+0.3V$       Operating Temperature ..... -40°C to 85°C

\*Note: These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

**D.C. Characteristics**
**Supply voltage: 2.7V~3.6V**
 **$T_a = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		VCC	Conditions				
$V_{CC}$	Operating Voltage	—	—	2.7	—	3.6	V
$I_{CC}$	Operating Current	3V	O/P Unload, $f = 5\text{MHz}$	—	—	10	mA
$V_{IL}$	Input Low Voltage	3V	—	$V_{SS}$	—	0.4	V
$V_{IH}$	Input High Voltage	3V	—	2.0	—	$V_{CC}$	V
$V_{OL}$	Output Low Voltage	3V	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
$V_{OH}$	Output High Voltage	3V	$I_{OH} = -0.4\text{mA}$	2.4	—	$V_{CC}$	V
$I_{LI}$	Input Leakage Current	3V	$V_{IN} = 0$ to $V_{CC}$	—	—	10	$\mu\text{A}$
$I_{LO}$	Output Leakage Current	3V	$V_{OUT} = 0$ to $V_{CC}$	—	—	10	$\mu\text{A}$
$I_{STB1}$	Standby Current	3V	$\overline{CE} = V_{IL}$ $\overline{CE} = V_{IH}$	—	—	500	$\mu\text{A}$
$I_{STB2}$	Standby Current	3V	$\overline{CE} \leq 0.2V$ $\overline{CE} \geq V_{CC} - 0.2V$	—	—	10	$\mu\text{A}$
$C_{IN}$	Input Capacitance (See note)	—	$f = 1\text{MHz}$	—	—	10	pF
$C_{OUT}$	Output Capacitance (See note)	—	$f = 1\text{MHz}$	—	—	10	pF

Note: These parameters are periodically sampled but not 100% tested.

Supply voltage: 4.5V~5.5V

Ta=-40°C to 85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>CC</sub>	Conditions				
V <sub>CC</sub>	Operating Voltage	—	—	4.5	—	5.5	V
I <sub>CC</sub>	Operating Current	5V	O/P Unload, f=5MHz	—	—	25	mA
V <sub>IL</sub>	Input Low Voltage	5V	—	V <sub>SS</sub>	—	0.8	V
V <sub>IH</sub>	Input High Voltage	5V	—	2.2	—	V <sub>CC</sub>	V
V <sub>OL</sub>	Output Low Voltage	5V	I <sub>OL</sub> =3.2mA	—	—	0.4	V
V <sub>OH</sub>	Output High Voltage	5V	I <sub>OH</sub> =-1mA	2.4	—	V <sub>CC</sub>	V
I <sub>LI</sub>	Input Leakage Current	5V	V <sub>IN</sub> =0 to V <sub>CC</sub>	—	—	10	μA
I <sub>LO</sub>	Output Leakage Current	5V	V <sub>OUT</sub> =0 to V <sub>CC</sub>	—	—	10	μA
I <sub>STB1</sub>	Standby Current	5V	CE=V <sub>IL</sub> CE=V <sub>IH</sub>	—	—	1.5	mA
I <sub>STB2</sub>	Standby Current	5V	CE ≤ 0.2V CE ≥ V <sub>CC</sub> -0.2V	—	—	30	μA
C <sub>IN</sub>	Input Capacitance (See note)	—	f=1MHz	—	—	10	pF
C <sub>OUT</sub>	Output Capacitance (See note)	—	f=1MHz	—	—	10	pF

Note: These parameters are periodically sampled but not 100% tested.

**A.C. Characteristics**

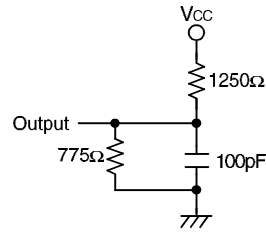
Ta=-40°C to 85°C

Symbol	Parameter	V <sub>CC</sub> =2.7V~3.6V		V <sub>CC</sub> =4.5V~5.5V		Unit
		Min.	Max.	Min.	Max.	
t <sub>CYC</sub>	Cycle Time	250	—	150	—	ns
t <sub>AA</sub>	Address Access Time	—	250	—	150	ns
t <sub>ACE</sub>	Chip Enable Access Time	—	250	—	150	ns
t <sub>AOE</sub>	Output Enable Access Time	—	150	—	80	ns
t <sub>OH</sub>	Output Hold Time	—	—	10	—	ns
t <sub>OD</sub>	Output Disable Time (See Note)	—	—	—	70	ns
t <sub>OE</sub>	Output Enable Time (See Note)	—	—	10	—	ns

Note: These parameters are periodically sampled but not 100% tested.

**A.C. test conditions**

Output load: see figure right  
 Input rise and fall time: 10ns  
 Input pulse levels: 0.4V to 2.4V  
 Input and output timing reference levels:  
 0.8V and 2.0V ( $V_{CC}=5V$ ), 1.5V ( $V_{CC}=3V$ )



\* Including scope and jig

Output load circuit

**Functional Description**

The HT23C256 has two modes, namely data read mode and standby mode, controlled by  $\overline{CE}/\overline{OE1}/\overline{OE1}$  and  $\overline{OE}/\overline{OE/NC}$  inputs.

• Standby mode

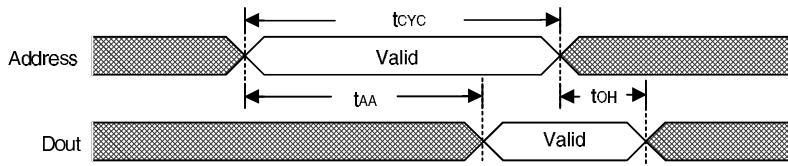
The HT23C256 has lower current consumption, controlled by the chip enable input ( $\overline{CE}/\overline{CE}$ ). When a low/high level is applied to the  $\overline{CE}/\overline{CE}$  input regardless of the output enable ( $\overline{OE}/\overline{OE/NC}$ ) states the chip will enter the standby mode.

• Data read mode

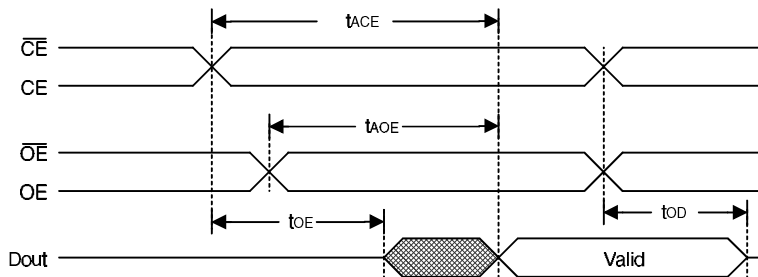
When both the chip enable ( $\overline{CE}/\overline{CE}/\overline{OE}/\overline{OE1}$ ) and the output enable ( $\overline{OE}/\overline{OE/NC}$ ) are active, the chip is in data read mode. Otherwise, active  $\overline{CE}/\overline{CE}$  and inactive  $\overline{OE}/\overline{OE/NC}$  result in deselect mode. The output will remain in Hi-Z state.

**Timing Diagrams**

• Propagation delay due to address ( $\overline{CE}/\overline{CE}/\overline{OE1}/\overline{OE1}$  and  $\overline{OE}/\overline{OE}$  are active)



• Propagation delay due to chip enable and output enable (address valid)



Characteristic Curves

