32K(4Kx8) EEPROM with I²C Interface .

DESCRIPTION

The IN24AA32AN, IN24AA32AD, IN24LC32AN, IN24LC32AD are a 32K(4Kx8) nonvolatile Electrically Erasable PROM with I²C Interface .
The ICs is purposed for reading & writing in byte or page (32byte) modes and long time nonvolatile data storage in electronic units with I²Cinterface.
The ICs are functionally and pin compatible to 24AA32 (Microchip)
IN24AA32AN, IN24LC32AN are realized in DIP-8 (MS-001BA) package.
IN24AA32AD, IN24LC32AD are realized in SO-8 (MS-012AA) package.

FEATURES

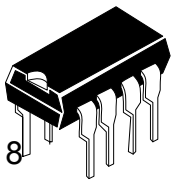
- Data capacity, Q_{INF}: 32768 bit,
- Supply voltage range , U_{CC}

for IN24AA32AN, IN24AA32AD 1,8 …5,5 V;
for IN24LC32AN, IN24LC32AD 2,5 …5,5 V;

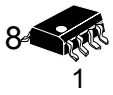
- Maximum clock frequency, f_C:

for 2,5 V ≤ U_{CC} ≤ 5,5 V 400 kHz;
for 1,8 V ≤ U_{CC} ≤ 5,5 V 100 kHz;

- Maximum stand-by current, I_{CC} 1,0 uA;
- Maximum read current, I_{OCCR} 0,4 mA;
- Maximum write current, I_{OCCW} 3,0 mA;
- Endurance $N_{E/W}$, 1000000 cycles;
- Operating temperature range -40 … +85°C.



N SUFFIX
DIP



D SUFFIX
SOIC

IN24AA32AN, IN24LC32AN are realized in DIP-8 (MS-001BA) package.
IN24AA32AD, IN24LC32AD are realized in SO-8 (MS-012AA) package.

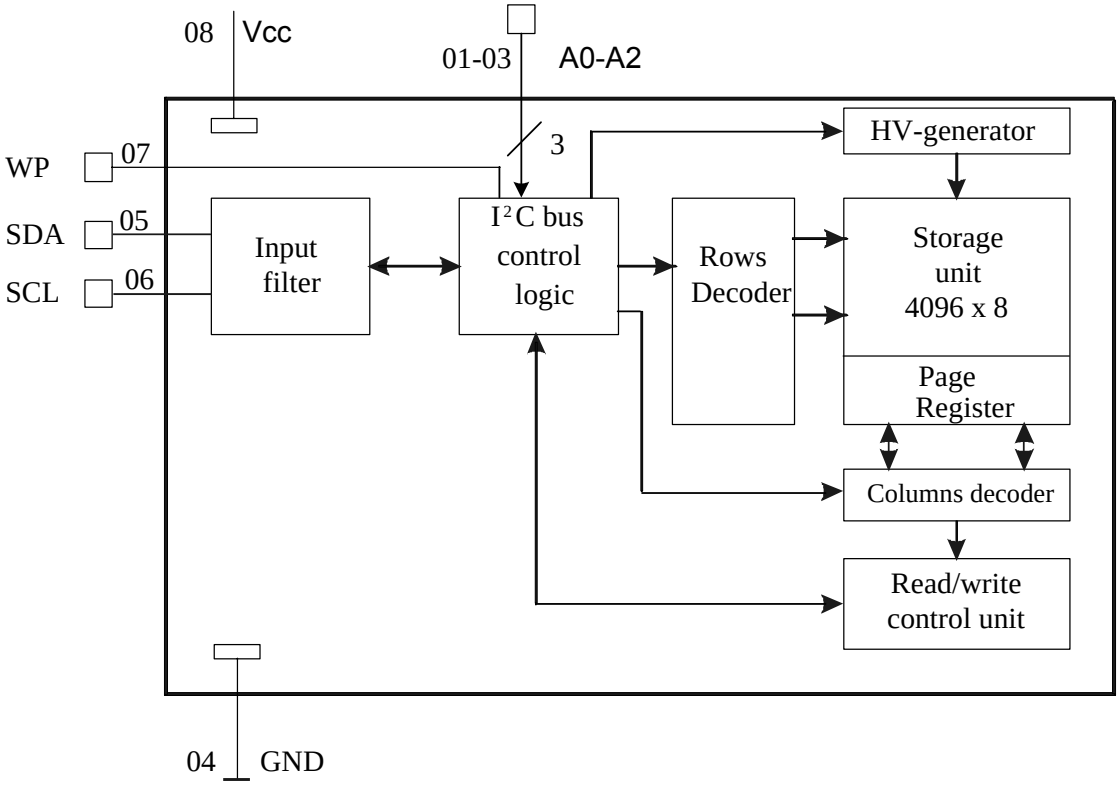


Fig.2 Block Diagram

Table 1 – Pin description

Pin number	Pin Name	Function
01	A0	Address input
02	A1	Address input
03	A2	Address input
04	GND	Common pin
05	SDA	Serial Data I/O pin
06	SCL	Clock Input
07	$\overline{WP}$	Write disable input (U_{WP} = GND for write enable mode, U_{WP} = U_{CC} for write disable mode)
08	V_{CC}	Power supply pin

Table 2 Recommended Operation Conditions & Maximum Ratings*

Parameter, unit		Symbol	Recommended Operation Conditions		Maximum Ratings	
			Min	Max	Min	Max
Supply voltage,V	IN24AA32AN, IN24AA32AD	Ucc	1,8	5,5	0	6,5
	IN24LC32AN, IN24LC32AD		2,5	5,5		
High level input voltage, V		U_{IH}	0,7Ucc	-	–	Ucc + 1,0
Low level input voltage, V	2,5 V ≤ Ucc ≤ 5,5 V	U_{IL}	-	$0,3U_{CC}$	- 0,3	-
	1,8 V ≤ Ucc < 2,5 V (IN24AA32AN, IN24AA32AD)		-	$0,2U_{CC}$		
Low level output current мА		I_{OL}	–	–	2,1	-
Load capacity,pF		C_L	-	100	-	-

Table 3 Electric Parameters

Parameter, unit	Symbol	Mode	Min	Max	T_A, °C
Low level output voltage, V	U_{OL}	U_{CC} = 2,5 V, I_{OL} = 2,1 mA	–	0,4	25 ± 10; -45; 85
		U_{CC} = 4,5 V, I_{OL} = 3,0 mA	-	0,4	
Low level input leakage current, uA	I_{ILL}	U_{CC} = 5,5 V, U_{IL} = 0,1V	–	-1,0	
High level input leakage current, uA	I_{ILH}	U_{CC} = 5,5 V, U_{IL} = 5,5 V	-	1,0	
Low level output leakage current, uA	I_{OLL}	U_{CC} = 5,5 V, U_O = 0,1V	-	-1,0	
High level output leakage current, uA	I_{OLH}	U_{CC} = 5,5 V, U_0 = 5,5 V	–	1,0	
Consumption current, uA	I_{CC}		–	1,0	
Consumption current (Operating Read), mA	$I_{OCC\ R}$	Ucc = 5,5 V, f_C = 400 kHz	–	0,4	
Consumption current (Operating Write), mA	$I_{OCC\ W}$	Ucc = 5,5 V, f_C = 400 kHz	–	3,0	
SCL, SDA pins noise signal duration, ns	t_{SP}			50	
Switch-on transition time (measured on U_{IHmin} & U_{ILmax} levels), ns	t_{OF}	1,8 V ≤ U_{CC} < 2,5 V, I_{OL}=3,0 mA, C_L≤100 pF (for IN24AA32AN, IN24AA32AD)	–	250	
		2,5V ≤ U_{CC} ≤ 5,5V I_{OL}=3,0 mA, C_L≤100 pF	20+0,1C_L	250	
Write/Erase cycle duration (byte, page modes), ms	t_{CY}	U_{CC} = 4,5 V f_C = 1 MHz	–	5	
SCL, SDA, pins hysteresis voltage, V	U_{HYS}		0,05Ucc	-	
Program/erase cycles per byte	$N_{E/W}$		1000000	-	

Table 4 –I²C bus parameters (-40 °C ≤ Ta ≤ 85 °C)

Parameter, unit	Symbol	1,8 V ≤ U_{CC} < 2,5 V*		2,5 V ≤ U_{CC} ≤ 5,5V	
		Min.	Max.	Min.	Max.
Clock frequency, kHz	f_C	-	100	-	400
Time the bus to be free before generation of «Start» condition, us	t_{BUF}	4,7	-	1,3	-
«Start» condition hold time , us	$t_{HD.STA}$	4,0	-	0,6	-
SCL pin low level duration , us	t_{LOW}	4,7	-	1,3	-
SCL pin high level duration , us	t_{HIGH}	4,0	-	0,6	-
«Start» condition setup time , us	$t_{SU.STA}$	4,7	-	0,6	-
Data hold time for slave transmitter, ns	$t_{HD.DAT}$	0	-	0	-
Data setup time, ns	$t_{SU.DAT}$	250	-	100	-
Data access time on SCL signal, us	t_{AA}	-	3,5	-	0,9
SDA, SCL rise time, us	t_r	-	1,0	-	0,3
SDA, SCL fall time, us	t_f	-	300	-	300
«Stop » condition setup time , us	$t_{SU.STO}$	4,0	-	0,6	-
Data hold time for write disable mode, us	$t_{HD.WP}$	4,7	-	1,3	-
Data setup time for write disable mode, us	$t_{SU.WP}$	4,0	-	0,6	-

Note – Being transmitter, IC has to provide internal delay not less 300 ns, to exept random generation of «Start » & «Stop » conditions

* I²C bus parameters for supply voltage range 1,8 V ≤ U_{CC} < 2,5 V are indicated for IN24AA32AN, IN24AA32AD only

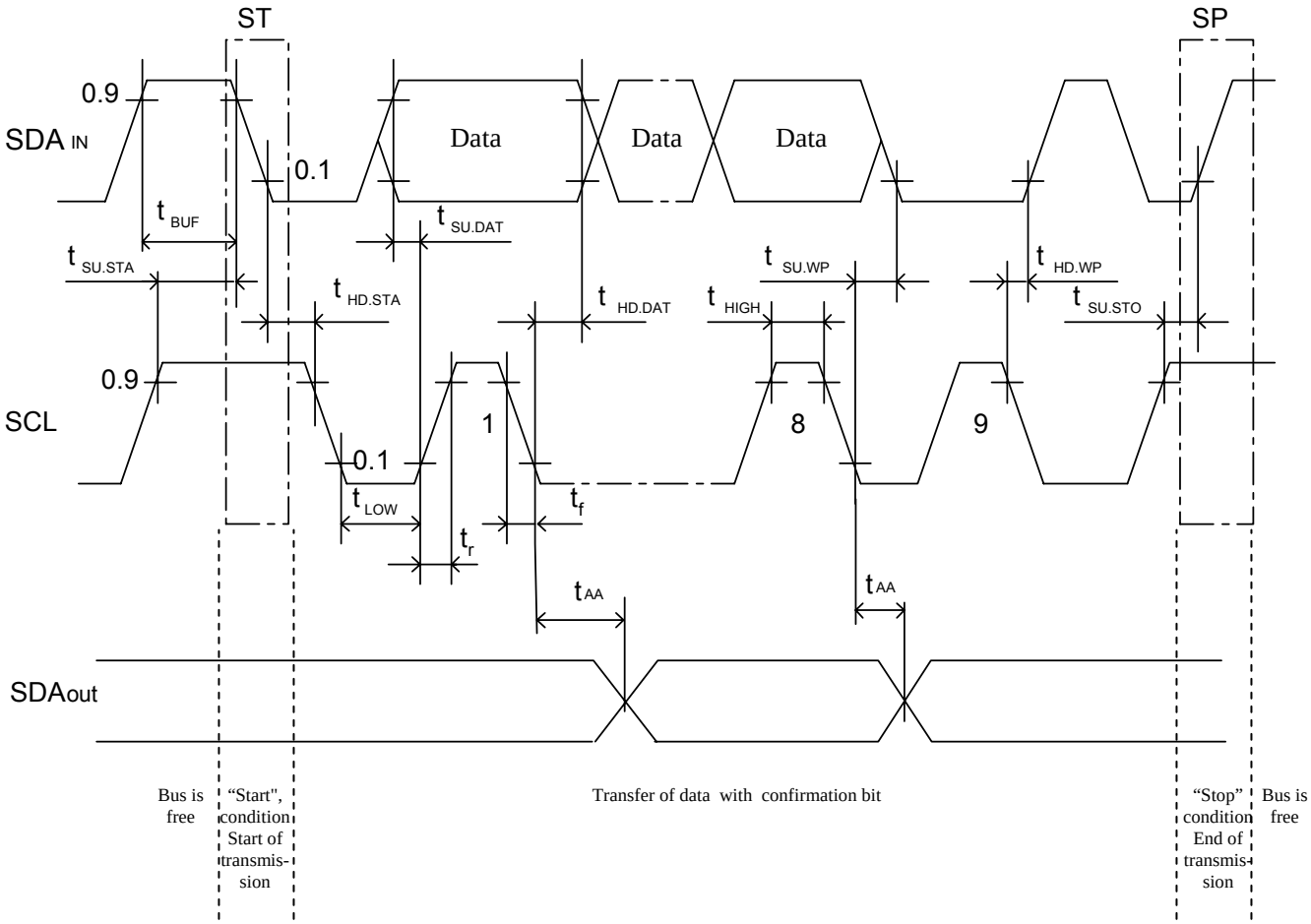


Fig. 3 –I^2C –bus operation time diagramm

Tab. 5 – Control words format

Symbol	Bit number								9th bit (confirmation bit)	Function
	1	2	3	4	5	6	7	8		
CS/WR	1	0	1	0	A2	A1	A0	0	"0", from chip	Chip select word for write operation
CS/RD	1	0	1	0	A2	A1	A0	1	"0", from chip	Chip select word for read out operation
WA (1 байт WA1)	X7	X6	X5	X4	X3	X2	X1	X0	"0", from chip	Word address Low address byte
(2 байт WA2)	0	0	0	0	X11	X10	X9	X8		High address byte
DE	D7	D6	D5	D4	D3	D2	D1	D0	"0", from chip	Input data
DA	D7	D6	D5	D4	D3	D2	D1	D0	"0" or "1", from "Master"	Reading data

* "Master" – device that control data transmission through bus , (MPU, MCU)

Chip select word consist of few parts:

- 1-4th bits are fixed combination saved inside chip. These bits is used for indentification of chip type;
- 5-7th bits have to correspond to state of address inputs A0-A2. These bits allow to increase data capacity by means of connecting up to 8 ICs to one bus;
- 8th bit indicates direction of data transfer ("0" – write data to IC, "1" – read-out data from IC).

Tab. 6 – Main states of I^2C-bus

Symbol	Purpose
ST	"Start" condition. Transition of SDA bus from high to low while SCL is high.
SP	"Stop" condition. Transition of SDA bus from low to high while SCL is high.
PROG	Active programming cycle
As	Confirmation bit from IC A_S = 0 – IC received input data
Am	Confirmation bit from "Master" Am = 0 – autoincremrnt , Am = 1 - before "Stop" condition
X0-X7	Address bits of a byte
D0-D7	Data bits
A2 – A0	Bits of data capacity increasing on I^2C-bus. These bits have to correspond to state of address inputs A0-A2

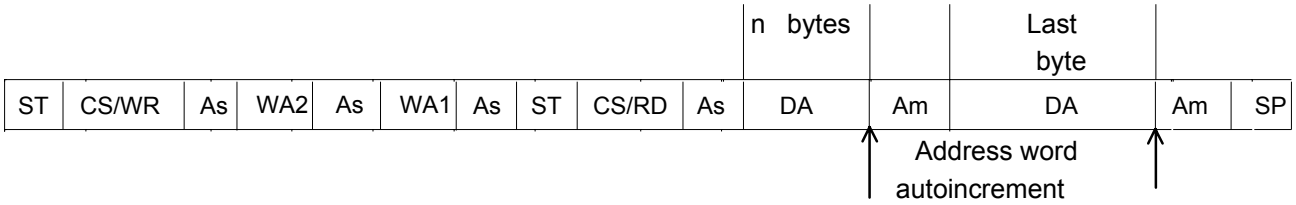


Fig. 4 Protocol of I^2C –bus for mode "Read defined address word"

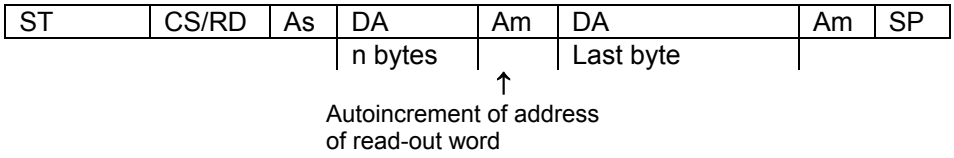


Fig. 5 Protocol of I^2C –bus for mode "Read random address"

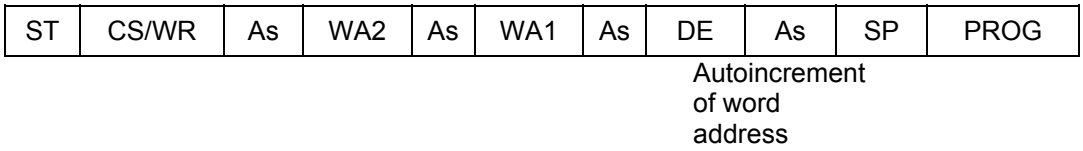


Fig. 6 Protocol of I^2C –bus for mode " Write/Erase Byte "

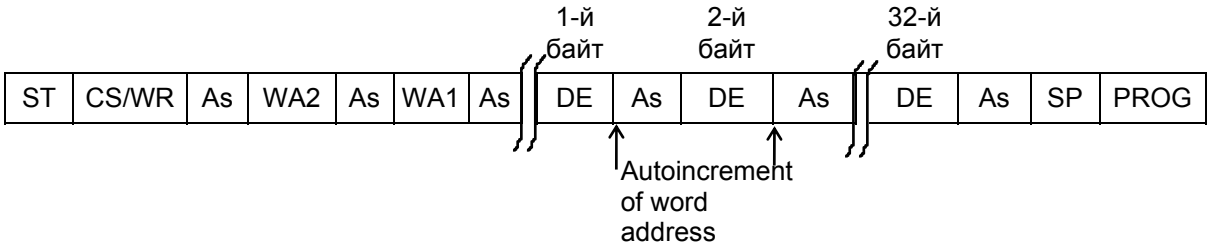
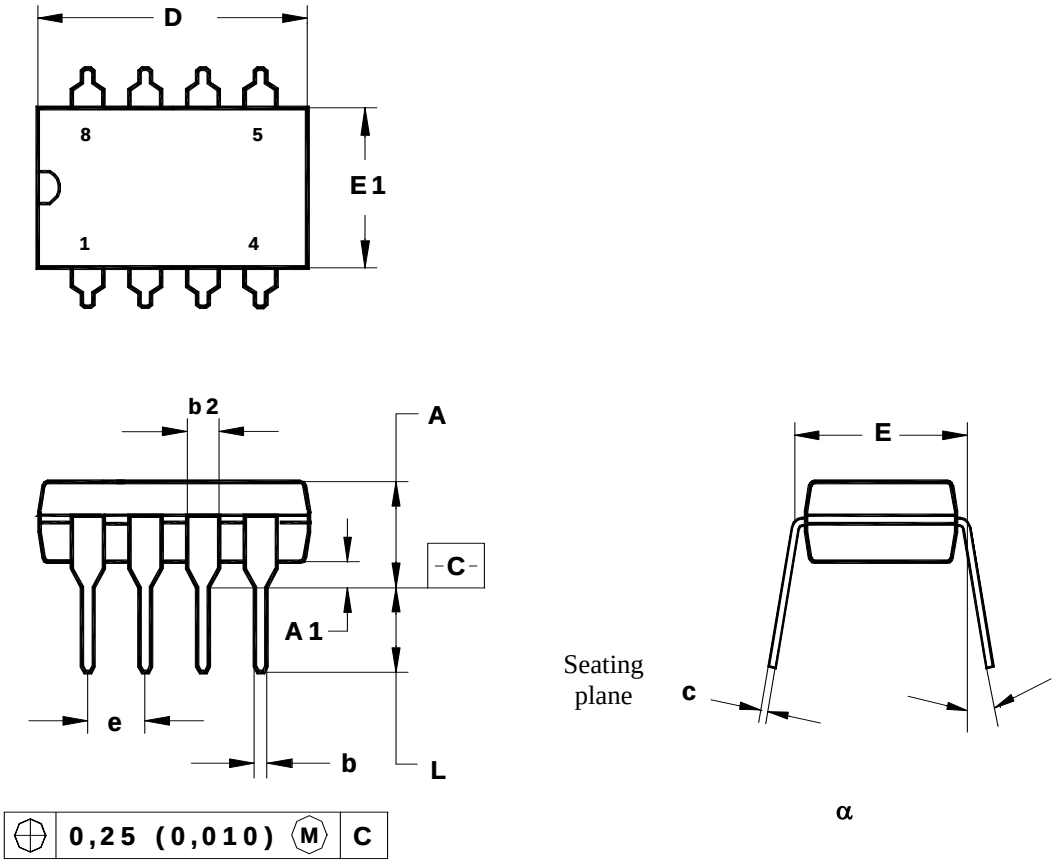


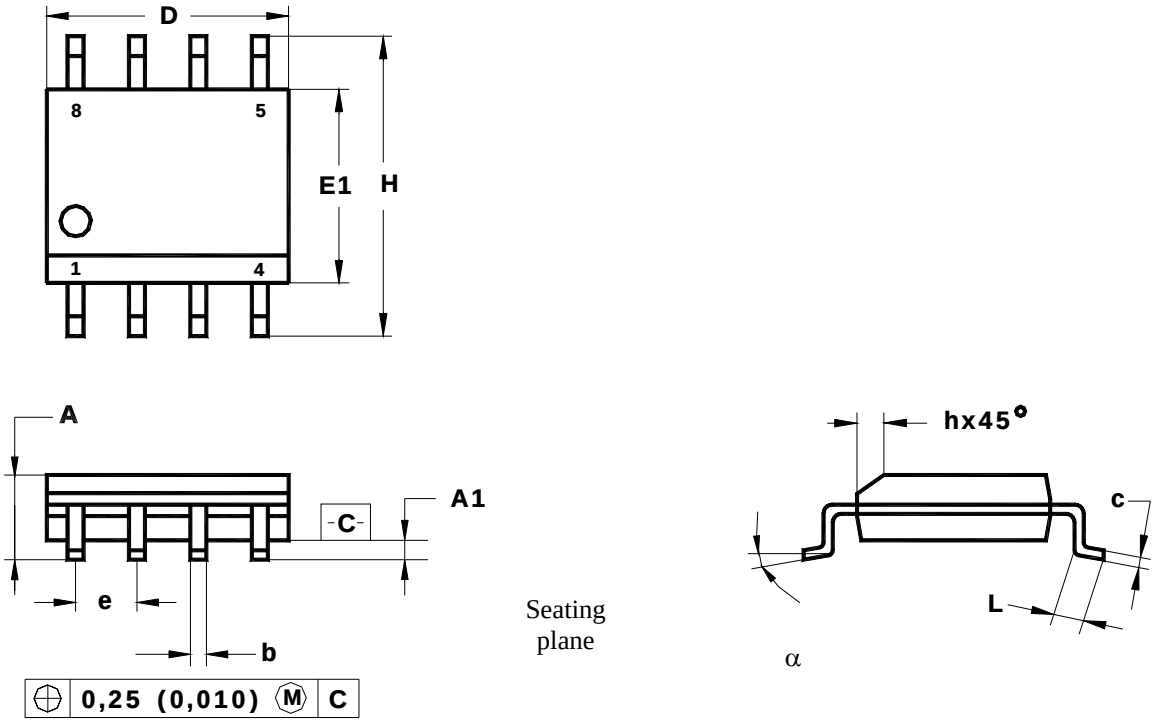
Fig. 7 Protocol of I^2C –bus for mode " Write/Erase Page "

N SUFFIX PLASTIC DIP
(MS-001BA)



	D	E1	A	b	b2	e	α	L	E	c	A1
mm											
min	9.02	6.07	—	0.36	1.14		0°	2.93	7.62	0.20	0.38
max	10.16	7.11	5.33	0.56	1.78	2.54	15°	3.81	8.26	0.36	—
inches											
min	0.355	0.240	—	0.014	0.045		0°	0.115	0.300	0.008	0.015
max	0.400	0.280	0.210	0.022	0.070	0.1	15°	0.150	0.325	0.014	—

D SUFFIX PLASTIC SOP
(MS-012AA)



	D	E1	H	b	e	α	A	A1	c	L	h
mm											
min	4.80	3.80	5.80	0.33		0°	1.35	0.10	0.19	0.41	0.25
max	5.00	4.00	6.20	0.51	1.27	8°	1.75	0.25	0.25	1.27	0.50
inches											
min	0.1890	0.1497	0.2284	0.013		0°	0.0532	0.0040	0.0075	0.016	0.0099
max	0.1968	0.1574	0.2440	0.020	0.100	8°	0.0688	0.0090	0.0098	0.050	0.0196