AVXX32E -A SERIES

DATA SHEET

APLUS INTEGRATED CIRCUITS INC.

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Features

- Operating voltage: 2.4V~5.0V
- One single-key can implement play-all, play-next and random function.
- Maximum play count is 16.
- Each input can implement looping function.
- Single-key input can be last-key priority for stand-alone input or first-key priority.
- Each input trigger can select trigger mode: (For OKY, TG0, TG1, TG3) Edge/Level, Hold/Unhold, Retrigger/Irretrigger.
- Each input trigger can select its own debounce time:
  Fast debounce: < 200us;
  Slow debounce: ~16ms (S.R.=6.0kHz)
- Support bouncing trigger solution for retrigger application. (Second trigger force to retrigger and slow debounce.)
- Maximum table entries are 204*4.
- Word count is only limited by ROM capacity.
- 3 output ports for Status or LED application:
  - OP_A Status:
    Busy_high, DC_low, Stop_high,DC_high
    LED: +Fast,+Slow, Dyn(7/10), Off
  - OP_B Status:
    Busy_high, DC_low, Stop_high, DC_high
    LED: -Fast, -Slow, Dyn(9/10), On
  - OP_C Status: Busy_high, DC_low, Busy_low, DC_high
    LED: +Fast, +Slow, On, Off
- Each output can specify its initial state (High or Low)
- Outputs can be set as constant current regardless of the supply voltage varied.
- Two PWM playing ports. Drive speaker or buzzer directly.
- Body define: 3, 7, 14 seconds. (Total ROM size : 18k,42k,84k)
- voice length(3s body:16384*5,7s body:40960*5,14s body:83968*5)
- Voice algorithm: 5-bits LOG_PCM
- External resister for system frequency
- Sixteen default sampling frequencies are supported. The default frequencies can be changed by applying an external resistor.
- Support single key play on/off. (For OKY, TG0, TG1)
- Programmable only pull-low input. (For OKY,TG3)
- Programmable pull-high, pull-low or floating input. (For TG0,TG1)
- TG3_OPC pin can option as input or output by mask option

General Description

The AVXX32E -A are series of single-chip synthesizing CMOS VLSI IC which synthesizes voice by LOG_PCM algorithm. Table programming and shared multiple I/O pins make the applications flexible.

Powerful functions and pure speech architecture make the AVXX32E -A series are able to best fit most speech applications and a best cost/performance ratio as a result.

The programming of the AVXX32E -A series is first to define words. Each word contains voice data (or mute length), output method, assemble the words into sentences first, and then the programmer can assign the sentences to the keys corresponding to the user inputs.

The TG3_OPC pin of the AVXX32E -A series is multiplexed. This means it can option as input pin or output pin.

Body Option Table

Body	ROM	Table	KEY	OUT
AV0332E	84K	D0 – 3FF	OKY, TG0 – TG1 & TG3	OPA, OPB, OPC
AV0732E	42K	D0 – 2FF	OKY, TG0 – TG1 & TG3	OPA, OPB, OPC
AV1432E	18K	D0 – 1FF	OKY, TG0, TG3	OPA, OPC

Pin Description

Pin Name	I/O	Description
VDD	Power	Positive power supply
TEST	In	Test enable pad, high-active, pull-low
OSC	In	With resister connected to VDD for system clock generating
OKY	In	Trigger input, active-high, with internal pull_low resistor. Can define as sequential key or random key.
TG0, TG1	In	Trigger input, active-high with internal pull_low resistor.
TG3_OPC	In	Trigger input, active-high
	Out	Status output
OPB	Out	Status output
OPA	Out	Status output
PWM1, PWM2	Out	Voltage output to drive speaker or buzzer
VSS	Power	Negative power supply

Absolute Maximum Rating

Symbol	Rating	Unit
V_{DD}~V_{SS}	-0.5 ~ +0.5	V
V_{IN} (for input)	V_{SS}-0.3 < V_{IN} < V_{DD}+0.3	V
V_{OUT} (for all outputs)	V_{SS} < V_{OUT} < V_{DD}	V
T (operating)	-10 ~ +60	℃
T (storage)	-55 ~ +125	℃

DC Characteristics

Symbol	Parameter		Min	Typ.	Max	Unit	Condition
V_{DD}	Operating Voltage		2.4	3.0	5.0	V	
Isb	Supply Current	Standby	—	—	1	μA	V_{DD}=3.0V, I/O open
Iop		Operating	—	—	400	μA	V_{DD}=3.0V, No loading
I_{OL}	OPA, OPB source Current		—	–20	—	mA	V_{DD}=3.0V, V_{IP}=2.7V
Ioh	OPA, OPB sink Current		—	20	—	mA	V_{DD}=3.0V, V_{OP}=0.3V
d F/F	Frequency Variation by diff. lot		—	—	±10	%	V_{DD}=4.5V f_{OSC} =384kHz

Function Diagram

1. OPA/B/C (1:0) are the output options.

Output	Option	0(00)	1(01)	2(10)	3(11)
OPA	Status	BH	DL	SH	DH
	LED	+Fast	+Slow	Dy07	OFF
OPB	Status	BH	DL	SH	DH
	LED	-Fast	-Slow	Dy09	ON
OPC	Status	BH	DL	BL	DH
	LED	+Fast	+Slow	ON	OFF

Status output mode:

SH: Single pulse output, hi-level output

BH: Busy output, hi-level output

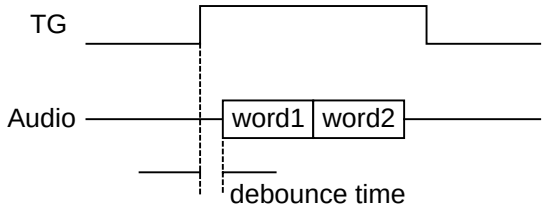
BL: Busy output, lo-level output
DH: Always Hi-level output
DL: Always Lo-level output

LED output mode:
+Fast, -Fast: High frequency alternate output
+Slow, -Slow: Low frequency alternate output
Dy09: Volume level (9/10)output control. If code > 9/10(FFh), then output “Lo”. Otherwise output “Hi”
Dy07: Volume level (7/10)output control. If code > 7/10(FFh), then output “Lo”. Otherwise output “Hi”
ON : Always Lo-level output
OFF: Always Hi-level output
Note: The Status and LED mode is optioned by mask option.

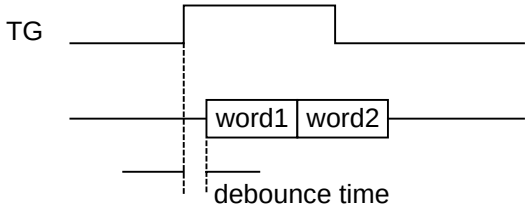
Edge/Level mode (If sentence = word1+word2)

- **Edge mode**

  Trigger length > Voice length

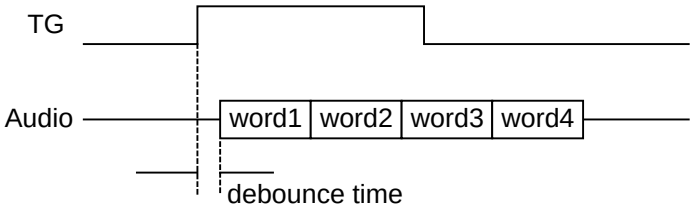


  Trigger length < Voice length

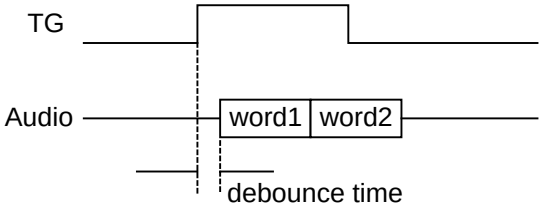


- **Level mode**

  Trigger length > Voice length (if sentence=word1+word2)

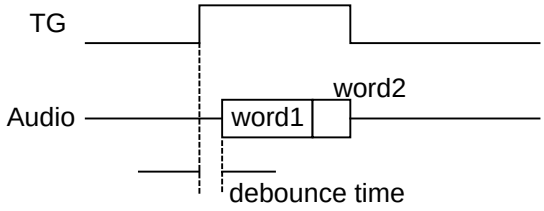


  Trigger length < Voice length (if sentence = word1+word2)

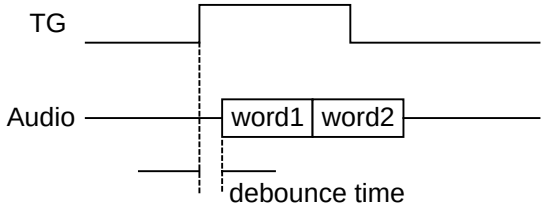


Hold/Unhold mode (If sentence = word1+word2)

- **Hold mode**

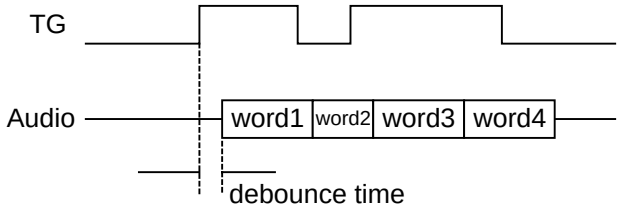


- **Unhold mode**

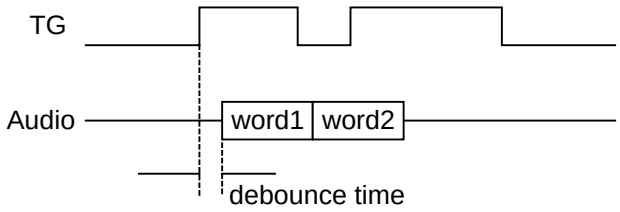


Retrigger/Irretrigger mode (If sentence = word1+word2)

- **Retrigger mode (Edge Unhold mode)**

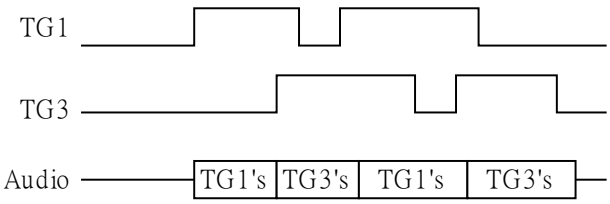


- **Irretrigger mode (Edge, Unhold mode)**



Last key priority

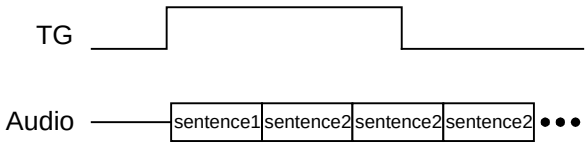
- **If TG1, TG3 are retrigger mode**



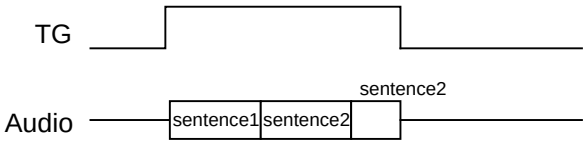
Looping function

If sentence is set to looping mode (sentence1_sentence2)

- **Unhold mode**

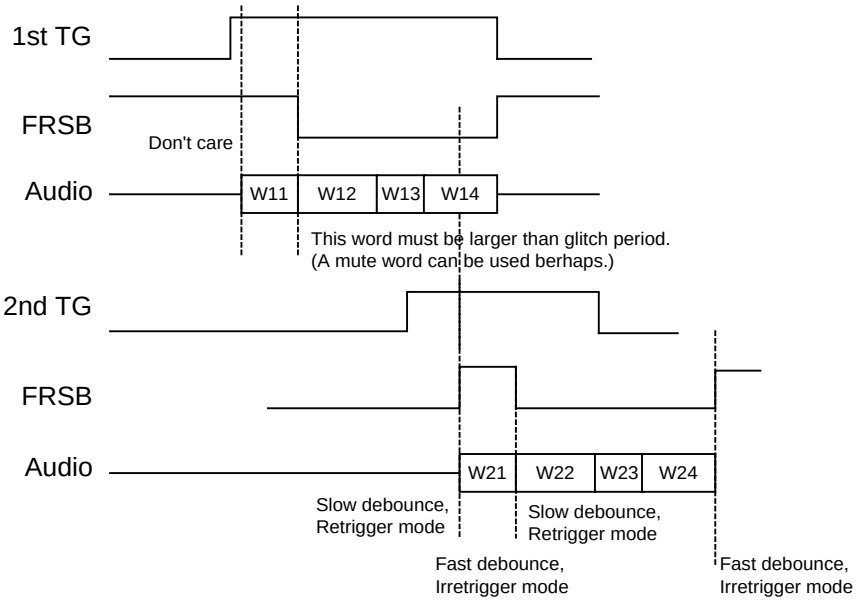


- **Hold mode**



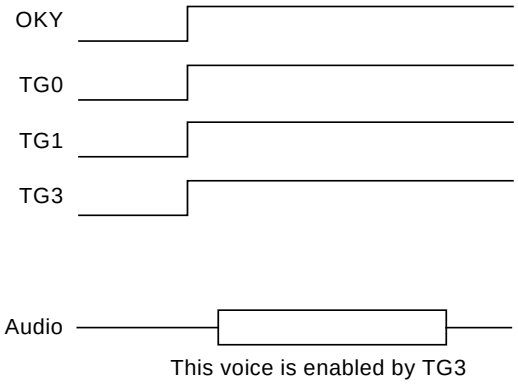
Force to retrigger and slow debounce option

(Trigger mode set to Fast debounce and Irretrigger mode)



Busy=0, FRSB set to high;
Busy=1, depending on FRSB setting.
If FRSB=0, force to slow debounce and retrigger mode;
If FRSB=1, no change (fast debounce and irretrigger mode).

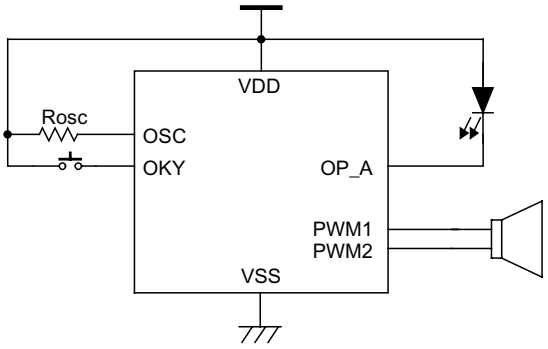
Stand-alone trigger inputs are enabled at the same time



Trigger input priority is TG3 > TG1 > TG0 > OKY

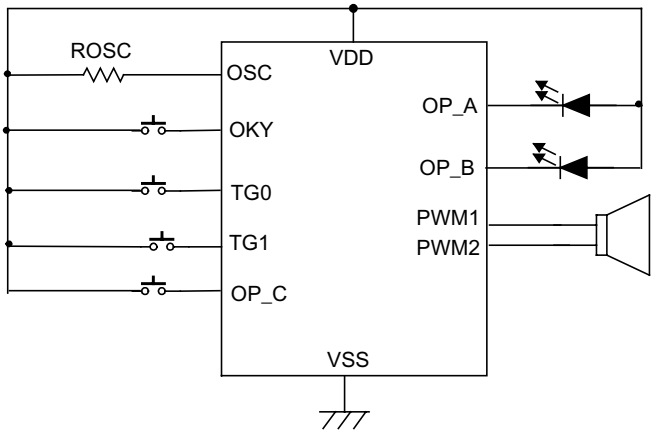
Application circuit

- **External resister, Driver speaker by PWM, driver LED**



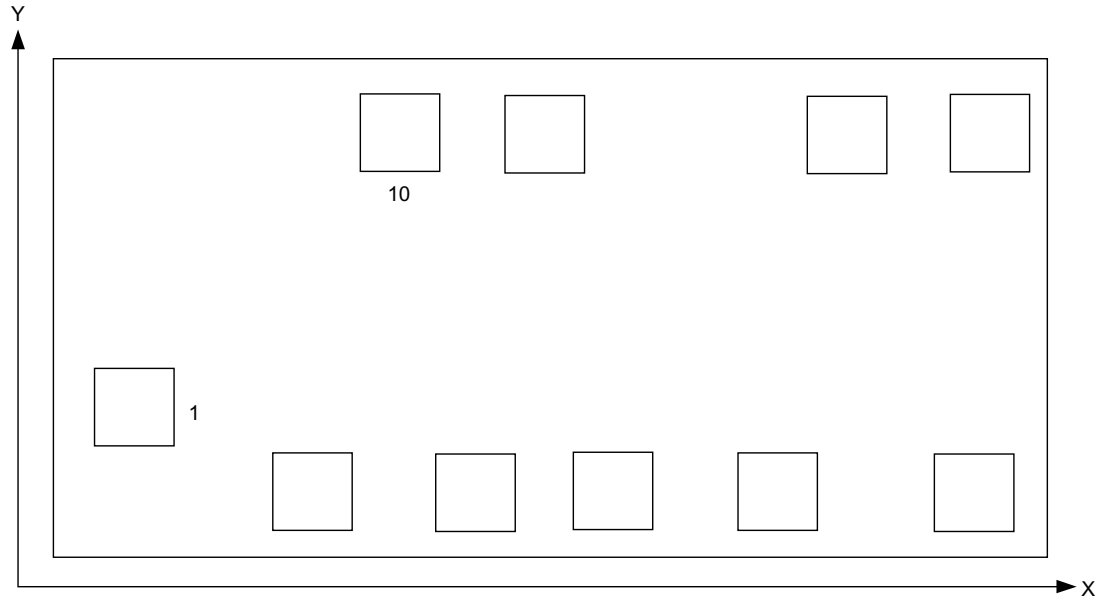
R_{OSC}=200kΩ for frequency option 8

- **Direct Keys**



- **Pad Diagram & Pad Location**

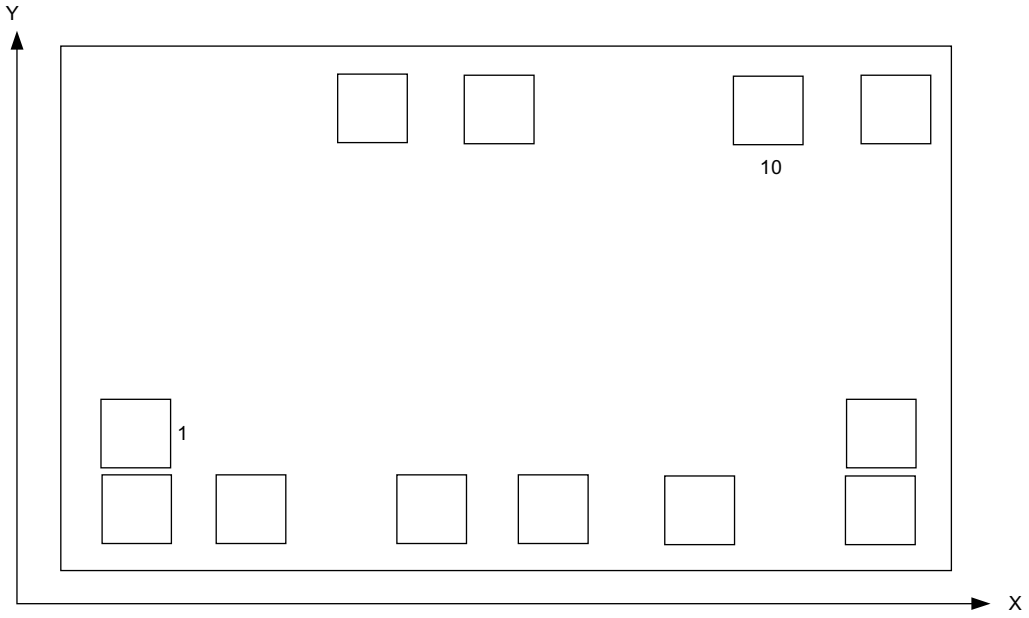
(1) AV0332E



Note: The IC substrate should be connect to VSS

Pad No.	Pad Name	X(um)	Y(um)	Pad No.	Pad Name	X(um)	Y(um)
1	PAD_OSC	108.75	214.05	6	PAD_TG0	1281.1	94.05
2	PAD_OKY	356.2	94.05	7	VDD	1302.8	595.6
3	PAD_OPA	586.1	94.05	8	PAD_PWM2	1101.9	595.6
4	PAD_TG3OPC	777.4	94.05	9	PAD_PWM1	681.1	595.6
5	PAD_TEST	1007.3	94.05	10	VSS	480.2	595.6
Chip size : 1387.9 x 696.6 (μm)^2							

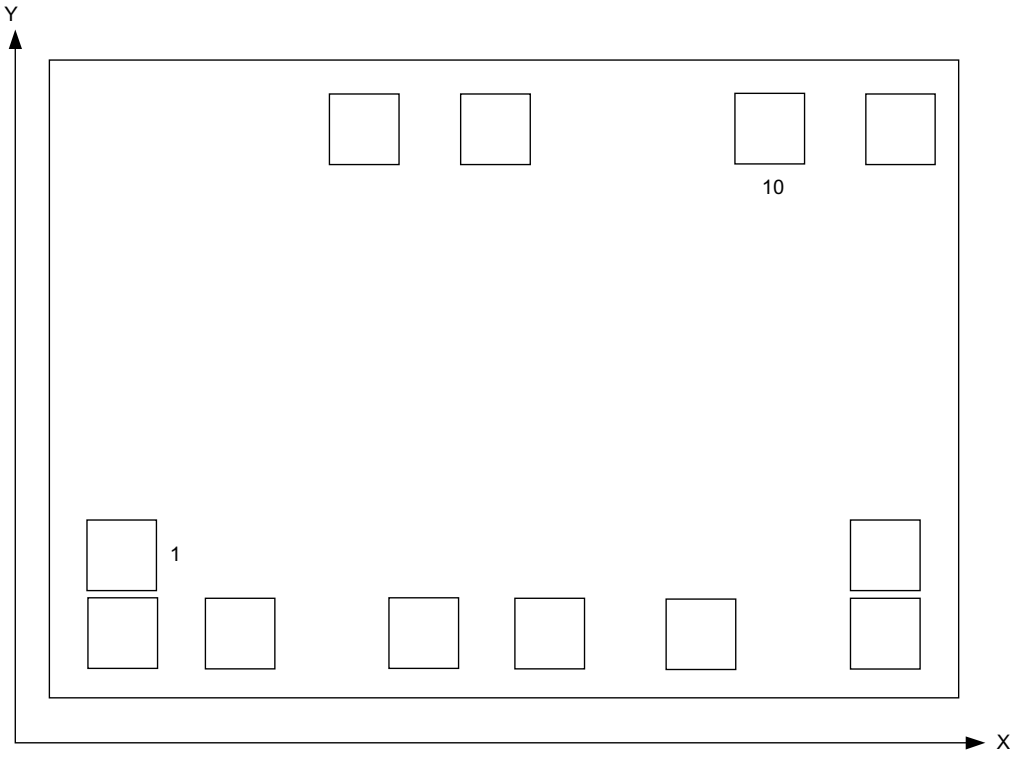
(2) AV0732E



Note: The IC substrate should be connect to VSS

Pad No.	Pad Name	X(um)	Y(um)	Pad No.	Pad Name	X(um)	Y(um)
1	PAD_OSC	108.75	214.05	7	PAD_TG1	1279.15	94.05
2	PAD_OKY	108.75	94.05	8	PAD_TG0	1279.15	214.05
3	PAD_OPA	291.65	94.05	9	VDD	1302.8	722.3
4	PAD_OPB	573.45	94.05	10	PAD_PWM2	1101.9	722.3
5	PAD_TG3OPC	764.75	94.05	11	PAD_PWM1	681.1	722.3
6	PAD_TEST	994.65	94.05	12	VSS	480.2	722.3
Chip size : 1387.9 x 823.3 $(\mu m)^2$							

(3)AV1432E



Note: The IC substrate should be connect to VSS

Pad No.	Pad Name	X(um)	Y(um)	Pad No.	Pad Name	X(um)	Y(um)
1	PAD_OSC	108.75	214.1	7	PAD_TG1	1279.2	94.05
2	PAD_OKY	108.75	94.05	8	PAD_TG0	1279.2	214.1
3	PAD_OPA	291.65	94.05	9	VDD	1302.8	867
4	PAD_OPB	573.45	94.05	10	PAD_PWM2	1101.9	867
5	PAD_TG3OPC	764.75	94.05	11	PAD_PWM1	681.1	867
6	PAD_TEST	994.65	94.05	12	VSS	480.2	867
Chip size : 1387.9 x 968 (μm)^2							