J105 SERIES
N-Channel JFETs

The J105 Series are high-performance JFET analog switches designed to offer low on-resistance and fast switching. $r_{DS(ON)}$ <3 Ω is guaranteed with the J105 which makes this device the lowest of any commercially available JFET. The J105 Series devices are housed in a low-cost TO-92 package and offer a wide range of tape and reel options. (See Section 7.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (pA)	t_{ON} MAX (ns)
J105	-10	3	10	14
J106	-6	6	10	14
J107	-4.5	8	10	14

For further design information please consult the typical performance curves NVA.

TO-92 (TO-226AA) **BOTTOM VIEW**

1 DRAIN
2 SOURCE
3 GATE

SIMILAR PRODUCTS

- TO-52, See U290 Series
- Chips, See NVA Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	50	mA
Power Dissipation (Case 25°C)	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature Range	T_J	-55 to 135	°C
Storage Temperature Range	T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

4

SPECIFICATIONS[a]			LIMITS							
				J105		J106		J107		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 1 µA		-4.5	-10	-2	-6	-0.5	-4.5	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		500		200		100		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.02		-3		-3		-3	
		T_A = 125°C	-10							
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 25 mA	-0.01							nA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 5 V, V_{GS} = -10 V	0.01		3		3		3	
		T_A = 125°C	5							
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA			3		6		8	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 25 mA f = 1 kHz	55							mS
Common-Source Output Conductance	g_{os}		5							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA f = 1 kHz			3		6		8	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V f = 1 MHz	120		160		160		160	
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = -10 V f = 1 MHz	20		35		35		35	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 25 mA f = 1 kHz	3							$nV/\sqrt{Hz}$
SWITCHING										
Turn-On Time	$t_{d(ON)}$	V_{DD} = 1.5 V, $V_{GS(ON)}$ = 0 V	6							
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	8							
Turn-Off Time	$t_{d(OFF)}$	J105 28mA -12V 50Ω J106 27mA -7V 50Ω J107 26mA -5V 50Ω	5							ns
	t_f		9							

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.