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## PRELIMINARY CUSTOMERPROCUREMENTSPECIFICATION

# Z86C60/65 CMOSZ8® 32KROMMICROCONTROLLER

## **FEATURES**

Part	ROM (KB)	RAM* (Bytes)	I/O	Speed (MHz)	28-pin DIP		
Z86C60	16	256	22	16	Х		
Z86C65	32	256	22	16	Х		
*Comonal Du	*Conservat Deservation						

\*General-Purpose

- 28-Pin DIP Package
- 3.0V to 5.5V Operating Range
- Low-Power Consumption: 200 mW
- Fast Instruction Pointer: 0.75 µs @ 16 MHz
- Two Standby Modes: STOP and HALT

#### **GENERAL DESCRIPTION**

The Z86C60/65 microcontrollers introduce a new level of sophistication to single-chip architecture. The Z86C65 is a member of the Z8 single-chip microcontroller family with 32 Kbytes of ROM and 256 bytes of RAM. The Z86C60 is identical, except that it only has 16 Kbytes of ROM.

The Z86C60/65 are housed in a 28-pin DIP package, and manufactured in CMOS technology. The Z86C96 ROMless Z8 will support the Z86C60/65.

Zilog's CMOS microcontroller offers fast execution, more efficient use of memory, more sophisticated interrupts, input/output bit manipulation capabilities, and easy hard-ware/software system expansion along with low cost and low power consumption.

The Z86C60/65 architecture is characterized by Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

For applications which demand powerful I/O capabilities, the Z86C60/65 fulfills this with 22 pins dedicated to input

- Low EMI Mode Option
- Auto Latches
- Two Programmable 8-Bit Counter/Timers Each with 6-Bit Programmable Prescaler
- Three Vectored, Priority Interrupts from Three Different Sources
- On-Chip Oscillator that Accepts a Crystal Ceramic Resonator, LC, or External Clock Source
- ROM Mask Options:
  - ROM Protect
  - RAM Protect

and output. These lines are grouped into four ports. Each port is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are three basic address spaces available to support this wide range of configurations: Program Memory, Data Memory, and 236 General-Purpose Registers.

To unburden the program from coping with the real-time problems such as counting/timing and serial data communication, the Z86C60/65 offers two on-chip counter/timers with a large number of user selectable modes.

#### Notes:

All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V <sub>cc</sub>	V <sub>DD</sub>
Ground	GND	V <sub>SS</sub>

## **GENERAL DESCRIPTION**



Figure 1. Z86C60/65 Functional Block Diagram

## **PIN DESCRIPTION**



#### Z86C60/65 28-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	V <sub>cc</sub>	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	/RESET	Reset	Input
5	/DS	Data Strobe	Output
6	P35	Port 3, Pin 5	Output
7	GND	Ground	Input
8-13	P05-P00	Port 0, Pins 0,1,2,3,4,5	In/Output
14-21	P17-P10	Port 1, Pins 0,1,2,3,4,5,6,	7 In/Output
22-26	P25-P21	Port 2, Pins 1,2,3,4,5	In/Output
27	P31	Port 3, Pin 1	Input
28	P36	Port 3, Pin 6	Output

Figure 2. Z86C60/65 28-Pin DIP Pin Assignments

## ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Мах	Units
V <sub>CC</sub> T <sub>STG</sub> T <sub>A</sub>	Supply Voltage* Storage Temp Oper Ambient Temp	$-0.3 \\ -65 \\ \dagger$	+7.0 +150 †	V C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

#### Notes:

\* Voltages on all pins with respect to GND.

† See ordering information

## STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load).



Figure 3. Test Load Diagram

#### **DC ELECTRICAL CHARACTERISTICS** Z86C60/65

		$T_A = t_0 + t_0$	0°C 70°C	Typical at		
Sym	Parameter	Min	Max	25°C	Units	Conditions
V <sub>m</sub>	OperatingVoltage	4.5	5.5		V	[3]
ŵ	MaxInputVoltage		7		V	[3]Ι <sub>IN</sub> <250μΑ
V <sub>сн</sub>	ClockInputHighVoltage	0.85V <sub>cc</sub>	V <sub>cc</sub> +0.3		V	DrivenbyExternalClockGenerator
Va	ClockInputLowVoltage	V <sub>ss</sub> -0.3	0.8		V	DrivenbyExternalClockGenerator
V <sub>H</sub>	InputHighVoltage	2	V <sub>cc</sub> +0.3		V	
V,	InputLowVoltage	V <sub>SS</sub> -0.3	0.2V		V	
Ч	OutputHighVoltage	24	V <sub>cc</sub>		V	I <sub>он</sub> =2.0mА
V	OutputHighVoltage		V <sub>cc</sub> -100mV		V	I <sub>04</sub> =–100μA
V <sub>й</sub>	OutputHighVoltage(LowEMI)	24			V	$I_{OH}^{i} = -0.5 \text{mA}$
٧ <sub>0</sub> ΄	OutputLowVoltage		0.4		V	$I_{0}^{-}$ = +5.0 mA[2]
Va	OutputLowVoltage(LowEMI)		0.4		V	$I_{0} = +2.0 \text{ mA}[2]$
V <sub>RH</sub>	ResetInputHighVoltage	$0.85V_{cc}$	V <sub>cc</sub> +0.3		V	
VR	ResetInputLowVoltage	-0.3	0.2V <sub>cc</sub>		V	
I,	InputLeakage	-2	2		μA	V <sub>IN</sub> =0V,V <sub>CC</sub>
l <sub>a-</sub>	OutputLeakage	-2	2		μA	V <sub>IN</sub> =0V,V <sub>CC</sub>
l <sub>R</sub>	ResetInputCurrent		-180		μA	V <sub>RL</sub> =0V
l <sub>cc</sub>	SupplyCurrent(StandardMode)		35	24	mA	[1]@16MHz
l <sub>cc</sub>	SupplyCurrent(LowEMI)		6.0	<u>4.</u> 0	mA	@4MHz
	StandbyCurrent(StandardMode)		15	4.5	mA	[1]HALTModeV <sub>IN</sub> =0V,V <sub>cc</sub> @16MHz
	StandbyCurrent(LowEMI)		1.6	0.8	mA	@4MHz
L CC2	StandbyCurrent		10	5	μA	[1]STOPModeV <sub>IN</sub> =0V,V <sub>CC</sub>
ALL	AutoLatchLowCurrent	-14	+14	5	μA	$V_{cc}=5.0V$

#### Notes:

[1] All inputs driven to either 0V or  $V_{cc}$ , outputs floating. [2]  $V_{cc} = 4.5V$  to 5.5V [3] /Reset pin must be a maximum of  $V_{cc} + 0.3V$ .



## **AC CHARACTERISTICS**

Additional Timing Diagram





## **AC CHARACTERISTICS**

Additional Timing Table Z86C60/65 (Standard Mode Only)

No	Symbol	Parameter	T <sub>A</sub> = ( to +7( 16 M Min	D°C 0°C Hz Max	Units	Notes
1	ТрС	Input Clock Period	62.5	DC	n s	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		10	n s	[1]
3	TwC	Input Clock Width	ut Clock Width 31		n s	[1]
4	TwTinL	Timer Input Low Width	75		n s	[2]
5	TwTinH	Timer Input High Width	5 TpC		n s	[2]
6	TpTin	Timer Input Period	8 TpC		n s	[2]
7	TrTin,TfTin	Timer Input Rise and Fall Times	100		n s	[2]
8 a	TwIL	Interrupt Request Input Low Times	est Input Low Times 70		n s	[2,4]
8 b	TwIL	Interrupt Request Input Low Times	5 TpC		n s	[2,5]
9	TwIH	Interrupt Request Input High Times	5 TpC		n s	[2,3]

#### Notes:

- [1] Clock timing references use  $0.85V_{\rm CC}$  for a logic 1 and 0.8V for a logic 0. [2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
- [3] Interrupt references request through Port 3.
- [4] Interrupt request through Port 3 (P33-P31).
- [5] Interrupt request through Port 30.

#### **Pre-Characterization Product:**

The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-con-

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