Integrated Device Technology, Inc.

SELF-TIMED BiCMOS ECL STATIC RAM 64K (16K x 4-BIT) STRAM

PRELIMINARY
IDT10496LL
IDT100496LL
IDT101496LL

FEATURES:

- 16,384-words x 4-bit organization
- Self-Timed Write, with latches on inputs and latches on outputs
- Balanced Read/Write cycle time: 13/15ns
- Access time: 10/12 ns (max.)
- Fully compatible with ECL logic levels
- Through-hole DIP and surface-mount packages

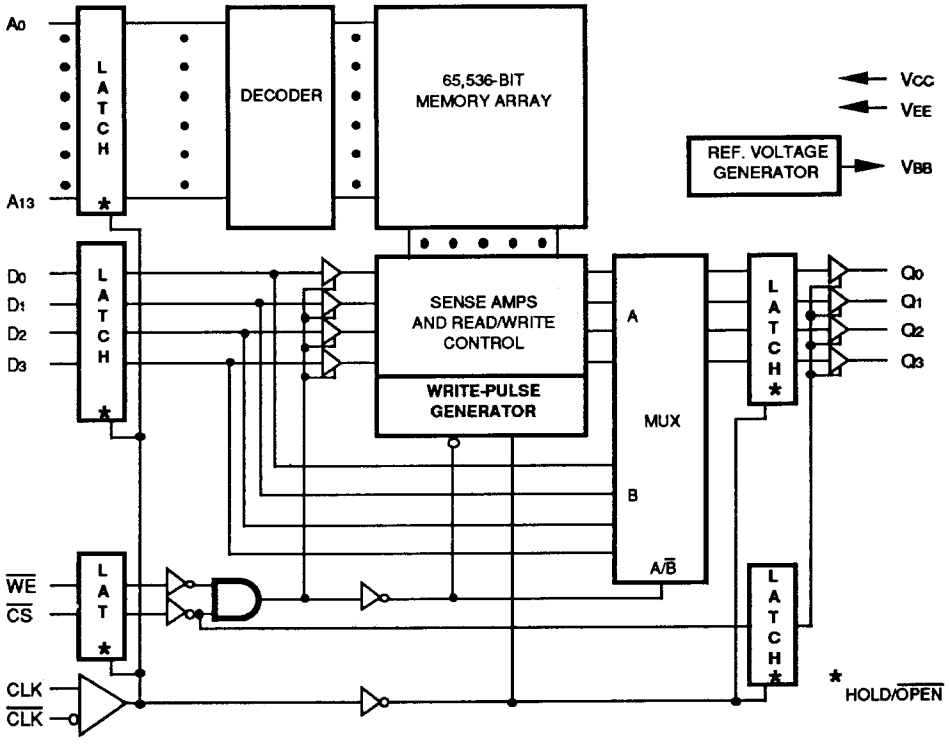
DESCRIPTION:

The IDT10496LL, IDT100496LL and IDT101496LL are 65,536-bit high-speed BiCEMOS™ ECL static random access memories organized as 16K x 4, with inputs and outputs fully compatible with ECL levels. Clocked level-sensitive latches on inputs and outputs, and the self-timed write operation, provide enhanced system performance over conventional RAMs, providing easier design and improved system level cycle times.

Inputs can flow into the device and then are latched by the leading edge of an externally supplied differential clock. The small input valid window required means more margin for system skews. Logic-to-memory propagation delay is included in device cycle time calculation, allowing this device to deliver better system performance than asynchronous SRAMs and glue logic.

Write timing is controlled internally based on the clock. Write Enable has no special requirements. The device allows balanced read and write cycle times, and reads and writes can be inserted in any order.

FUNCTIONAL BLOCK DIAGRAM



2768 drw 01

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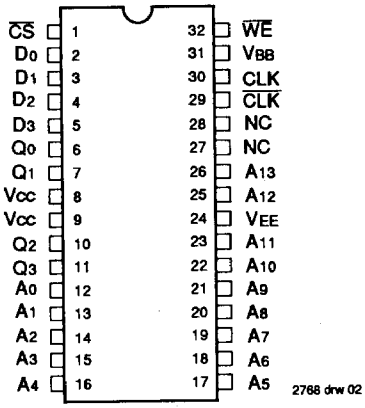
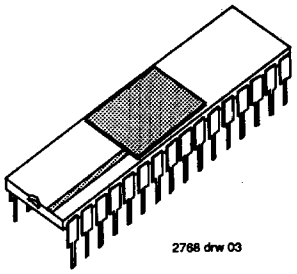
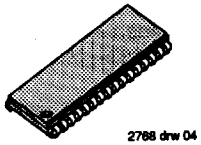
PIN CONFIGURATION



TOP VIEW



400-Mil-Wide
CERAMIC PACKAGE
C32



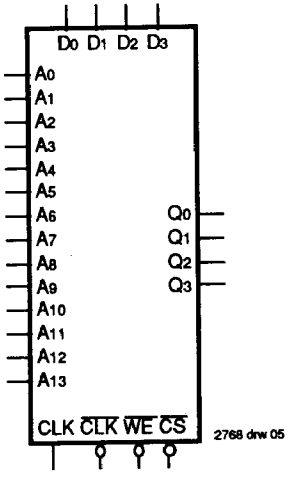
300-Mil-Wide
PLASTIC SOJ PACKAGE
Y32

PIN DESCRIPTION

Symbol	Pin Name
A0 through A13	Address Inputs
D0 through D3	Data Inputs
Q0 through Q3	Data Outputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
CLK, $\overline{CLK}$	Differential Clock Inputs
VBB	Reference Voltage Output (≈1.32V)
VEE	More Negative Supply Voltage
Vcc	Less Negative Supply Voltage
NC	No Connect - not internally bonded

2768 tbl 01

LOGIC SYMBOL



16Kx4
STRAM

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sec
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sec
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sec

2768 tbl 02

NOTE:
1. Referenced to Vcc

CAPACITANCE (TA=+25°C, f=1.0MHz)

Symbol	Parameter	DIP Typ.	DIP Max.	SOJ Typ.	SOJ Max.	Unit
CINCLK	Input Capacitance CLK/$\overline{CLK}$	6	–	3	–	pF
CIN	Input Capacitance except CLK/$\overline{CLK}$	4	–	3	–	pF
COUT	Output Capacitance	6	–	3	–	pF

2768 tbl 03

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	CLK	DataOUT(2)	Function
H	X	↑	L	Deselected
L	H	↑	RAM Data	Read
L	L	↑	WRITE Data	Write

2768 tbl 04

NOTES:
1. H=High, L=Low, X=Don't Care
2. DATAOUT changes when CLK returns high.

ECL-10K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2768 tbl 05

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L =50Ω to -2.0V, T_A = 0 to +75°C for DIP, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	V_{IN} = V_{IHB} or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	V_{IN} = V_{IHB} or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs[2]		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs[2]		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	V_{IN} = V_{IHA}	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	V_{IN} = V_{ILB}	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open[2]		-260	-200	–	mA	–

2768 tbl 06

NOTES:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.
2. Except CLK and $\overline{CLK}$, one of which is tied low and one is tied high.

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ECL-100K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
VTERM	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
TA	Operating Temperature		0 to +85	°C
TBIAS	Temperature Under Bias		-55 to +125	°C
TSTG	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
PT	Power Dissipation		2.0	W
IOUT	DC Output Current (Output High)		-50	mA

2768 tbl 07

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(VEE = -4.5V, RL=50Ω to -2.0V, TA = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit
VOH	Output HIGH Voltage	VIN = VIHA or VILB		-1025	-955	-880	mV
VOL	Output LOW Voltage	VIN = VIHA or VILB		-1810	-1715	-1620	mV
VOHC	Output Threshold HIGH Voltage	VIN = VIHB or VILA		-1035	–	–	mV
VOLC	Output Threshold LOW Voltage	VIN = VIHB or VILA		–	–	-1610	mV
VIH	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs(2)		-1165	–	-880	mV
VIL	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs(2)		-1810	–	-1475	mV
I IH	Input HIGH Current	VIN = VIHA	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I IL	Input LOW Current	VIN = VILB	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
IEE	Supply Current	All Inputs and Outputs Open(2)		-240	-180	–	mA

2768 tbl 08

NOTES:

1. Typical parameters are specified at VEE = -4.5V, TA = +25°C and maximum loading.
2. Except CLK and $\overline{CLK}$, one of which is tied low and one is tied high.

ECL-101K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		2.0	W
I_{OUT}	DC Output Current (Output High)		-50	mA

NOTE: 2768 tbl 09

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-101K DC ELECTRICAL CHARACTERISTICS

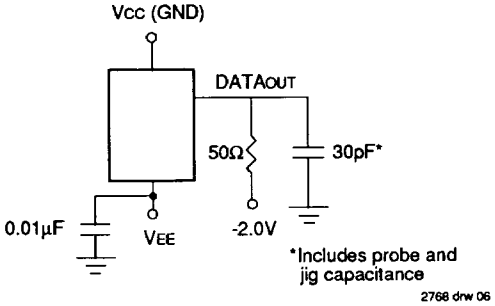
(V_{EE} = -5.2V, RL=50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs[2]		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs[2]		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open[2]		-260	-200	–	mA

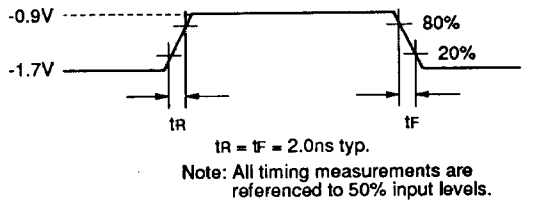
NOTES: 2768 tbl 10

1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.
2. Except CLK and $\overline{CLK}$, one of which is tied low and one is tied high.

LOAD CONDITION



INPUT PULSE



RISE/FALL TIME

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	–	–	2	–	ns
tF	Output Fall Time	–	–	2	–	ns

2770 tbl 11

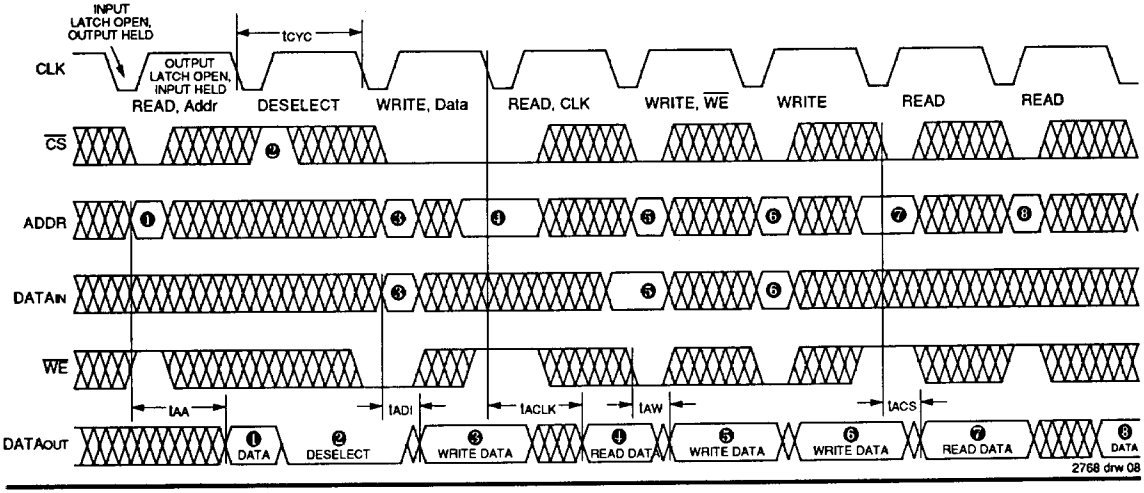
FUNCTIONAL DESCRIPTION

The IDT10496LL, IDT100496LL, and IDT101496LL Self-Timed BiCMOS ECL static RAMs (STRAM) provide high speed with low power dissipation typical of BiCMOS ECL. On-chip logic additionally helps improve system performance. The ECL-101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

As can be seen in the Functional Block Diagram on the title page, this device contains level-sensitive latches to sample and hold addresses, input data, and control status, and hold output data. Inputs are transparent while the clock (CLK) input is low (and $\overline{CLK}$ is high), and then hold their contents when the clock returns high. In the case of a write cycle, the memory cell is written during the clock-high time, and write data conducted to the outputs. Because the output latches are controlled by an inversion of the clock, output data flows out the output latch while clock is high and then is held into the next cycle during clock low.

The Latch-Latch architecture is most useful when read access data is needed within the same cycle that addresses settle. The input latch, when transparent, allows the access to begin as soon as addresses settle, allowing data to be ready somewhat sooner in the cycle than would be possible with a clocked-register implementation.

FUNCTIONAL DESCRIPTION TIMING EXAMPLE



READ TIMING

In a typical read cycle, the read address flows into the device while clock is low, as at ❶ below. Read access begins when the last address has settled. When clock returns high, the inputs are held so that addresses can begin to change for the next cycle.

Clock high also opens the output latches, so the read data for the read address clocked in at ❶ is gated through the output latch to the output pins. There is a short delay from rising clock to output ready, called t_{DR} (see Read Cycle Timing). If the clock-low time (t_{WL}) is shorter than the inherent access-time of the cell, output is guaranteed valid after the specified t_{AA}. But if t_{WL} is longer than the cell access-time, output data will be valid t_{DR} after clock goes high. Thus, the time it takes from address valid to data ready for any given address is

$t_{AA} = t_{AA}$ or $(t_{SA} + t_{DR})$,

whichever is larger. A permutation of this equation holds for each read and write access modes.

Because addresses and control lines (Write Enable and Chip Select) all must be stable for access to commence, there are two other read access modes, described as follows.

If addresses and controls are all stable before input latches are opened by clock going low, as at ❹ below, access begins on the low-going edge of clock. Data is available t_{ACLK} later, provided the output latch is opened by clock returning high.

If address and Write Enable are valid after clock-low, but Chip Select is last to go low, as at ❼ below, data is available t_{ACS} after the low-going edge of Chip Select.

The output latch takes some time to change state for the next cycle, but this time is very short. Therefore, data hold time from clock high (t_{DH}) is specified as zero minimum hold time.

DESELECT TIMING

Because the outputs are latched, they will continue to drive the output pins until a disable state is clocked through the device. The deselected state is achieved by de-asserting chip select ($\overline{CS}$ high) before clock returns high. This case occurs at ❷ below. Outputs then attain the disable state (low) t_{DR} later. Status of other inputs do not effect the disabling of the device when chip select is de-asserted with the proper relation to clock.

WRITE TIMING

Write cycles are identical to read cycles, except that write enable and write data need also be supplied, with the appropriate setup and hold timing. The device has on-chip timing that handles all aspects of writing data into the addressed RAM cell without the need for external write-pulse generation. The timing logic uses the clock-high time as the write pulse, and thus determines the minimum clock-high time, t_{WH}.

In addition to writing to the RAM cell, the write data is fed to the output register by a multiplexer, so that write data is available on the output pins after an access time. Thus the input data supplied at ❸ is available on the output t_{ADI} after the input data has settled, while the input data supplied at ❺ is available t_{AW} after Write Enable is asserted low. This function is sometimes called "Transparent Write," and is useful for write-through cache applications.

There are no restrictions on the order of read cycles and write cycles.

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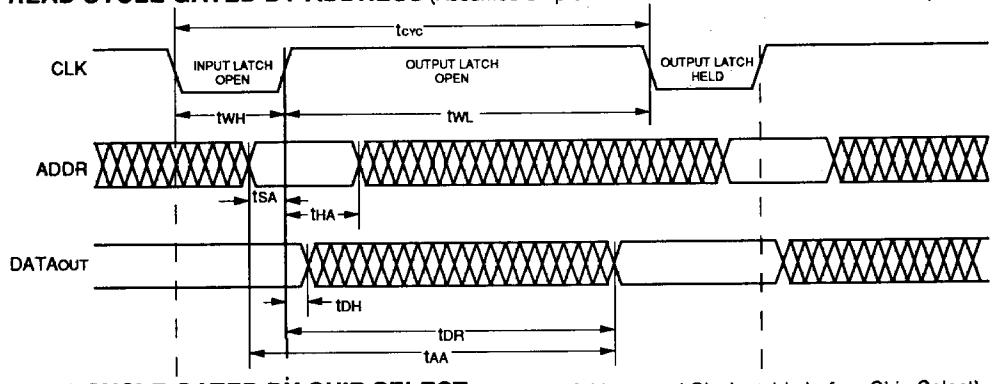
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10496LL13 100496LL13 101496LL13		10496LL15 100496LL15 101496LL15		Unit
			Min.	Max.	Min.	Max.	
Read Cycle							
tCYC	Cycle Time	–	13	–	15	–	ns
tAA[2]	Address Access Time	–	–	10	–	12	ns
tACS[3]	Chip Select Access Time	–	–	5	–	5	ns
tACLK[4]	Access Time from Clock Low	–	–	10	–	12	ns
tWL	Clock Low Pulse Width	–	3	–	3	–	ns
tWH	Clock High Pulse Width	–	10	–	12	–	ns
tSCS	Setup Time for Chip Select	–	1	–	1	–	ns
tSA	Setup Time for Address	–	1	–	1	–	ns
tHCS	Hold Time for Chip Select	–	2	–	2	–	ns
tHA	Hold Time for Address	–	2	–	2	–	ns
tDH	Data Hold from Clock Low	–	0	–	0	–	ns
tDR[5]	Data Ready from Clock Low	–	0	4	0	4	ns

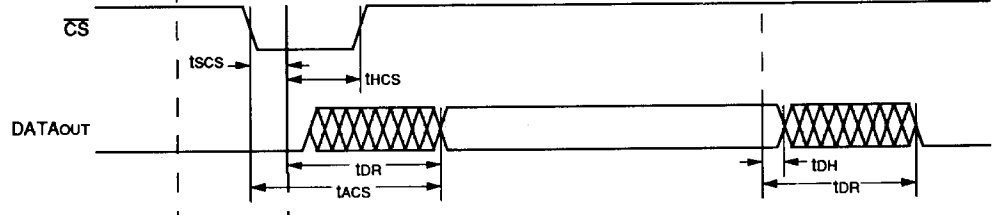
2768 tbl 12

NOTES:
1. Input and Output reference level is 50% point of waveform.
2. Read Cycle is gated by Address when tSA < tWL so that the access begins at the settling of Address. Access time is the larger of tAA or tSA + tDR.
3. Read Cycle is gated by Chip Select when tSCS < tWL so that access begins at the falling edge of Chip Select. Access time is the larger of tACS or tSCS + tDR.
4. Read Cycle is gated by Clock when tSA > tWL so that access begins at the falling edge of Clock. Access time is the larger of tACLK or tWL + tDR.
5. tDR(max) is specified when all other gating conditions have been satisfied, specifically, for READ cycle: when tSA > tAA(max) - tDR(max) and tSCS > tACS(max) - tDR(max) and tWL > tACLK(max) - tDR(max); for WRITE cycle: when tSD > tADI(max) - tDR(max) and tSWE > tAW(max) - tDR(max).

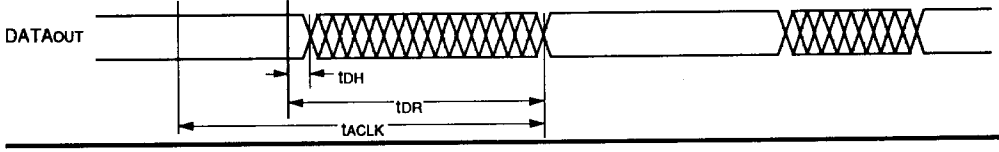
READ CYCLE GATED BY ADDRESS (Assumes Chip Select and Clock stable before Address)



READ CYCLE GATED BY CHIP SELECT (Assumes Address and Clock stable before Chip Select)



READ CYCLE GATED BY CLOCK (Assumes Address and Chip Select stable before Clock Low)



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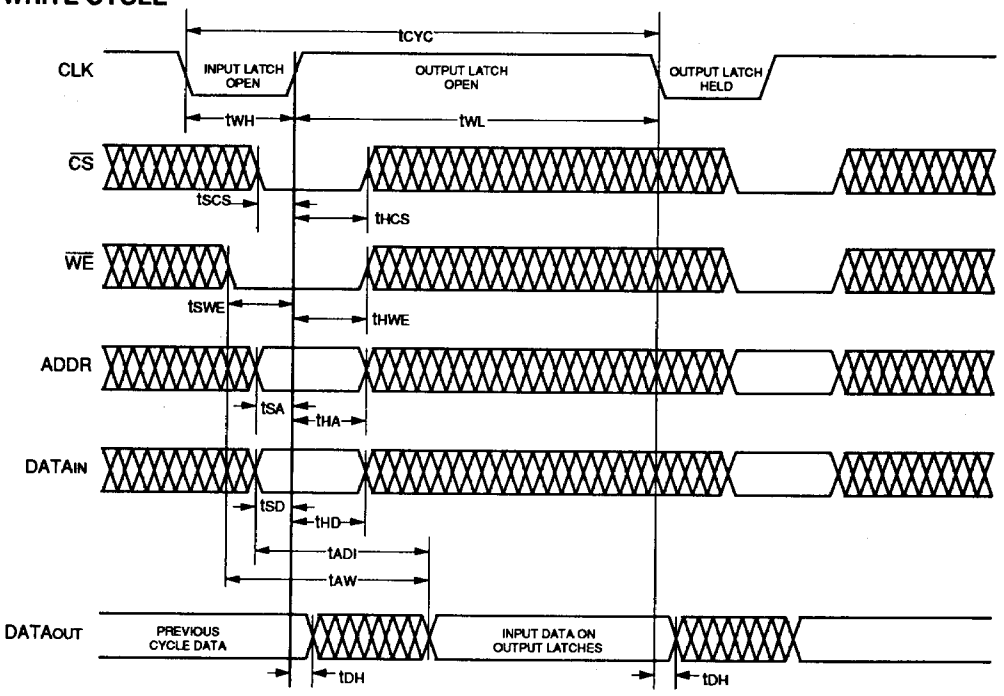
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10496LL13 100496LL13 101496LL13		10496LL15 100496LL15 101496LL15		Unit
			Min.	Max.	Min.	Max.	
Write Cycle[2]							
tAW[3]	Write Enable Low to Data Valid	–	–	5	–	5	ns
tADI[4]	Data In Valid to Data Out Valid	–	–	5	–	5	ns
tSWE	Setup Time for Write Enable	–	1	–	1	–	ns
tSD	Setup Time for Data In	–	1	–	1	–	ns
tHWE	Hold Time for Write Enable	–	2	–	2	–	ns
tHD	Hold Time for Data In	–	2	–	2	–	ns

NOTES:
2768 tbl 13

1. Input and Output reference level is 50% point of waveform.
2. All Setup, Hold, and Access timing are the same as the Read Cycle with the addition of above requirements. Write Data appears on output pins after rising edge of clock.
3. Access time is the larger of tAW or tSWE + tDR.
4. Access time is the larger of tADI or tSD + tDR.

WRITE CYCLE



2768 drw 10

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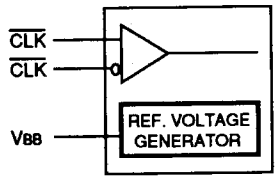
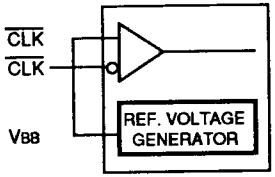
CLOCK INPUT

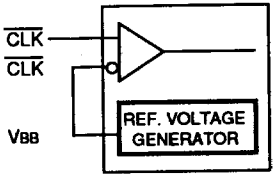
The clock input circuit has been designed to accomodate both single-ended and differential mode operation. Differential mode exhibits better common-mode noise rejection and is obtained by driving both true and complement clock lines with a differential driver, as shown in Figure (a). Single-ended operation is achieved as either falling-edge-active or rising-edge-active, as shown in Figures (b) and (c), respectively. VBB is designed to drive clock input only and is not intended to be used for any other purpose.



(a) Differential Mode



(b) Falling-Edge-Active Single-Ended Mode



(c) Rising-Edge-Active Single-Ended Mode

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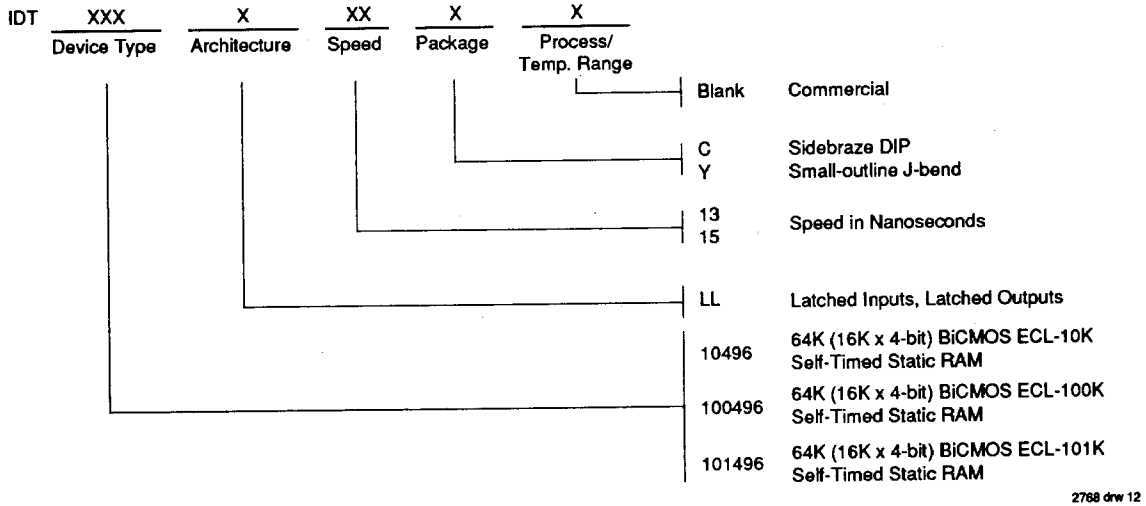
ORDERING INFORMATION



2768 drw 12