OAT1049x-V5-z-yy (for 80km)

OC-192/STM-64 SERDES Transceiver Module

Document Number	**OPS-0302-006**
Revision	**DRAFT 0.4**
DATE	**Oct.17, 2002**
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Modification History

Rev.	Date	Originator	Comment
DRAFT0.1	**Apr.28, 2002**	***T.ITOU***	
DRAFT0.2	**May30, 2002**	***T.ITOU***	Revision of "Block Diagram"
DRAFT0.3	**Aug.19, 2002**	***Y.FUJISAKU***	Revision of "Block Diagram" and "Specifications" Addition of "Absolute Maximum Ratings", "Operating Environment", "Mechanical Information", "Connector Pinout", "Precautions for Handling", "Qualifications and Reliability" and "Laser Safety"
DRAFT0.4	**Oct.17, 2002**	***Y.FUJISAKU***	Revision of "Block Diagram", "Operation Environment", "Specifications", "Connector Pinout" and "Ordering Information"

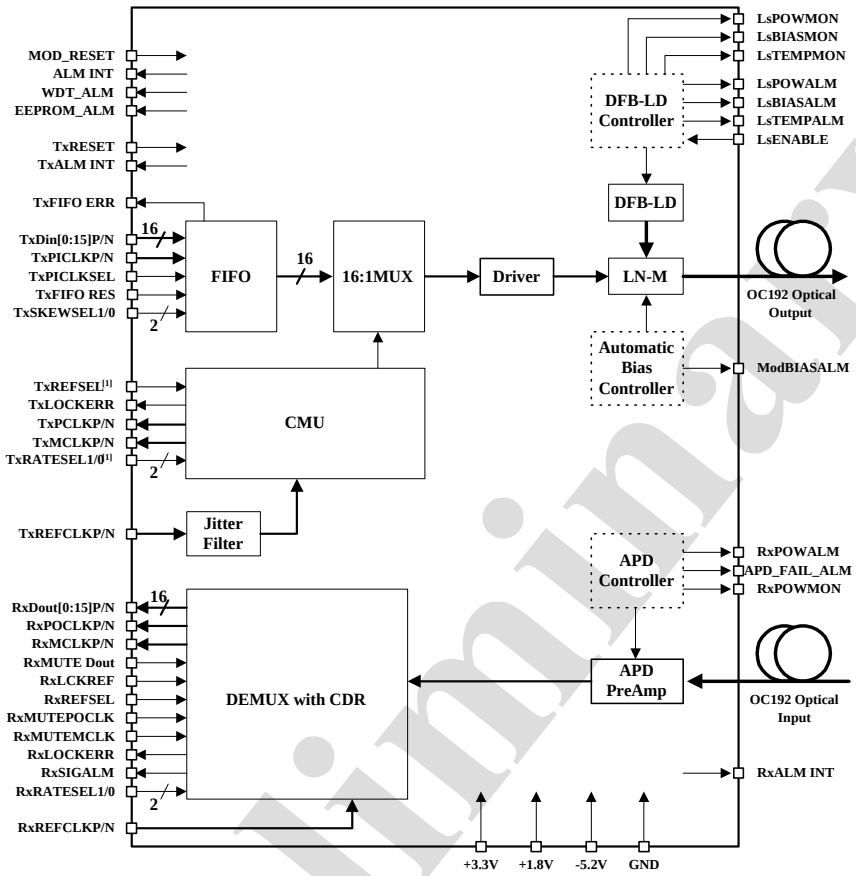
Features ;

- SONET/SDH 9.95328Gbit/s Operation
- Support 10.3Gbit/s(10GbE), 10.66Gbit/s(FEC) and 10.7Gbit/s(OTN) Rate
- Minimum Sensitivity: < -22dBm
- Optical Output Power: +2 to +6dBm
- Wavelength: 1550nm Band
- Transmission Distance: 80km(1600ps/nm)
- Dispersion Penalty: <2dB
- 16-Bit Parallel 622.08Mbit/s (Equivalent FEC Rate) LVDS Data Interface
- SERDES Timing Compliant with OIF1999.102.8 SFI-4 Interface
- Jitter Filter Built-in (Except for Multi-Rate Type)
- Compact Size: 88.9 × 114.3 × 17.5 (mm)
- Supply Voltage: +3.3V, +1.8V and -5.2V
- Low Power Consumption: < 9W max. (6W typ.)

Applications ;

- Metro Network SONET/SDH Systems
- 10 Gigabit Ethernet Systems
- Forward Error Correction Systems
- Optical Transport Network (OTN) Systems

1.Block Diagram



Note[1]: TxREFSEL and TxRATESEL1/0 are available for multi-rate type, OAT1049x-V5-C-yy

Figure 1.1 Block Diagram

2.Absolute Maximum Ratings

Table 2.1 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	Vcc	-0.5	+3.8	V
	Vdd	-0.5	+2.0	V
	Vee	-5.75	+0.5	V
LVDS Output Pin		0	+2.0	V
LVTTL Output Pin		0	+3.6	V
Optical Input Power	Pin	—	+3	dBm
Tension of Fiber		—	500	gf
Fiber Bending Radius		25	—	mm
Storage Temperature	Tstg	-40	85	°C

3.Operating Environment

Table 3.1 Operating Environment

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	3.13	3.3	3.46	V
	Vdd	1.71	1.8	1.89	V
	Vee	-5.46	-5.2	-4.94	V
Supply Current	Icc	—	0.7	1.6	A
	Idd	—	0.8	0.9	A
	Iee	—	0.4	0.5	A
Case Temperature	Tc	0	—	70	°C
Power Consumption		—	6	9	W

4.Specifications

4-1 Optical Interfaces

Table 4.1.1 Optical Interfaces

Parameter	Symbol	Min.	Max.	Unit	Note
Transmitter					
Optical Output Power	Pout	+2	+6	dBm	
Optical Waveform		OC-192/STM-64 Unamplified Mask Standard			See Figure 4.1.1
Center Wavelength	λc	1530	1565	nm	
Extinction Ratio	Er	10	—	dB	
Spectral Maximum –20dB Width	$\Delta\lambda_{20}$	—	1.0	nm	
Side Mode Suppression Ratio	SMSR	35	—	dB	
Receiver					
Minimum Sensitivity	Pin	—	-22	dBm	BER=1x10^{-12}
Minimum Overload	Pin	-5	—	dBm	@PRBS2^{31}-1
Input Wavelength	λc_rx	1280	1580	nm	
Rx Return Loss		27	—	dB	
Jitter Performance					
Jitter Generation		—	0.1	UIp-p	Bandpass filter; 50k to 80MHz
Jitter Tolerance and Transfer		Compliant with GR-253			See Figure 4.1.2, 4.1.3
Optical Path					
Dispersion	D_{Lrmax}	—	1600	ps/nm	
Optical Path Penalty		—	2	dB	

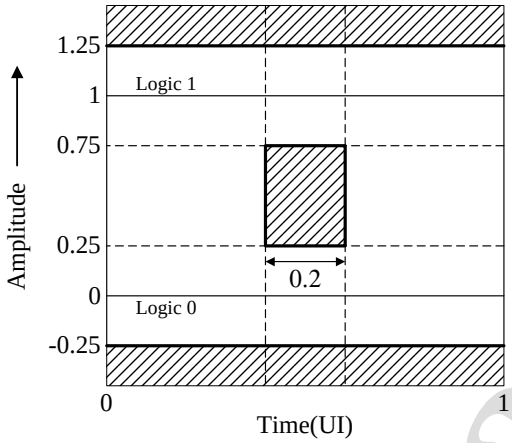


Figure 4.1.1 Eye Pattern Mask

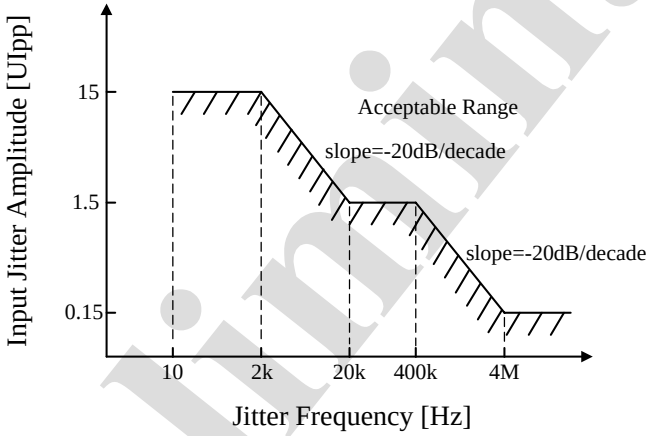


Figure 4.1.2 Jitter Tolerance Mask

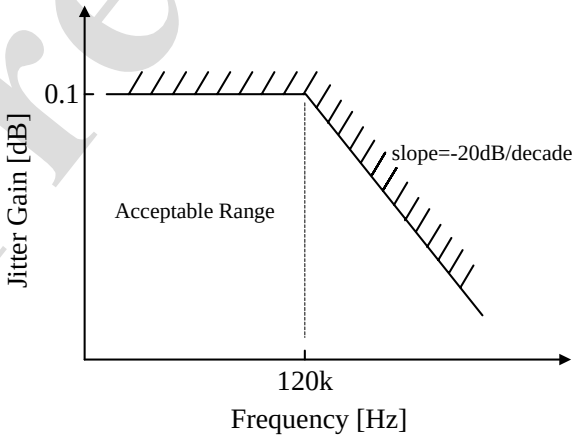


Figure 4.1.3 Jitter Transfer Mask

4-2 Electrical Interfaces

Table 4.2.1 Reference Clock Characteristics

Name	Parameter	Min.	Typ	Max.	Unit	Logic	Notes
Transmitter Reference Clock							
TxREFCLKP/N	Frequency		622.08		MHz	AC Coupled	OC-192/STM-64
			155.52[2]				
			644.53				10GbE
			161.13[2]				
			666.51				FEC
			166.63[2]				
			669.33				OTN
			167.33[2]				
			155.52/161.13/166.63/167.33 or 622.08/644.53/666.51/669.33				Multi-rate type[3]
	Frequency Tolerance	-20	—	-20	ppm		OC-192/STM-64
		-100	—	+100			10GbE
	Duty Cycle	40	—	60	%		
	Input Level	200	—	900	mV p-p		Single-ended voltage swing
Receiver Reference Clock							
RxREFCLKP/N	Frequency		155.52 or 622.08		MHz	AC Coupled	OC-192/STM-64
			161.13 or 644.53				10GbE
			166.63 or 666.51				FEC
			167.33 or 669.33				OTN
			155.52/161.13/166.63/167.33 or 622.08/644.53/666.51/669.33				Multi-rate type
	Frequency Tolerance	-20	—	+20			OC-192/STM-64
		-100	—	+100	ppm		10GbE
	Duty Cycle	40	—	60	%		
	Input Level	200	—	900	mV p-p		Single-ended voltage swing

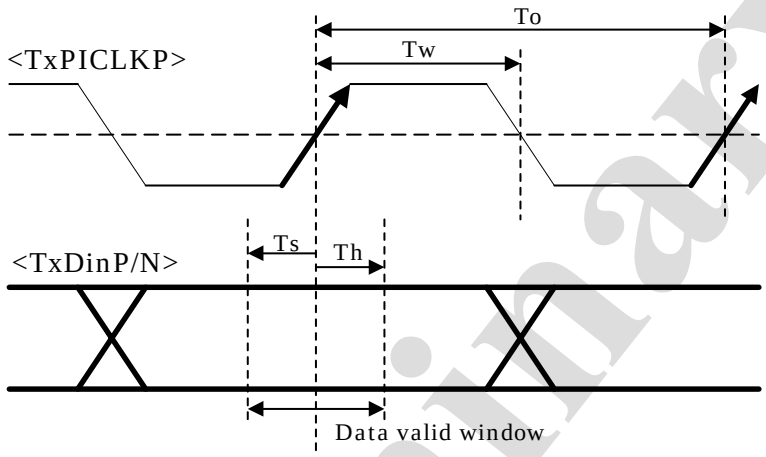
Note[2]: Though 622MHz operation of TxREFCLK is standard, 155MHz operation is also available.
Note[3]: Multi-rate type, OAT1049x-V5-C-yy can select 155MHz or 622MHz.

Table 4.2.2 Data/Clock Interfaces

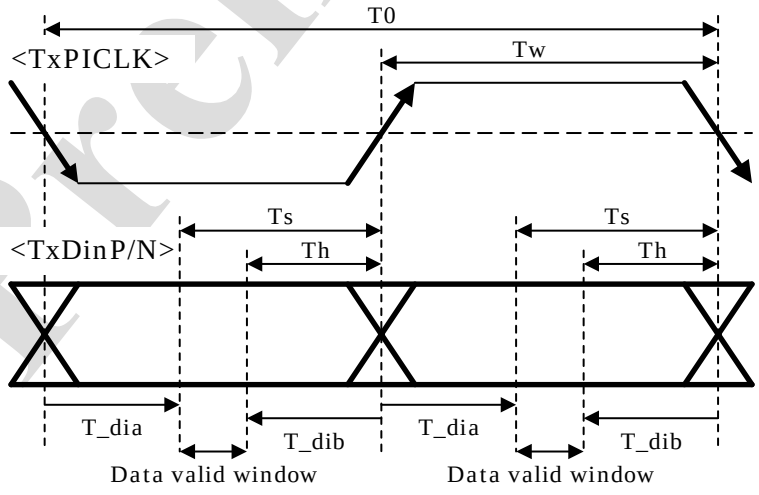
Name	Function	I/O	Logic	Note
Transmitter				
TxDin[0:15]P/N	Transmitter 16 bit parallel data input	I	LVDS	TxDin0: LSB TxDin15: MSB
TxPICLKP/N	Transmitter source synchronous parallel input clock	I	LVDS	
TxPCLKP/N	Transmitter parallel output clock	O	LVDS	
Receiver				
RxDout[0:15]P/N	Receiver 16 bit parallel data output	O	LVDS	RxDout0: LSB RxDout15: MSB
RxPOCLKP/N	Receiver source synchronous parallel output clock	O	LVDS	

Table 4.2.3 Data/Clock Timings

Name	Parameter	Symbol	Min.	Max.	Unit	Note
Transmitter Data/Clock Input Timing (622MHz Mode)						
TxPICLK	Duty Cycle	Tw/To	40	60	%	
	Rise Time	Tr	100	300	ps	20 – 80%
	Fall Time	Tf	100	300	ps	80 – 20%
TxDin [0:15]P/N	Setup Time	Ts	—	300	ps	
	Hold Time	Th	—	300	ps	



Transmitter Data/Clock Input Timing (311MHz Mode)						
TxPICLK	Duty Cycle	Tw/To	48	52	%	
	Rise Time	Tr	100	300	ps	20 – 80%
	Fall Time	Tf	100	300	ps	80 – 20%
TxDin [0:15]P/N	Setup Time	Ts	—	1100	ps	
	Hold Time	Th	—	500	ps	
	Define Data Invalid Window	T_dib	—	500	ps	
		T_dia	—	500	ps	



Receiver Data/Clock Output Timing						
RxPOCLK	Duty Cycle	Tw/To	45	55	%	
	Rise Time	Tr	—	300	ps	20 – 80%
	Fall Time	Tf	—	300	ps	80 – 20%
RxDout [0:15]P/N	Data/Clock Skew	Tcq_min,	—	250	ps	
		Tcq_max	—	250	ps	

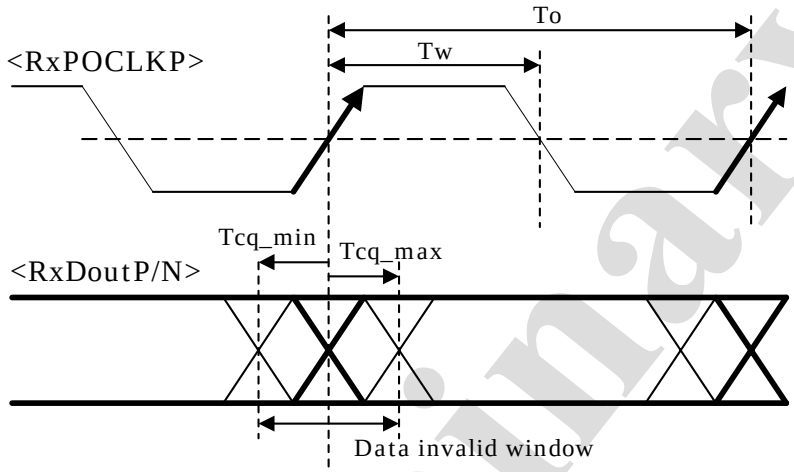


Table 4.2.4 Monitor Clocks

Name	**Function**	**I/O**	**Interface**	**Note**
Transmitter				
TxMCLKP/N	Transmitter monitor clock	O	LVDS	f=TxREFCLKP/N frequency
Receiver				
RxMCLKP/N	Receiver monitor clock	O	LVDS	f=RxREFCLKP/N frequency

Table 4.2.5 Transmitter Data Rate Select

TxRATESEL1[4]	**TxRATESEL0**[4]	**Function**		**Note**
		Serial Data Rate	**Parallel Data Rate**	
H	H	9.95328Gbit/s	622.08Mbit/s	LVTTL interface Internal pull up to Vcc (R>10kΩ)
L	L	10.3125Gbit/s	644.54Mbit/s	
L	H	10.664 to 10.709Gbit/s	666.51 to 669.33Mbit/s	
H	L			

Note[4]: TxRATESEL1/0 are available for multi-rate type, OAT1049x-V5-C-yy.

Table 4.2.6 Receiver Data Rate Select

RxRATESEL1	RxRATESEL0	Function		Note
		Serial Data Rate	Parallel Data Rate	
H	H	9.95328Gbit/s	622.08Mbit/s	LVTTL interface Internal pull up to Vcc (R>10kΩ)
L	L	10.3125Gbit/s	644.54Mbit/s	
L	H	10.664 to 10.709Gbit/s	666.51 to 669.33Mbit/s	
H	L			

Table 4.2.7 Digital Control Signals

Pin	Name	Function	Logic		Description	Note
Transmitter						
B21 B18	TxSKEWSEL 1/0	Adjust skew of TxPICLK (MSB, LSB)	LVTTL	LL	Delays the TxPICLK by 915ps	Internal pull up to Vcc (R>10kΩ) Applicable only when TxPICLKSEL is H
				LH	Delays the TxPICLK by 1015ps	
				HL	Delays the TxPICLK by 715ps	
				HH	Delays the TxPICLK by 815ps	
B27	TxPICLKSEL	Selects speed of input TxPICLK	LVTTL	L	Selects 622MHz	Internal pull down to GND (R>10kΩ)
				H	Selects 311MHz	
F21	LsENABLE	Enables/Disables laser	LVTTL	L	Normal operation	Internal pull down to GND (R>10kΩ)
				H	Laser disabled	
F30	TxREFSEL[5]	Selects TxREFCLK frequency	LVTTL	L	Selects 155MHz	Internal pull up to Vcc (R>10kΩ)
				H	Selects 622MHz	
K24	TxRESET[6]	Transmitter asynchronous system reset	LVTTL	L	MUX system reset	Internal pull up to Vcc (R>10kΩ)
				H	Normal operation	
K27	TxFIFO RES	MUX FIFO reset	LVTTL	L	MUX FIFO reset	Internal pull up to Vcc (R>10kΩ)
				H	Normal operation	
Receiver						
B6	RxMUTE Dout	Mutes the RxDout[0:15] to logical zero	LVTTL	L	Mutes the RxDout[0:15]	Internal pull up to Vcc (R>10kΩ)
				H	Normal operation	
B9	RxLCKREF	Locks RxPOCLK to RxREFCLK	LVTTL	L	Locks to RxREFCLK	Internal pull up to Vcc (R>10kΩ)
				H	Normal operation	
F15	RxREFSEL	Selects RxREFCLK frequency	LVTTL	L	Selects 155MHz	Internal pull down to GND (R>10kΩ)
				H	Selects 622MHz	
K9	RxMUTEPO CLK	Mutes the RxPOCLK to logical zero	LVTTL	L	Mutes the RxPOCLK	Internal pull up to Vcc (R>10kΩ)
				H	Normal operation	
K12	RxMUTEMC LK	Mutes the RxMCLK to logical zero	LVTTL	L	Mutes the RxMCLK	Internal pull up to Vcc (R>10kΩ)
				H	Normal operation	
Others						
D12	MOD_RESET	Module asynchronous system reset	LVTTL	L	Resets both Tx and Rx	Internal pull up to Vcc (R>10kΩ)
				H	Normal operation	

Note[5]: TxREFSEL is available for multi-rate type, OAT1049x-V5-C-yy.
Note[6]: TxRESET includes the function of resetting MZM modulator bias to quadrature point around 0V.

Table 4.2.8 Alarms

Pin	Name	Function	Logic		Description	Note
Transmitter						
B30	TxLOCKERR	Indicates loss of TxPLL lock	LVTTL	L	Indicates loss of PLL lock	
				H	Normal operation	
D30	LsPOWALM	Loss of laser average power alarm	LVTTL	L	Alarm active	Output degrades 3dB below the Po (BOL)
				H	Normal operation	
F24	LsBIASALM	Laser bias current alarm	LVTTL	L	Alarm active	Ib> 150mA (typ.)
				H	Normal operation	
F27	LsTEMPALM	Laser temperature alarm	LVTTL	L	Alarm active	Without +/-0.1K range
				H	Normal operation	
J16	TxALM INT	Electrical "OR" of all Tx alarms	Open collector	L	Alarm active	Excluding local functions
				H	Normal operation	
J20	ModBIASALM	Modulator bias alarm	LVTTL	L	Alarm active	
				H	Normal operation	
K30	TxFIFO ERR	Mux FIFO error indicator	LVTTL	L	Alarm active	
				H	Normal operation	
Receiver						
B15	RxLOCKERR	Loss of lock of RxPOCLK	LVTTL	L	Indicates loss of PLL lock	
				H	Normal operation	
F6	RxPOWALM	Loss of receiver average power alarm	LVTTL	L	Alarm active	Pin<-25dBm (typ.)
				H	Normal operation	
F12	RxSIGALM	Loss of receiver a.c. power alarm	LVTTL	L	Alarm active	Pin<-30dBm (typ.)
				H	Normal operation	
J14	RxALM INT	Electrical "OR" of all Rx alarms	Open collector	L	Alarm active	Excluding local functions
				H	Normal operation	
J24	APD_FAIL_ALM	High voltage DC/DC converter error	LVTTL	L	APD high voltage out of range	Local function
				H	Normal operation	
Others						
H15	ALM INT	Electrical "OR" of all Rx and Tx alarms	Open collector	L	Alarm active	Excluding local functions
				H	Normal operation	
J12	WDT_ALM	DSP watch dog timer error	LVTTL	L	DSP error	See Figure 4.2.1 Local function
				H	Normal operation	
J25	EEPROM_ALM	Program load error	LVTTL	L	Program load error	Local function
				H	Normal operation	

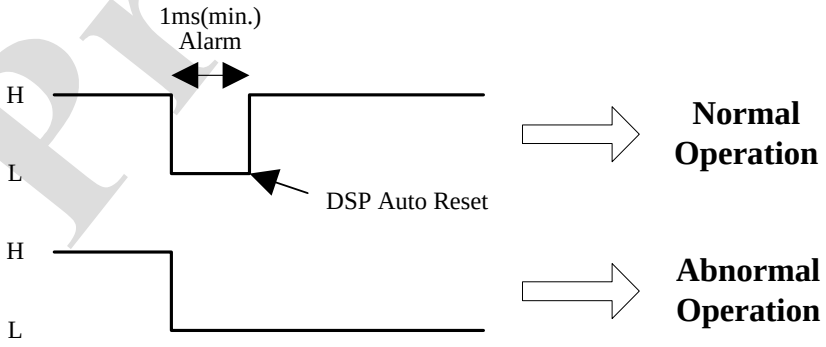


Figure 4.2.1 Operation of WDT_ALM

Table 4.2.9 Monitor Signals

Pin	Name	Function	Min.	Typ.	Max.	Unit
Transmitter						
D18	LsPOWMON	Laser output power monitor (BOL)	0.44	0.5	0.56	V
		50% variation of laser power		0.25		V
D21	LsTEMPMON	Laser temperature monitor	—	2.5	—	V
		Laser temperature monitor slope	20	25	30	mV/K
F18	LsBIASMON	Laser bias current monitor	17.8	20	22.5	mV/mA
Receiver						
F3	RxPOWMON[7]	Receiver power monitor	—	8	—	V/mW

Note[7]: RxPOWMON is incorrect in case of Pin > -5dBm.

Table 4.2.10 LVDS Interfaces

	Symbol	Min.	Typ.	Max.	Unit
Input					
LVDS Common Mode Input Voltage	$(V_A+V_B)/2$	850	—	2200	mV
LVDS Differential Input Swing	$\| V_A-V_B \|/2$	100	—	—	mVpp
LVDS Input High Voltage	V_{IH}	—	—	2400	mV
LVDS Input Low Voltage	V_{IL}	800	—	—	mV
LVDS Differential Input Impedance		80	100	120	Ω
LVDS Rise & Fall Times		—	—	300	ps
Output					
LVDS Common Mode Output Voltage	$(V_A+V_B)/2$	1100	1200	1300	mV
LVDS Differential Output Swing	$\| V_A-V_B \|/2$	250	—	400	mVpp
LVDS Output High Voltage	V_{OH}		TBD		mV
LVDS Output Low Voltage	V_{OL}		TBD		mV
LVDS Differential Output Impedance		80	100	120	Ω
LVDS Rise & Fall Times			TBD		ps

Table 4.2.11 LVTTL Interfaces

	Symbol	Min.	Typ.	Max.	Unit
Input					
Input High Voltage	V_{IH}	2000	—	5500	mV
Input Low Voltage	V_{IL}	-300	—	800	mV
Output					
Output High Voltage	V_{OH}	2400	—	Vcc	mV
Output Low Voltage	V_{OL}	GND	—	400	mV

5. Mechanical Information

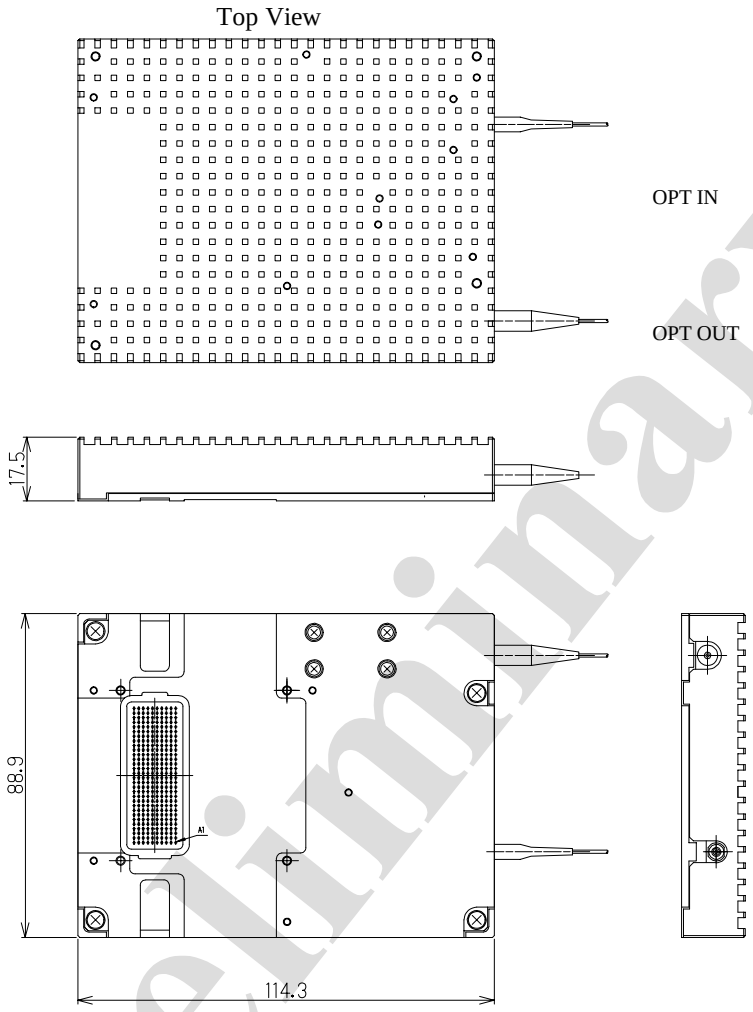


Figure 5-1 Package Outline (Unit:mm)

Table 5.1.1 Dimensions (with Heat Sink)

	Dimensions	Unit
Width	88.9	mm
Length	114.3	
Height	17.5	

Table 5.1.2 Connectors

Optical	SC/PC type standard Other connectors is available @FC, LC, MU
Electrical	300pin BERG MegArray @84501-10X

6.Connector Pinout

	K	J	H	G	F	E	D	C	B	A
1	NUC	NUC	GND	RxDout12P	(+)1.8V	RxDout8P	GND	RxDout4P	GND	RxDout0P
2	NUC	NUC	GND	RxDout12N	(+)1.8V	RxDout8N	GND	RxDout4N	GND	RxDout0N
3	RxRATESEL0	RxRATESEL1	NUC	GND	RxPOWMON	GND	NUC	GND	NUC	GND
4	(+)3.3V	NUC	GND	RxDout13P	(+)3.3V	RxDout9P	GND	RxDout5P	GND	RxDout1P
5	(+)3.3V	NUC	GND	RxDout13N	(+)3.3V	RxDout9N	GND	RxDout5N	GND	RxDout1N
6	NUC	NUC	NUC	GND	RxPOWALM	GND	NUC	GND	RxMUTE Dout	GND
7	(+)3.3V	NUC	GND	RxDout14P	(+)3.3V	RxDout10P	GND	RxDout6P	GND	RxDout2P
8	(+)3.3V	NUC	GND	RxDout14N	(+)3.3V	RxDout10N	GND	RxDout6N	GND	RxDout2N
9	RxMUTEPOCLK	NUC	NUC	GND	NUC	GND	NUC	GND	RxLCKREF	GND
10	(-)5.2V	NUC	GND	RxDout15P	(-)5.2V	RxDout11P	GND	RxDout7P	GND	RxDout3P
11	(-)5.2V	NUC	GND	RxDout15N	(-)5.2V	RxDout11N	GND	RxDout7N	GND	RxDout3N
12	RxMUTEMCLK	WDT_ALM	NUC	GND	RxSIGALM	GND	MOD_RESET	GND	NUC	GND
13	(-)5.2V	NUC	GND	NUC	(-)5.2V	RxPOCLKP	GND	RxMCLKP	GND	RxREFCLKP
14	(-)5.2V	RxALM INT	GND	NUC	(-)5.2V	RxPOCLKN	GND	RxMCLKN	GND	RxREFCLKN
15	NUC	NUC	ALM INT	GND	RxREFSEL	GND	NUC	GND	RxLOCKERR	GND
16	NUC	TxALM INT	GND	TxDin12P	(+)1.8V	TxDin8P	GND	TxDin4P	GND	TxDin0P
17	NUC	NUC	GND	TxDin12N	(+)1.8V	TxDin8N	GND	TxDin4N	GND	TxDin0N
18	NUC	NUC	NUC	GND	LsBIASMON	GND	LsPOWMON	GND	TxSKEWSEL0	GND
19	(+)3.3V	NUC	GND	TxDin13P	(+)3.3V	TxDin9P	GND	TxDin5P	GND	TxDin1P
20	(+)3.3V	ModBIASALM	GND	TxDin13N	(+)3.3V	TxDin9N	GND	TxDin5N	GND	TxDin1N
21	TxRATESEL0	TxRATESEL1	NUC	GND	LsENABLE	GND	LsTEMPMON	GND	TxSKEWSEL1	GND
22	(+)3.3V	NUC	GND	TxDin14P	(+)3.3V	TxDin10P	GND	TxDin6P	GND	TxDin2P
23	(+)3.3V	NUC	GND	TxDin14N	(+)3.3V	TxDin10N	GND	TxDin6N	GND	TxDin2N
24	TxRESET	APD_FAIL_ALM	NUC	GND	LsBIASALM	GND	NUC	GND	NUC	GND
25	(-)5.2V	EEPROM_ALM	GND	TxDin15P	(-)5.2V	TxDin11P	GND	TxDin7P	GND	TxDin3P
26	(-)5.2V	NUC	GND	TxDin15N	(-)5.2V	TxDin11N	GND	TxDin7N	GND	TxDin3N
27	TxFIFO RES	NUC	NUC	GND	LsTEMPALM	GND	NUC	GND	TxPICLKSEL	GND
28	(-)5.2V	NUC	GND	TxPICLKP	(-)5.2V	TxPCLKP	GND	TxMCLKP	GND	TxREFCLKP
29	(-)5.2V	NUC	GND	TxPICLKN	(-)5.2V	TxPCLKN	GND	TxMCLKN	GND	TxREFCLKN
30	TxFIFO ERR	NUC	NUC	GND	TxREFSEL	GND	LsPOWALM	GND	TxLOCKERR	GND

NUC: No User Connection

7. Precautions for Handling

The circuits of these modules operate at very small signal. In order to avoid the degradation of the optical sensitivity due to external noise, the bottom pattern of these modules on the PCB should be ground pattern with low impedance.

Do not mount/pattern device/circuits which generate high frequency noise close to the module.

In order to operate the module stable against the power noise, install the power supply noise reduction circuits.

The impedance between the power and ground pattern of the power circuit should be as low as possible. The elements around the module should be mounted close to the pins of the module.

If an optical power exceeding the absolute maximum ratings is fed to the module, the optical receiver may be damaged. Set the optical input power appropriately when in use of these modules.

8. Qualifications and Reliability

To help ensure high product reliability and customer satisfaction, OKI is committed to an intensive quality program that starts in the design phase and proceeds through the manufacturing process.

Optical transceiver modules are qualified to OKI internal standards using MIL-STD-883 test methods and procedures and using sample techniques consistent with Telcordia requirements.

This qualification program fully meets the intent of Telcordia reliability practices GR-468-CORE.

9. Laser Safety

All version of transceiver are Class 1 Laser products FDA complies with 21 CFR 1040.10 and 1040.11 requirements.

Also, all versions are Class 1 Laser products pre IEC 825-1**.**

10. Ordering Information

OAT1049x-V5-z-yy -[ ]

Table 10.1 Ordering Information

x		**z**		**yy**		**-[ ]** [8]	
Optical connector		Bit rate(Gbit/s)		Fiber length(m)		TxREFCLK frequency	
S	SC	A	9.95	10	1	(blank)	622MHz
F	FC	B	10.3	05	0.5	-L	155MHz
L	LC	C	9.95/10.3/10.6/10.7				
M	MU	D	10.7				
		E	10.6				

Note[8]: In case of z=A, B, D, E, "-[ ]" is added when 155MHz is specified to be TxREFCLK frequency.