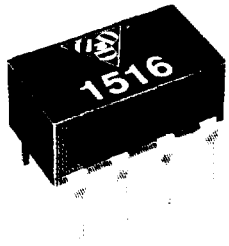
5 Taps — Delay Lines

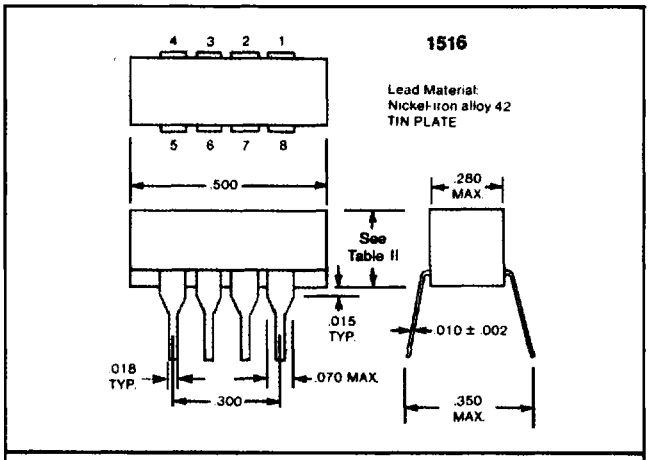
SERIES: 1516 (DIP)
1516S (SMD)

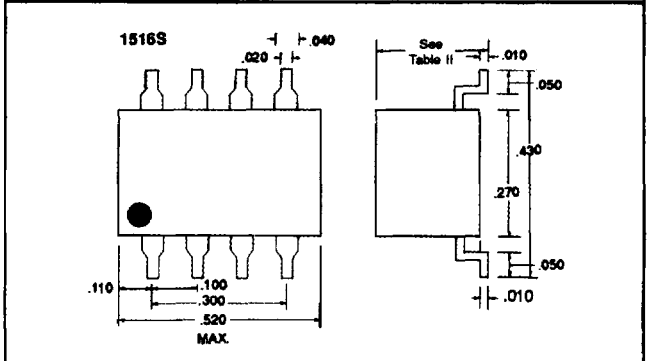
$T_D/T_R = 3/1$

FEATURES:



- 200 ns delay.
- 5 taps.
- Standard 8 pins DIP & SMD cases.
- Low D.C. resistance.
- Fast delivery.





PART NUMBER MAKE-UP

1516S A 101 151 A

- SERIES
- MOUNTING HEIGHT CODE (see Table II)
- DELAY TIME: Expressed in nanoseconds (ns). First two digits are significant figures. Last digit specifies number of zeros to follow.
- IMPEDANCE: Expressed in ohms. First two digits are significant. Last digit specifies number of zeros to follow.
- PIN SEQUENCE CODE: (SEE Table III). "STANDARD" Pin sequence if omitted.

SPECIFICATIONS:

- **Delay accuracy:** ± 5% (others on request)
- **No. taps:** 5 equally spaced taps
- **Taps accuracy:** ± 5% of tap delay
- **Impedance tolerance:** ± 10% (others on request)
- **Rise-time:** 30% of time delay
- **Withstanding voltage:** 50 Vdc min.
- **Temperature coefficient:** 100 PPM/°C.
- **Environment:** Meets or exceeds MIL-D-23859C.

TABLE I

Td (ns)[1]	Td/tap (ns)[2] (±5%)	Tr (ns) Max.	ATTENUATION (%) TYPICAL PER IMPEDANCE 50	100	200	300	500
5	1	3		5			
10	2	4	3	5	5		
15	3	5	3	5	5		
20	4	6	3	5	5	5	
25	**5**	**7**	**3**	**5**	**5**	**5**	**7**
30	**6**	**10**	**3**	**5**	**5**	**5**	**7**
40	**8**	**13**	**3**	**5**	**5**	**5**	**7**
50	**10**	**15**	**3**	**5**	**5**	**7**	**7**
60	**12**	**20**	**3**	**5**	**6**	**7**	**8**
75	15	25	3	5	6	7	8
80	16	26	4	5	6	7	8
100	20	30	4	5	6	7	8
110	22	32	4	5	6	7	8
125	25	40	4	5	6	7	8
150	**30**	**50**		**5**	**8**	**10**	**10**
180	**36**	**60**		**7**	**8**	**10**	**10**
200	**40**	**70**		**8**	**10**	**12**	**12**

[1] Or ± 2 ns, whichever is greater.
[2] Or ± 1 ns, whichever is greater, referenced from input.

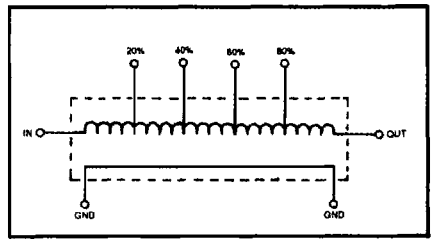


TABLE II

MOUNTING HEIGHT CODE	DIMENSIONS (MAX)
A	.187
B	.240
C	.290

TABLE III

CODE	IN	20%	40	60%	80%	OUT	GROUND
STANDARD	2	3	4	5	6	7	1, 8
A	1	2	3	4	6	7	5, 8
B	1	7	3	6	4	5	8
C	7	2	6	3	5	4	1, 8
D	1	2	7	3	6	4	5, 8

Other pin sequences available

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