

Z86E33/733/E34 Z86E43/743/E44 CMOS Z8 OTP MICROCONTROLLERS

FEATURES

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Speed (MHz)
Z86E33	4	237	24	12
Z86733	8	237	24	12
Z86E34	16	237	24	12
Z86E43	4	236	32	12
Z86743	8	236	32	12
Z86E44	16	236	32	12

Note: *General-Purpose

- Standard Temperature ($V_{CC} = 3.5V$ to $5.5V$)
- Extended Temperature ($V_{CC} = 4.5V$ to $5.5V$)
- Available Packages:
28-Pin DIP/SOIC/PLCC OTP (E33/733/E34)
40-Pin DIP OTP (E43/743/E44)
44-Pin PLCC/QFP OTP (E43/743/E44)
- Software Enabled Watch-Dog Timer (WDT)
- Push-Pull/Open-Drain Programmable on Port 0, Port 1, and Port 2
- 24/32 Input/Output Lines
- Clock-Free WDT Reset

- Auto Power-On Reset (POR)
- Programmable OTP Options:
RC Oscillator
EPROM Protect
Auto Latch Disable
Permanently Enabled WDT
Crystal Oscillator Feedback Resistor Disable
RAM Protect
- Low-Power Consumption: 60 mW
- Fast Instruction Pointer: $0.75 \mu s$
- Two Standby Modes: STOP and HALT
- Digital Inputs CMOS Levels, Schmitt-Triggered
- Software Programmable Low EMI Mode
- Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Two Comparators
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive

GENERAL DESCRIPTION

The Z86E33/733/E34/E43/743/E44 8-Bit One-Time Programmable (OTP) Microcontrollers are members of Zilog's single-chip Z8[®] MCU family featuring enhanced wake-up circuitry, programmable Watch-Dog Timers, Low Noise EMI options, and easy hardware/software system expansion capability.

Four basic address spaces support a wide range of memory configurations. The designer has access to three addi-

tional control registers that allow easy access to register mapped peripheral and I/O circuits.

For applications demanding powerful I/O capabilities, the Z86E33/733/E34 have 24 pins, and the Z86E43/743/E44 have 32 pins of dedicated input and output. These lines are grouped into four ports, eight lines per port, and are configurable under software control to provide timing, status sig-

*Z86E33/733/E34

GENERAL DESCRIPTION (Continued)

nals, and parallel I/O with or without handshake, and address/data bus for interfacing external memory.

Power connections follow conventional descriptions below:

Notes: All signals with a preceding front slash, "/", are active Low. For example, B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}

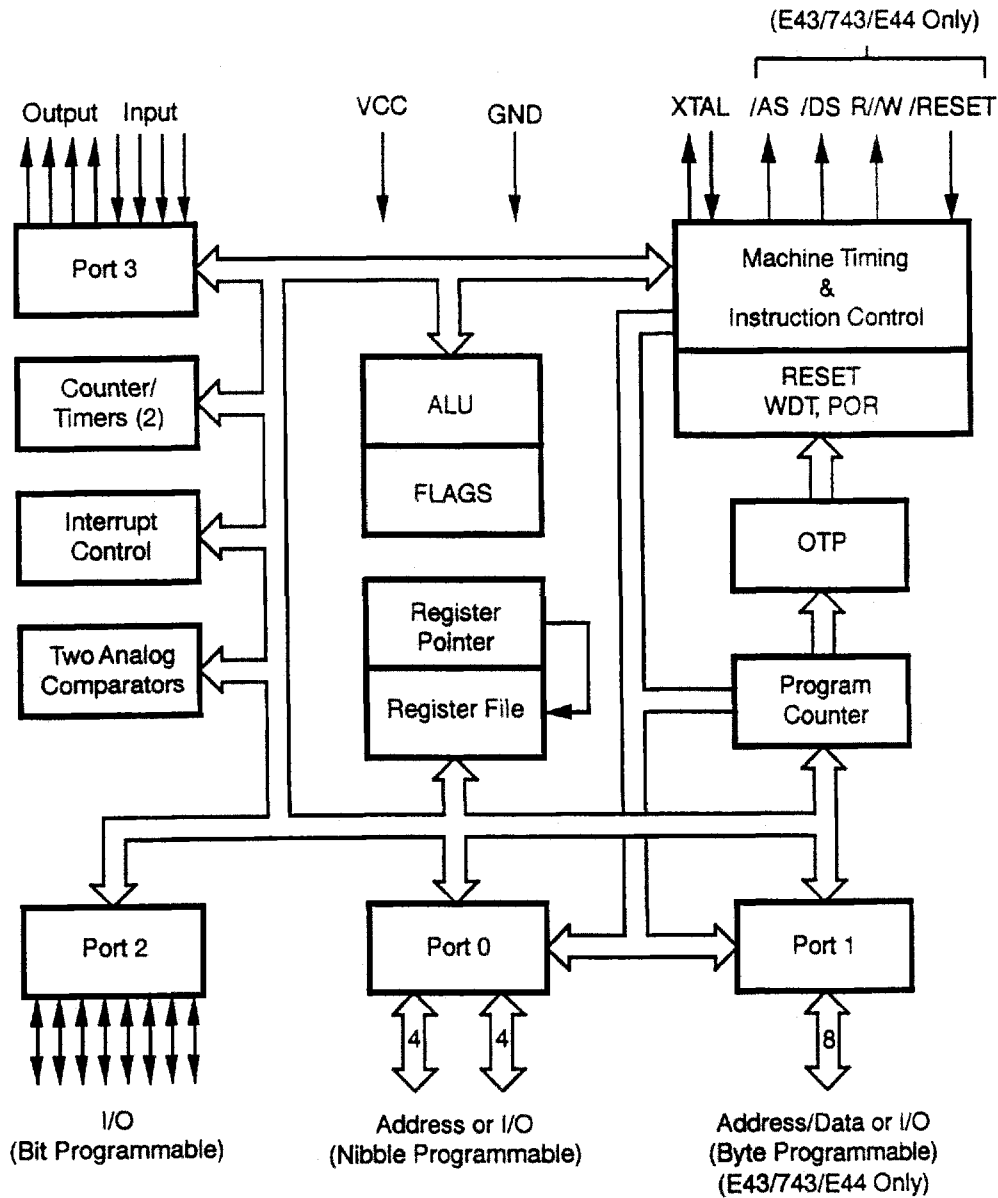


Figure 1. Functional Block Diagram

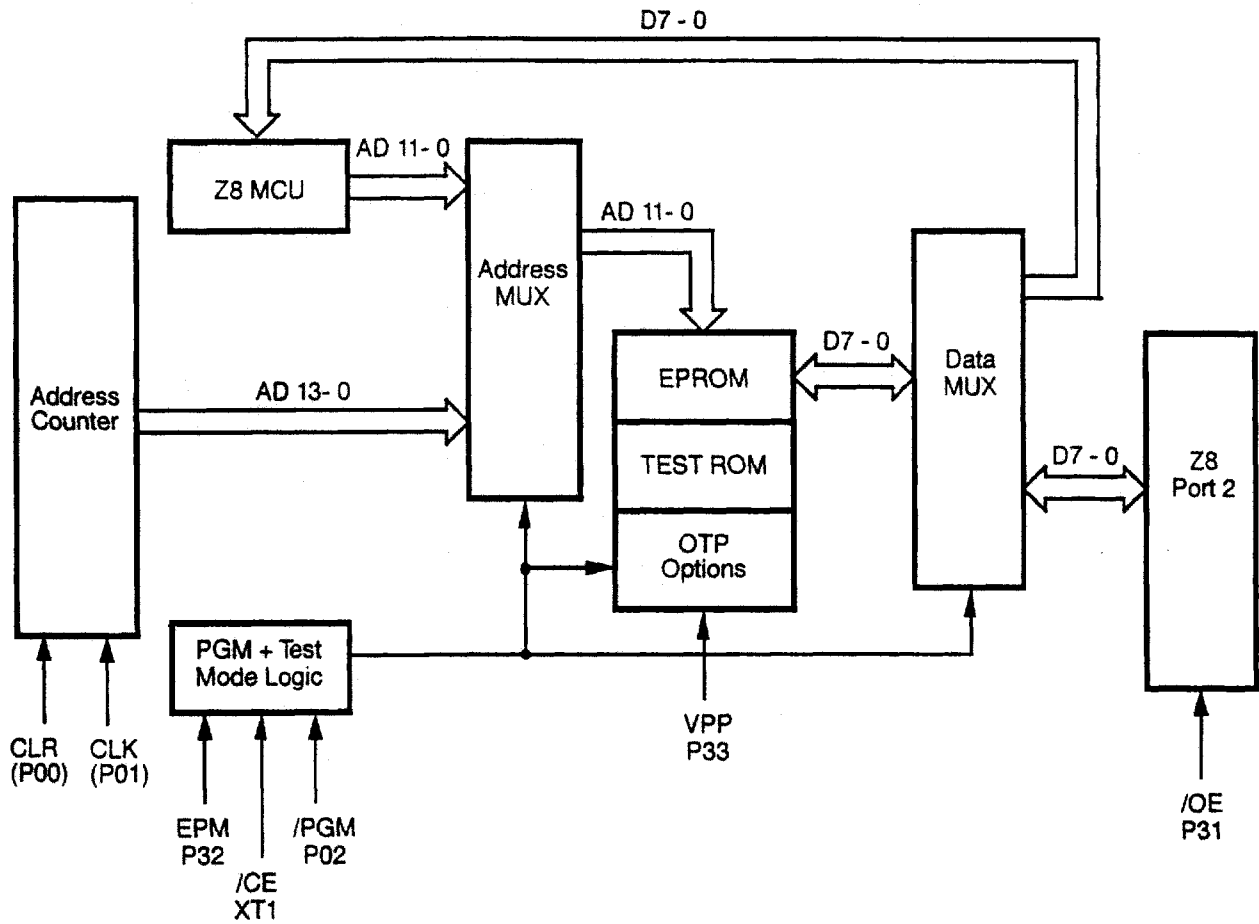


Figure 2. EPROM Programming Block Diagram

PIN IDENTIFICATION

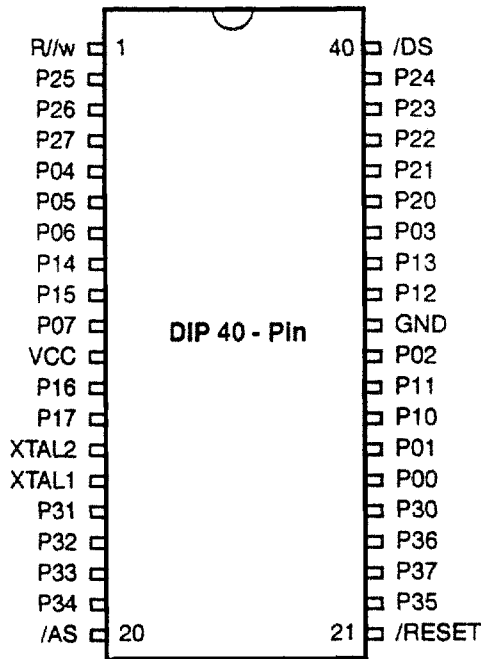


Figure 3. 40-Pin DIP Pin Configuration Standard Mode

Table 1. 40-Pin DIP Pin Identification Standard Mode

Pin #	Symbol	Function	Direction
1	R/W	Read/Write	Output
2-4	P25-P27	Port 2, Pins 5,6,7	In/Output
5-7	P04-P06	Port 0, Pins 4,5,6	In/Output
8-9	P14-P15	Port 1, Pins 4,5	In/Output
10	P07	Port 0, Pin 7	In/Output
11	V _{CC}	Power Supply	
12-13	P16-P17	Port 1, Pins 6,7	In/Output
14	XTAL2	Crystal Oscillator	Output
15	XTAL1	Crystal Oscillator	Input
16-18	P31-P33	Port 3, Pins 1,2,3	Input
19	P34	Port 3, Pin 4	Output
20	/AS	Address Strobe	Output
21	/RESET	Reset	Input
22	P35	Port 3, Pin 5	Output
23	P37	Port 3, Pin 7	Output
24	P36	Port 3, Pin 6	Output
25	P30	Port 3, Pin 0	Input
26-27	P00-P01	Port 0, Pins 0,1	In/Output
28-29	P10-P11	Port 1, Pins 0,1	In/Output
30	P02	Port 0, Pin 2	In/Output
31	GND	Ground	
32-33	P12-P13	Port 1, Pins 2,3	In/Output
34	P03	Port 0, Pin 3	In/Output
35-39	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output
40	/DS	Data Strobe	Output

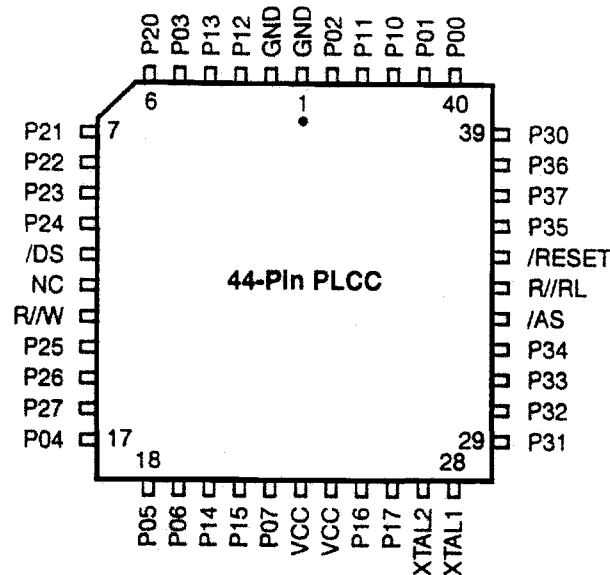


Figure 4. 44-Pin PLCC Pin Configuration
Standard Mode

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1-2	GND	Ground	
3-4	P12-P13	Port 1, Pins 2,3	In/Output
5	P03	Port 0, Pin 3	In/Output
6-10	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output
11	/DS	Data Strobe	Output
12	NC	No Connection	
13	R//W	Read/Write	Output
14-16	P25-P27	Port 2, Pins 5,6,7	In/Output
17-19	P04-P06	Port 0, Pins 4,5,6	In/Output
20-21	P14-P15	Port 1, Pins 4,5	In/Output
22	P07	Port 0, Pin 7	In/Output
23-24	VCC	Power Supply	
25-26	P16-P17	Port 1, Pins 6,7	In/Output
27	XTAL2	Crystal Oscillator	Output

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
28	XTAL1	Crystal Oscillator	Input
29-31	P31-P33	Port 3, Pins 1,2,3	Input
32	P34	Port 3, Pin 4	Output
33	/AS	Address Strobe	Output
34	R//RL	ROM/ROMless select	Input
35	/RESET	Reset	Input
36	P35	Port 3, Pin 5	Output
37	P37	Port 3, Pin 7	Output
38	P36	Port 3, Pin 6	Output
39	P30	Port 3, Pin 0	Input
40-41	P00-P01	Port 0, Pins 0,1	In/Output
42-43	P10-P11	Port 1, Pins 0,1	In/Output
44	P02	Port 0, Pin 2	In/Output

PIN IDENTIFICATION (Continued)

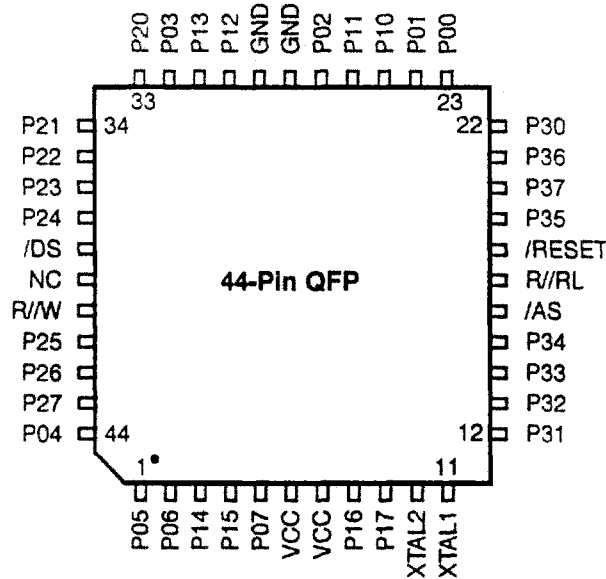


Figure 5. 44-Pin QFP Pin Configuration
Standard Mode

Table 3. 44-Pin QFP Pin Identification

Pin #	Symbol	Function	Direction
1-2	P05-P06	Port 0, Pins 5,6	In/Output
3-4	P14-P15	Port 1, Pins 4,5	In/Output
5	P07	Port 0, Pin 7	In/Output
6-7	VCC	Power Supply	
8-9	P16-P17	Port 1, Pins 6,7	In/Output
10	XTAL2	Crystal Oscillator	Output
11	XTAL1	Crystal Oscillator	Input
12-14	P31-P33	Port 3, Pins 1,2,3	Input
15	P34	Port 3, Pin 4	Output
16	/AS	Address Strobe	Output
17	R//RL	ROM/ROMless select	Input
18	/RESET	Reset	Input
19	P35	Port 3, Pin 5	Output
20	P37	Port 3, Pin 7	Output
21	P36	Port 3, Pin 6	Output

Table 3. 44-Pin QFP Pin Identification

Pin #	Symbol	Function	Direction
22	P30	Port 3, Pin 0	Input
23-24	P00-P01	Port 0, Pin 0,1	In/Output
25-26	P10-P11	Port 1, Pins 0,1	In/Output
27	P02	Port 0, Pin 2	In/Output
28-29	GND	Ground	
30-31	P12-P13	Port 1, Pins 2,3	In/Output
32	P03	Port 0, Pin 3	In/Output
33-37	P20-24	Port 2, Pins 0,1,2,3,4	In/Output
38	/DS	Data Strobe	Output
39	NC	No Connection	
40	R//W	Read/Write	Output
41-43	P25-P27	Port 2, Pins 5,6,7	In/Output
44	P04	Port 0, Pin 4	In/Output

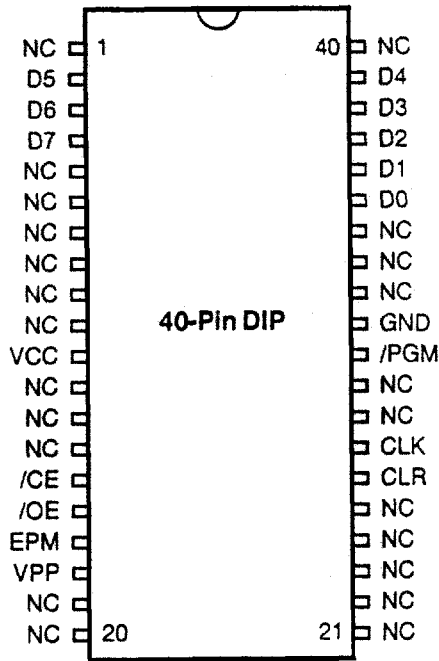


Figure 6. 40-Pin DIP Pin Configuration
EPROM Mode

Table 4. 40-Pin DIP Package Pin Identification
EPROM Mode

Pin #	Symbol	Function	Direction
1	NC	No Connection	
2-4	D5-D7	Data 5,6,7	In/Output
5-10	NC	No Connection	
11	V _{CC}	Power Supply	
12-14	NC	No Connection	
15	/CE	Chip Select	Input
16	/OE	Output Enable	Input
17	EPM	EPROM Prog. Mode	Input
18	VPP	Prog. Voltage	Input
19-25	NC	No Connection	
26	CLR	Clear	Input
27	CLK	Clock	Input
28-29	NC	No Connection	
30	/PGM	Prog. Mode	Input
31	GND	Ground	
32-34	NC	No Connection	
35-39	D0-D4	Data 0,1,2,3,4	In/Output
40	NC	No Connection	

PIN IDENTIFICATION (Continued)

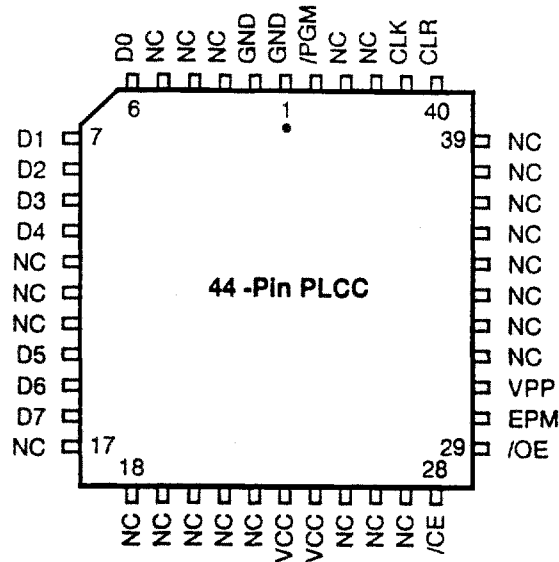


Figure 7. 44-Pin PLCC Pin Configuration
 EPROM Programming Mode

Table 5. 44-Pin PLCC Pin Configuration
 EPROM Programming Mode

Pin #	Symbol	Function	Direction
1-2	GND	Ground	
3-5	NC	No Connection	
6-10	D0-D4	Data 0,1,2,3,4	In/Output
11-13	NC	No Connection	
14-16	D5-D7	Data 5,6,7	In/Output
17-22	NC	No Connection	
23-24	VCC	Power Supply	
25-27	NC	No Connection	
28	/CE	Chip Select	Input

Table 5. 44-Pin PLCC Pin Configuration
 EPROM Programming Mode

Pin #	Symbol	Function	Direction
29	/OE	Output Enable	Input
30	EPM	EPROM Prog. Mode	Input
31	V _{pp}	Prog. Voltage	Input
32-39	NC	No Connection	
40	CLR	Clear	Input
41	CLK	Clock	Input
42-43	NC	No Connection	
44	/PGM	Prog. Mode	Input

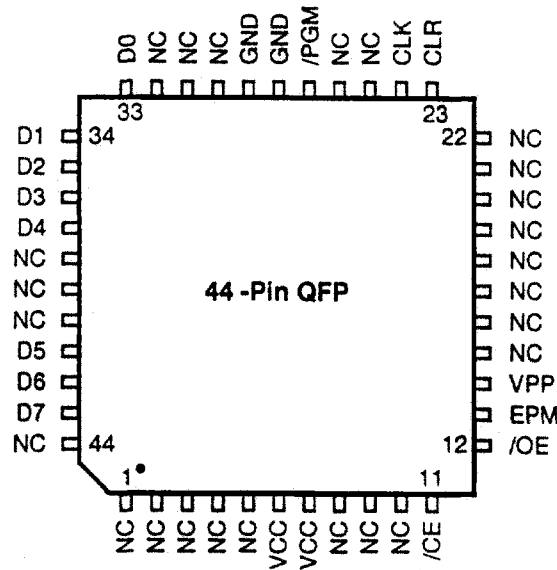


Figure 8. 44-Pin QFP Pin Configuration
EPROM Programming Mode

Table 6. 44-Pin QFP Pin Identification
EPROM Programming Mode

Pin #	Symbol	Function	Direction
1-5	NC	No Connection	
6-7	V _{CC}	Power Supply	
8-10	NC	No Connection	
11	/CE	Chip Select	Input
12	/OE	Output Enable	Input
13	EPM	EPROM Prog. Mode	Input
14	V _{PP}	Prog. Voltage	Input
15-22	NC	No Connection	
23	CLR	Clear	Input

Table 6. 44-Pin QFP Pin Identification
EPROM Programming Mode

Pin #	Symbol	Function	Direction
24	CLK	Clock	Input
25-26	NC	No Connection	
27	/PGM	Prog. Mode	Input
28-29	GND	Ground	
30-32	NC	No Connection	
33-37	D0-D4	Data 0,1,2,3,4	In/Output
38-40	NC	No Connection	
41-43	D5-D7	Data 5,6,7	In/Output
44	NC	No Connection	

PIN IDENTIFICATION (Continued)

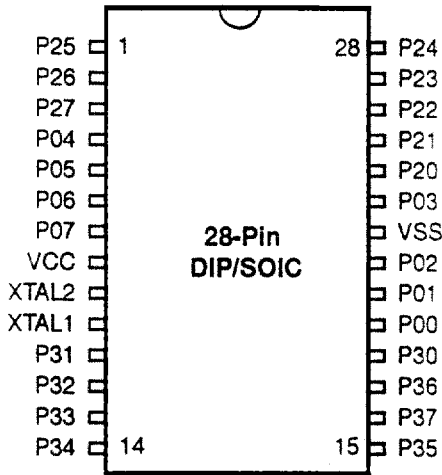


Figure 9. Standard Mode
 28-Pin DIP/SOIC Pin Configuration

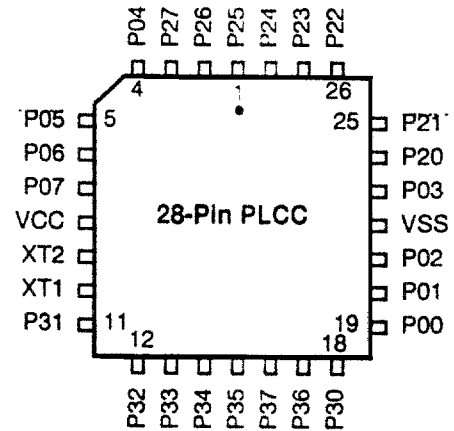


Figure 10. Standard Mode
 28-Pin PLCC Pin Configuration

Table 7. 28-Pin DIP/SOIC/PLCC
 Pin Identification
 Standard Mode

Pin #	Symbol	Function	Direction
1-3	P25-P27	Port 2, Pins 5,6,	In/Output
4-7	P04-P07	Port 0, Pins 4,5,6,7	In/Output
8	V _{CC}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P31-P33	Port 3, Pins 1,2,3	Input
14-15	P34-P35	Port 3, Pins 4,5	Output
16	P37	Port 3, Pin 7	Output
17	P36	Port 3, Pin 6	Output
18	P30	Port 3, Pin 0	Input
19-21	P00-P02	Port 0, Pins 0,1,2	In/Output
22	V _{SS}	Ground	
23	P03	Port 0, Pin 3	In/Output
24-28	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output

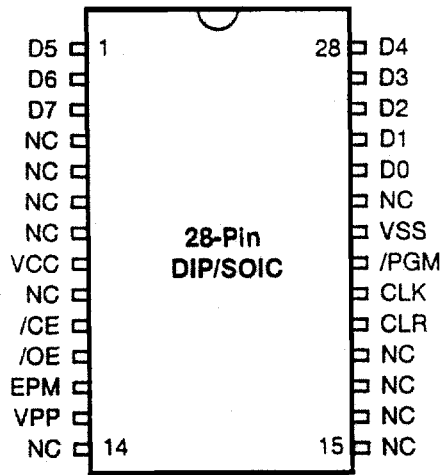


Figure 11. EPROM Programming Mode
28-Pin DIP/SOIC Pin Configuration

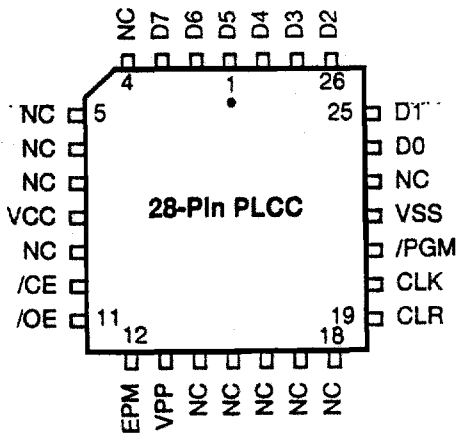


Figure 12. EPROM Programming Mode
28-Pin PLCC Pin Configuration

Table 8. 28-Pin EPROM
Pin Identification
EPROM Mode

Pin #	Symbol	Function	Direction
1-3	D5-D7	Data 5,6,7	In/Output
4-7	NC	No Connection	
8	V _{CC}	Power Supply	
9	NC	No connection	
10	/CE	Chip Select	Input
11	/OE	Output Enable	Input
12	EPM	EPROM Prog. Mode	Input
13	V _{PP}	Prog. Voltage	Input
14-18	NC	No Connection	
19	CLR	Clear	
20	CLK	Clock	
21	/PGM	Prog. Mode	Input
22	V _{SS}	Ground	
23	NC	No Connection	
24-28	D0-D4	Data 0,1,2,3,4	In/Output

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Ambient Temperature under Bias	-40	+105	C
Storage Temperature	-65	+150	C
Voltage on any Pin with Respect to V _{SS} [Note 1]	-0.6	+7	V
Voltage on V _{DD} Pin with Respect to V _{SS}	-0.3	+7	V
Voltage on XTAL1, P32, P33 and /RESET Pins with Respect to V _{SS} [Note 2]	-0.6	V _{DD} +1	V
Total Power Dissipation		1.21	W
Maximum Allowable Current out of V _{SS}		220	mA
Maximum Allowable Current into V _{DD}		180	mA
Maximum Allowable Current into an Input Pin [Note 3]	-600	+600	μA
Maximum Allowable Current into an Open-Drain Pin [Note 4]	-600	+600	μA
Maximum Allowable Output Current Sunk by Any I/O Pin		25	mA
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA
Maximum Allowable Output Current Sunk by /RESET Pin		3	mA

Notes:

1. This applies to all pins except XTAL pins and where otherwise noted.
2. There is no input protection diode from pin to V_{DD}.
3. This excludes XTAL pins.
4. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Total power dissipation should not exceed 1.2 W for the package. Power dissipation is calculated as follows:

$$\begin{aligned} \text{Total Power Dissipation} &= V_{DD} \times [I_{DD} - (\text{sum of } I_{OH})] \\ &+ \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] \\ &+ \text{sum of } (V_{OL} \times I_{OL}) \end{aligned}$$

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Test Load).

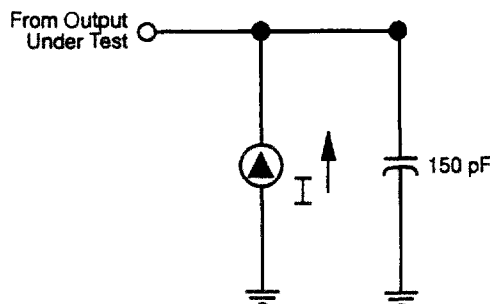


Figure 13. Test Load Diagram

CAPACITANCE

$T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$, $f = 1.0\text{ MHz}$; unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC} Note [3]	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$		Typical @ 25°C	Units	Conditions	Notes
			Min	Max				
V_{CH}	Clock Input High Voltage	3.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	1.8	V	Driven by External Clock Generator	
		5.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.5	V		
V_{CL}	Clock Input Low Voltage	3.5V	$\text{GND}-0.3$	$0.2 V_{CC}$	0.9	V	Driven by External Clock Generator	
		5.5V	$\text{GND}-0.3$	$0.2 V_{CC}$	1.5	V		
V_{IH}	Input High Voltage	3.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.5	V		
		5.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.5	V		
V_{IL}	Input Low Voltage	3.5V	$\text{GND}-0.3$	$0.2 V_{CC}$	1.5	V		
		5.5V	$\text{GND}-0.3$	$0.2 V_{CC}$	1.5	V		
V_{OH}	Output High Voltage Low EMI Mode	3.5V	$V_{CC}-0.4$		3.3	V	$I_{OH} = -0.5\text{ mA}$	
		5.5V	$V_{CC}-0.4$		4.8	V		
V_{OH1}	Output High Voltage	3.5V	$V_{CC}-0.4$		3.3	V	$I_{OH} = -2.0\text{ mA}$ $I_{OH} = -2.0\text{ mA}$	
		5.5V	$V_{CC}-0.4$		4.8	V		
V_{OL}	Output Low Voltage Low EMI Mode	3.5V		0.4	0.2	V	$I_{OL} = +1.0\text{ mA}$ $I_{OL} = +1.0\text{ mA}$	
		5.5V		0.4	0.2	V		
V_{OL1}	Output Low Voltage	3.5V		0.4	0.1	V	$I_{OL} = +4.0\text{ mA}$ $I_{OL} = +4.0\text{ mA}$	8
		5.5V		0.4	0.1	V		
V_{OL2}	Output Low Voltage	3.5V		1.2	0.5	V	$I_{OL} = +10\text{ mA}$ $I_{OL} = +10\text{ mA}$	8
		5.5V		1.2	0.5	V		
V_{RH}	Reset Input High Voltage	3.5V	$.8 V_{CC}$	V_{CC}	1.7	V		13
		5.5V	$.8 V_{CC}$	V_{CC}	2.1	V		
V_{RL}	Reset Input Low Voltage	3.5V	$\text{GND}-0.3$	$0.2 V_{CC}$	1.3	V		13
		5.5V	$\text{GND}-0.3$	$0.2 V_{CC}$	1.7	V		
V_{OLR}	Reset Output Low Voltage	3.5V		0.6	0.3	V	$I_{OL} = +1.0\text{ mA}$ $I_{OL} = +1.0\text{ mA}$	13
		5.5V		0.6	0.2	V		
V_{OFFSET}	Comparator Input Offset Voltage	3.5V		25	10	mV		
		5.5V		25	10	mV		
V_{ICR}	Input Common Mode Voltage Range	3.5V	0	$V_{CC}-1.0\text{V}$		V		10
		5.5V	0	$V_{CC}-1.0\text{V}$		V		
I_{IL}	Input Leakage	3.5V	-1	2	0.032	μA	$V_{IN} = 0\text{V}, V_{CC}$ $V_{IN} = 0\text{V}, V_{CC}$	
		5.5V	-1	2	0.032	μA		
I_{OL}	Output Leakage	3.5V	-1	2	0.032	μA	$V_{IN} = 0\text{V}, V_{CC}$ $V_{IN} = 0\text{V}, V_{CC}$	
		5.5V	-1	2	0.032	μA		

DC ELECTRICAL CHARACTERISTICS (Continued)

T _A = 0 °C to +70 °C								
Sym	Parameter	V _{CC} Note [3]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
I _{IR}	Reset Input Current	3.5V	-20	-130	-65	μA		
		5.5V	-20	-180	-112	μA		
I _{CC}	Supply Current	3.5V		15	5	mA	@ 12 MHz	4,5
		5.5V		20	15	mA	@ 12 MHz	4,5
I _{CC1}	Standby Current	3.5V		4	2	mA	V _{IN} = 0V, V _{CC}	4,5
		5.5V		6	4	mA	@ 12 MHz	4,5
	Halt Mode	3.5V		3	1.5	mA	Clock Divide by	4,5
		5.5V		5	3	mA	16 @ 12 MHz	4,5
I _{CC2}	Standby Current	3.5V		10	2	μA	V _{IN} = 0V, V _{CC}	6,11
		5.5V		10	3	μA	V _{IN} = 0V, V _{CC}	6,11
	Stop Mode	3.5V		15	7	μA	V _{IN} = 0V, V _{CC}	6,11,14
		5.5V		30	10	μA	V _{IN} = 0V, V _{CC}	6,11,14
I _{ALL}	Auto Latch Low Current	3.5V	0.7	8	2.4	μA	0V < V _{IN} < V _{CC}	9
		5.5V	1.4	15	4.7	μA	0V < V _{IN} < V _{CC}	9
I _{ALH}	Auto Latch High Current	3.5V	-0.6	-5	-1.8	μA	0V < V _{IN} < V _{CC}	9
		5.5V	-1	-8	-3.8	μA	0V < V _{IN} < V _{CC}	9
T _{POR}	Power On Reset	3.5V	3.0	24	7	ms		
		5.5V	2.0	13	4	ms		
V _{LV}	Auto Reset Voltage		2.3	3.0	2.8	V		1,7

Notes:

1. Device does function down to the Auto Reset voltage.
2. GND=0V
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V and the V_{CC} voltage specification of 3.5V guarantees only 3.5V.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1 = CL2 = 22 pF
6. Same as note [4] except inputs at V_{CC}.
7. Max. temperature is 70°C.
8. STD Mode (not Low EMI Mode)
9. Auto Latch (mask option) selected
10. For analog comparator inputs when analog comparators are enabled.
11. Clock must be forced Low, when XTAL1 is clock driven and XTAL2 is floating.
12. Typicals are at V_{CC} = 5.0V and V_{CC} = 3.5V
13. Z86E43/743/E44 only.
14. WDT running

$T_A = -40\text{ }^\circ\text{C to } +105\text{ }^\circ\text{C}$								
Sym	Parameter	V_{CC} Note [3]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	4.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.5	V	Driven by External Clock Generator	
		5.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.5	V		
V_{CL}	Clock Input Low Voltage	4.5V	GND-0.3	$0.2 V_{CC}$	1.5	V	Driven by External Clock Generator	
		5.5V	GND-0.3	$0.2 V_{CC}$	1.5	V		
V_{IH}	Input High Voltage	4.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.5	V		
		5.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.5	V		
V_{IL}	Input Low Voltage	4.5V	GND-0.3	$0.2 V_{CC}$	1.5	V		
		5.5V	GND-0.3	$0.2 V_{CC}$	1.5	V		
V_{OH}	Output High Voltage Low EMI Mode	4.5V	$V_{CC}-0.4$		4.8	V	$I_{OH} = -0.5\text{ mA}$	8
		5.5V	$V_{CC}-0.4$		4.8	V	$I_{OH} = -0.5\text{ mA}$	8
V_{OH1}	Output High Voltage	4.5V	$V_{CC}-0.4$		4.8	V	$I_{OH} = -2.0\text{ mA}$	8
		5.5V	$V_{CC}-0.4$		4.8	V	$I_{OH} = -2.0\text{ mA}$	8
V_{OL}	Output Low Voltage Low EMI Mode	4.5V		0.4	0.2	V	$I_{OL} = +1.0\text{ mA}$	
		5.5V		0.4	0.2	V	$I_{OL} = +1.0\text{ mA}$	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	$I_{OL} = +4.0\text{ mA}$	8
		5.5V		0.4	0.1	V	$I_{OL} = +4.0\text{ mA}$	8
V_{OL2}	Output Low Voltage	4.5V		1.2	0.5	V	$I_{OL} = +12\text{ mA}$	8
		5.5V		1.2	0.5	V	$I_{OL} = +12\text{ mA}$	8
V_{RH}	Reset Input High Voltage	4.5V	$.8 V_{CC}$	V_{CC}	1.7	V		13
		5.5V	$.8 V_{CC}$	V_{CC}	2.1	V		13
V_{OLR}	Reset Output Low Voltage	4.5V		0.6	0.3	V	$I_{OL} = +1.0\text{ mA}$	13
		5.5V		0.6	0.2	V	$I_{OL} = +1.0\text{ mA}$	13
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25	10	mV		
		5.5V		25	10	mV		
V_{ICR}	Input Common Mode Voltage Range	4.5V	0	$V_{CC}-1.5V$		V		10
		5.5V	0	$V_{CC}-1.5V$		V		10
I_{IL}	Input Leakage	4.5V	-1	2	<1	μA	$V_{IN} = 0V, V_{CC}$	
		5.5V	-1	2	<1	μA	$V_{IN} = 0V, V_{CC}$	
I_{OL}	Output Leakage	4.5V	-1	2	<1	μA	$V_{IN} = 0V, V_{CC}$	
		5.5V	-1	2	<1	μA	$V_{IN} = 0V, V_{CC}$	
I_{IR}	Reset Input Current	4.5V	-18	-180	-112	μA		13
		5.5V	-18	-180	-112	μA		13
I_{CC}	Supply Current	4.5V		20	15	mA	@ 12 MHz	4,5
		5.5V		20	15	mA	@ 12 MHz	4,5
I_{CC1}	Standby Current Halt Mode	4.5V		6	2	mA	$V_{IN} = 0V, V_{CC}$ @ 12 MHz	4,5
		5.5V		6	4	mA	$V_{IN} = 0V, V_{CC}$ @ 12 MHz	4,5
I_{CC2}	Standby Current (Stop Mode)	4.5V		10	2	μA	$V_{IN} = 0V, V_{CC}$	6,11
		5.5V		10	3	μA	$V_{IN} = 0V, V_{CC}$	6,11
		4.5V		40	10	μA	$V_{IN} = 0V, V_{CC}$	6,11,14
		5.5V		40	10	μA	$V_{IN} = 0V, V_{CC}$	6,11,14

DC ELECTRICAL CHARACTERISTICS (Continued)

$T_A = -40\text{ }^\circ\text{C to } +105\text{ }^\circ\text{C}$

Sym	Parameter	V _{CC} Note [3]	Min	Max	Typical @ 25°C	Units	Conditions	Notes
I _{ALL}	Auto Latch Low Current	4.5V	1.4	20	4.7	μA	0V < V _{IN} < V _{CC}	9
		5.5V	1.4	20	4.7	μA	0V < V _{IN} < V _{CC}	9
I _{ALH}	Auto Latch High Current	4.5V	-1.0	-10	-3.8	μA	0V < V _{IN} < V _{CC}	9
		5.5V	-1.0	-10	-3.8	μA	0V < V _{IN} < V _{CC}	9
T _{POR}	Power On Reset	4.5V	2.0	14	4	ms		
		5.5V	2.0	14	4	ms		
V _{LV}	Auto Reset Voltage		2.0	3.3	2.8	V		1

1. Device does function down to the Auto Reset voltage.
2. GND=0V
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V ± 0.5V.
4. All outputs unloaded, I/O pins floating, inputs at rail.
5. CL1= CL2 = 22 pF
6. Same as note [4] except inputs at V_{CC}.
7. Maximum temperature is 70°C
8. STD Mode (not Low EMI Mode)
9. Auto Latch (mask option) selected
10. For analog comparator inputs when analog comparators are enabled.
11. Clock must be forced Low, when XTAL1 is clock driven and XTAL2 is floating.
12. Typicals are at V_{CC} = 5.0V
13. Z86E43/743/E44 only.
14. WDT is not running.

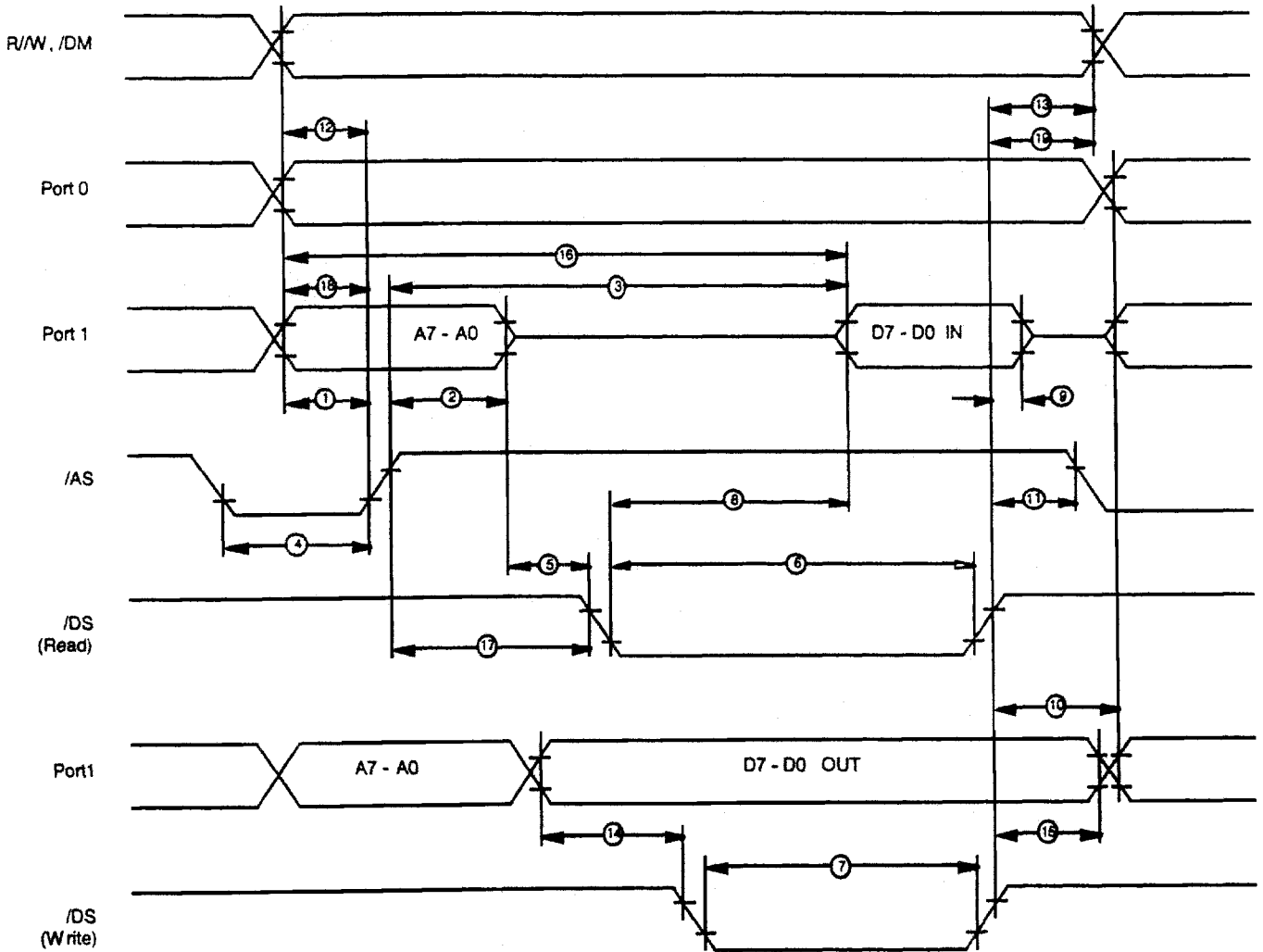


Figure 14. External I/O or Memory Read/Write Timing
(Z86E43/743/E44 Only)

DC ELECTRICAL CHARACTERISTICS (Continued)

				T _A = 0°C to 70°C 12 MHz			
No	Symbol	Parameter	Note [3] V _{CC}	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	3.5V	35		ns	2
			5.5V	35		ns	2
2	TdAS(A)	/AS Rise to Address Float Delay	3.5V	45		ns	2
			5.5V	45		ns	2
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid	3.5V		250	ns	1,2
			5.5V		250	ns	1,2
4	TwAS	/AS Low Width	3.5V	55		ns	2
			5.5V	55		ns	2
5	TdAS(DS)	Address Float to /DS Fall	3.5V	0		ns	
			5.5V	0		ns	
6	TwDSR	/DS (Read) Low Width	3.5V	200		ns	1,2
			5.5V	200		ns	1,2
7	TwDSW	/DS (Write) Low Width	3.5V	110		ns	1,2
			5.5V	110		ns	1,2
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid	3.5V		150	ns	1,2
			5.5V		150	ns	1,2
9	ThDR(DS)	Read Data to /DS Rise Hold Time	3.5V	0		ns	2
			5.5V	0		ns	2
10	TdDS(A)	/DS Rise to Address Active Delay	3.5V	45		ns	2
			5.5V	55		ns	2
11	TdDS(AS)	/DS Rise to /AS Fall Delay	3.5V	30		ns	2
			5.5V	45		ns	2
12	TdR/W(AS)	R/W Valid to /AS Rise Delay	3.5V	45		ns	2
			5.5V	45		ns	2
13	TdDS(R/W)	/DS Rise to R/W Not Valid	3.5V	45		ns	2
			5.5V	45		ns	2
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	3.5V	55		ns	2
			5.5V	55		ns	2
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	3.5V	45		ns	2
			5.5V	55		ns	2
16	TdA(DR)	Address Valid to Read Data Req'd Valid	3.5V		310	ns	1,2
			5.5V		310	ns	1,2
17	TdAS(DS)	/AS Rise to /DS Fall Delay	3.5V	65		ns	2
			5.5V	65		ns	2
18	TdDM(AS)	/DM Valid to /AS Rise Delay	3.5V	35		ns	2
			5.5V	35		ns	2
19	ThDS(AS)	/DS Valid to Address Valid Hold Time	3.5V	35		ns	2
			5.5V	35		ns	2

Notes:

1. When using extended memory timing, add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. The V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V and the V_{CC} voltage specification of 3.5V guarantees only 3.5V

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
 For Standard Mode (not Low-EMI Mode for outputs) with SMR D1 = 0, D0 = 0.

$T_A = -40^\circ\text{C to } 105^\circ\text{C}$
12 MHz

No	Symbol	Parameter	Note [3]		Max	Units	Notes
			V_{CC}	Min			
1	TdA(AS)	Address Valid to /AS Rise Delay	4.5V	35		ns	2
			5.5V	35			
2	TdAS(A)	/AS Rise to Address Float Delay	4.5V	45		ns	2
			5.5V	45			
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid	4.5V		250	ns	1,2
			5.5V		250		
4	TwAS	/AS Low Width	4.5V	55		ns	2
			5.5V	55			
5	TdAS(DS)	Address Float to /DS Fall	4.5V	0		ns	
			5.5V	0			
6	TwDSR	/DS (Read) Low Width	4.5V	200		ns	1,2
			5.5V	200			
7	TwDSW	/DS (Write) Low Width	4.5V	110		ns	1,2
			5.5V	110			
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid	4.5V		150	ns	1,2
			5.5V		150		
9	ThDR(DS)	Read Data to /DS Rise Hold Time	4.5V	0		ns	2
			5.5V	0			
10	TdDS(A)	/DS Rise to Address Active Delay	4.5V	45		ns	2
			5.5V	55			
11	TdDS(AS)	/DS Rise to /AS Fall Delay	4.5V	45		ns	2
			5.5V	45			
12	TdRW(AS)	R/W Valid to /AS Rise Delay	4.5V	45		ns	2
			5.5V	45			
13	TdDS(R/W)	/DS Rise to R/W Not Valid	4.5V	45		ns	2
			5.5V	45			
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	4.5V	55		ns	2
			5.5V	55			
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	4.5V	55		ns	2
			5.5V	55			
16	TdA(DR)	Address Valid to Read Data Req'd Valid	4.5V		310	ns	1,2
			5.5V		310		
17	TdAS(DS)	/AS Rise to /DS Fall Delay	4.5V	65		ns	2
			5.5V	65			
18	TdDM(AS)	/DM Valid to /AS Rise Delay	4.5V	35		ns	2
			5.5V	35			
19	ThDS(AS)	/DS Valid to Address Valid Hold Time	4.5V	35		ns	2
			5.5V	35			

Notes:

1. When using extended memory timing, add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. The V_{CC} voltage specification of 5.5V guarantees $5.0V \pm 0.5V$ and the V_{CC} voltage specification of 3.5V guarantees only 3.5V

Standard Test Load

All timing references use 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
For Standard Mode (not Low-EMI Mode for outputs) with SMR, D1 = 0, D0 = 0.

DC ELECTRICAL CHARACTERISTICS (Continued)

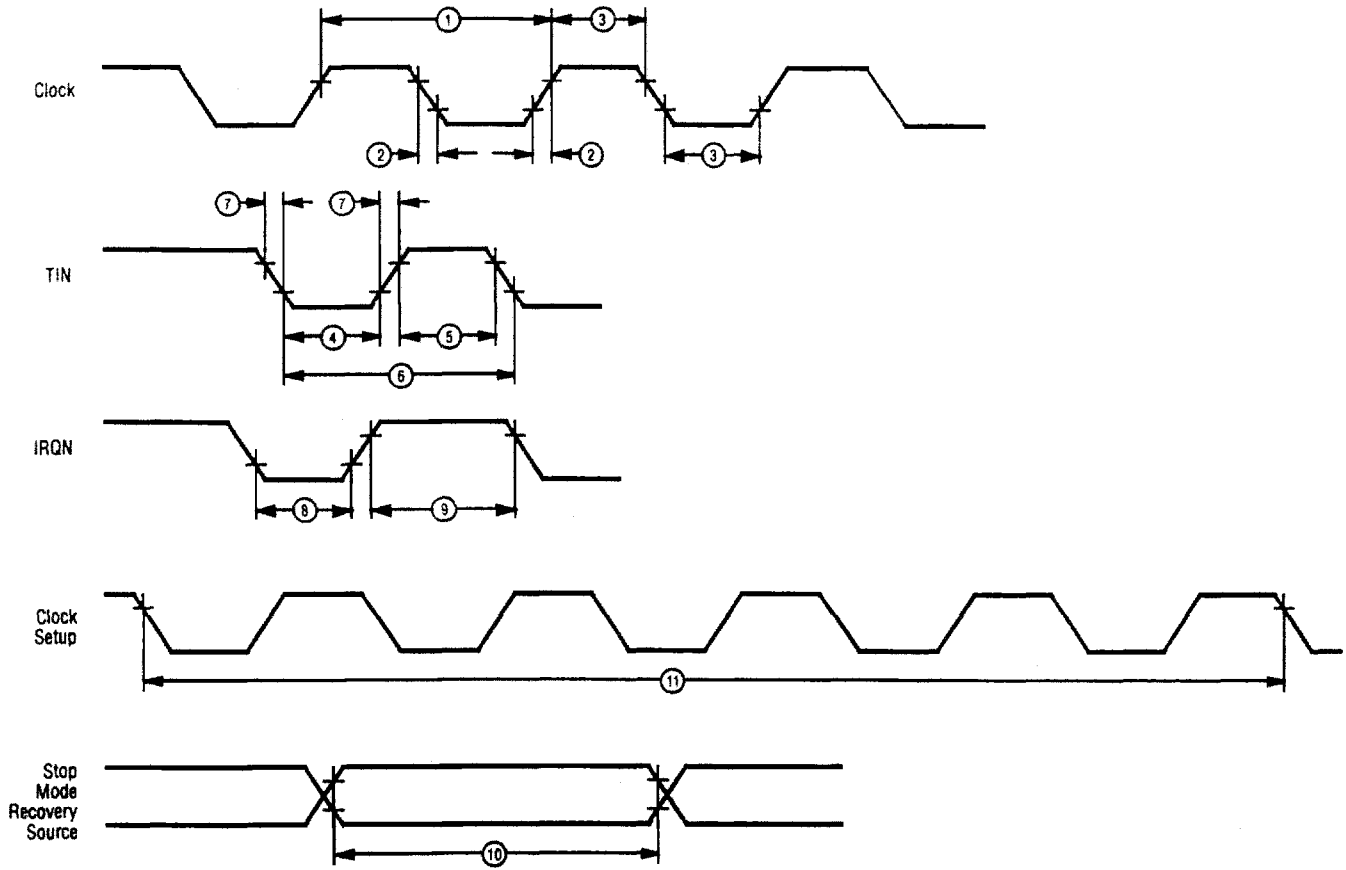


Figure 15. Additional Timing Diagram

Additional Timing Table (Divide-By-One Mode)

$T_A = 0\text{ }^\circ\text{C to }+70\text{ }^\circ\text{C}$									
4 MHz 6 MHz									
No	Symbol	Parameter	V_{CC} Note [6]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	3.5V	250	DC	166	DC	ns	1,7,8
			5.5V	250	DC	166	DC	ns	1,7,8
2	TrC, TfC	Clock Input Rise & Fall Times	3.5V		25		25	ns	1,7,8
			5.5V		25		25	ns	1,7,8
3	TwC	Input Clock Width	3.5V	100		100		ns	1,7,8
			5.5V	100		100		ns	1,7,8
4	TwTinL	Timer Input Low Width	3.5V	100		100		ns	1,7,8
			5.5V	70		70		ns	1,7,8
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC			1,7,8
			5.5V	5TpC		5TpC			1,7,8
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC			1,7,8
			5.5V	8TpC		8TpC			1,7,8
7	TrTin, TtTin	Timer Input Rise & Fall Timer	3.5V		100		100	ns	1,7,8
			5.5V		100		100	ns	1,7,8
8A	TwIL	Int. Request Low Time	3.5V	100		100		ns	1,2,7,8
			5.5V	70		70		ns	1,2,7,8
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC			1,3,7,8
			5.5V	5TpC		5TpC			1,3,7,8
9	TwiH	Int. Request Input High Time	3.5V	5TpC		5TpC			1,2,7,8
			5.5V	5TpC		5TpC			1,2,7,8
10	TwsM	STOP Mode	3.5V	12		12		ns	4,8
		Recovery Width Spec	5.5V	12		12		ns	4,8
11	Tost	Oscillator Startup Time	3.5V		5TpC		5TpC		4,8,9
			5.5V		5TpC		5TpC		4,8,9

Notes:

- Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
- Interrupt request via Port 3 (P31-P33).
- Interrupt request via Port 3 (P30).
- SMR-D5 = 1, POR STOP Mode Delay is on.
- Reg. WDTMR.
- The V_{CC} voltage specification of 5.5V guarantees 5.0V \pm 0.5V and the V_{CC} voltage specification of 3.5V guarantees 3.5V only.
- SMR D1 = 0.
- Maximum frequency for internal system clock is 4 MHz when using Low EMI OSC PCON Bit D7 = 0.
- For RC and LC oscillator, and for oscillator driven by clock driver.

Additional Timing Table (Divide-By-One Mode)

$T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$									
4 MHz 6 MHz									
No	Symbol	Parameter	V_{CC} Note [6]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	250	DC	166	DC	ns	1,7,8
			5.5V	250	DC	166	DC	ns	1,7,8
2	TrC, TfC	Clock Input Rise & Fall Times	4.5V		25		25	ns	1,7,8
			5.5V		25		25	ns	1,7,8
3	TwC	Input Clock Width	4.5V	100		100		ns	1,7,8
			5.5V	100		100		ns	1,7,8
4	TwTinL	Timer Input Low Width	4.5V	100		100		ns	1,7,8
			5.5V	70		70		ns	1,7,8
5	TwTinH	Timer Input High Width	4.5V	5TpC		5TpC			1,7,8
			5.5V	5TpC		5TpC			1,7,8
6	TpTin	Timer Input Period	4.5V	8TpC		8TpC			1,7,8
			5.5V	8TpC		8TpC			1,7,8
7	TrTin, Tftin	Timer Input Rise & Fall Timer	4.5V		100		100	ns	1,7,8
			5.5V		100		100	ns	1,7,8
8A	TwIL	Int. Request Low Time	4.5V	100		100		ns	1,2,7,8
			5.5V	70		70		ns	1,2,7,8
8B	TwIL	Int. Request Low Time	4.5V	5TpC		5TpC			1,3,7,8
			5.5V	5TpC		5TpC			1,3,7,8
9	TwIH	Int. Request Input High Time	4.5V	5TpC		5TpC			1,2,7,8
			5.5V	5TpC		5TpC			1,2,7,8
10	TwsM	STOP Mode	4.5V	12		12		ns	4,8
		Recovery Width Spec	5.5V	12		12		ns	4,8
11	Tost	Oscillator Startup Time	4.5V		5TpC		5TpC		4,8,9
			5.5V		5TpC		5TpC		4,8,9

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33).
3. Interrupt request via Port 3 (P30).
4. SMR-D5 = 1, POR STOP Mode Delay is on.
5. Reg. WDTMR.
6. The V_{CC} voltage specification of 5.5V guarantees 5.0V \pm 0.5V and the V_{CC} voltage specification of 3.5V guarantees 3.5V only.
7. SMR D1 = 0.
8. Maximum frequency for internal system clock is 4 MHz when using Low EMI OSC PCON Bit D7 = 0.
9. For RC and LC oscillator, and for oscillator driven by clock driver.

Handshake Timing Diagrams

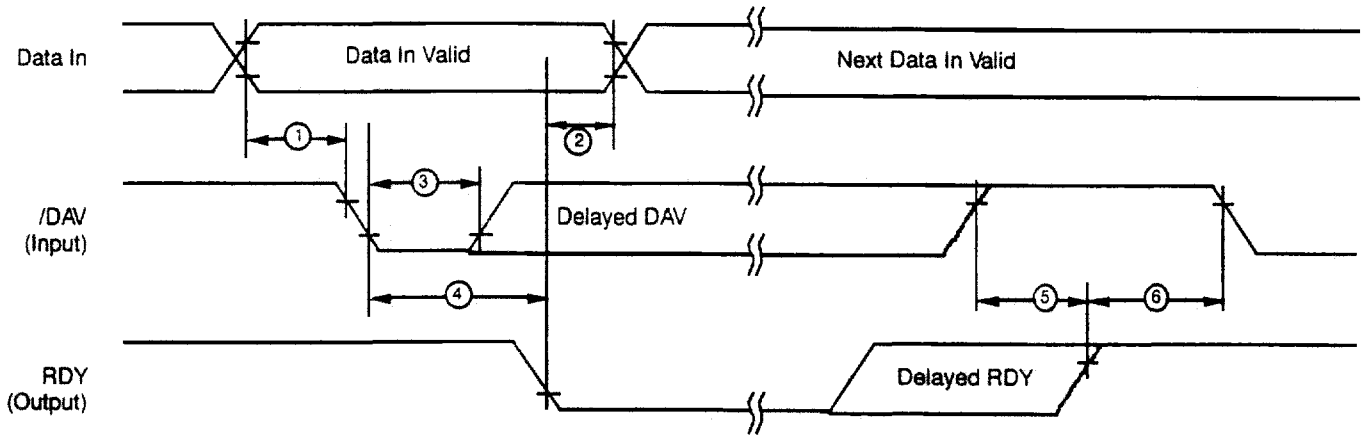


Figure 16. Input Handshake Timing

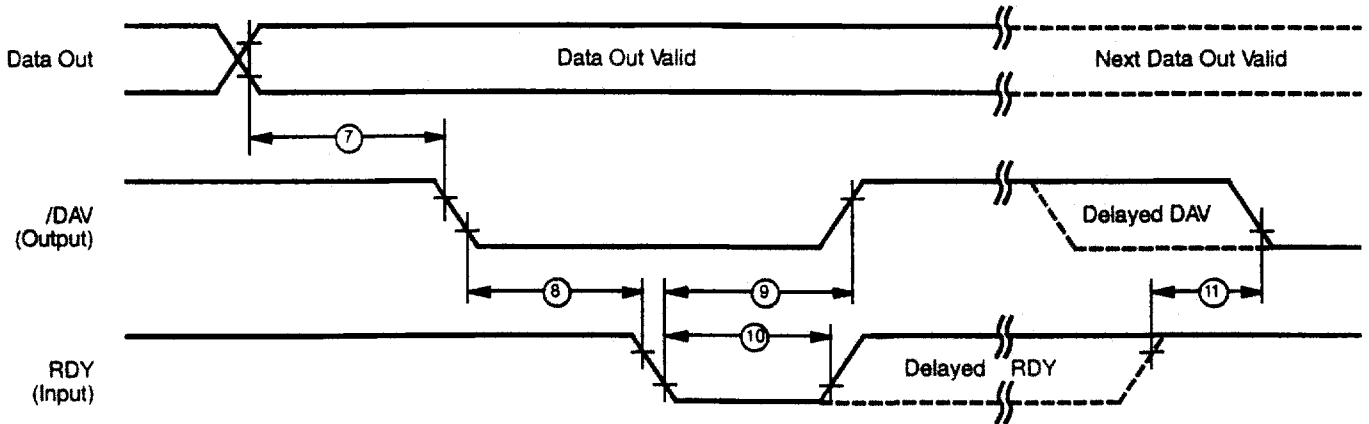


Figure 17. Output Handshake Timing

Additional Timing Table (Divide by Two Mode)

$T_A = 0\text{ }^\circ\text{C to } +70\text{ }^\circ\text{C}$										
12 MHz 4 MHz										
No	Symbol	Parameter	V_{CC} Note [6]	Min	Max	Min	Max	Units	Conditions	Notes
1	TpC	Input Clock Period	3.5V	62.5	DC	250	DC	ns		1,7,8
			5.5V	62.5	DC	250	DC	ns		1,7,8
2	TrC,TfC	Clock Input Rise & Fall Times	3.5V		15		25	ns		1,7,8
			5.5V		15		25	ns		1,7,8
3	TwC	Input Clock Width	3.5V	31		31		ns		1,7,8
			5.5V	31		31		ns		1,7,8
4	TwTinL	Timer Input Low Width	3.5V	70		70		ns		1,7,8
			5.5V	70		70		ns		1,7,8
5	TwTinH	Timer Input High Width	3.5V	5TpC		5TpC				1,7,8
			5.5V	5TpC		5TpC				1,7,8
6	TpTin	Timer Input Period	3.5V	8TpC		8TpC				1,7,8
			5.5V	8TpC		8TpC				1,7,8
7	TrTin, TfTin	Timer Input Rise & Fall Timer	3.5V		100		100	ns		1,7,8
			5.5V		100		100	ns		1,7,8
8A	TwIL	Int. Request Low Time	3.5V	70		70		ns		1,2,7,8
			5.5V	70		70		ns		1,2,7,8
8B	TwIL	Int. Request Low Time	3.5V	5TpC		5TpC				1,3,7,8
			5.5V	5TpC		5TpC				1,3,7,8
9	TwIH	Int. Request Input High Time	3.5V	5TpC		5TpC				1,2,7,8
			5.5V	5TpC		5TpC				1,2,7,8
10	Twsm	STOP Mode Recovery Width Spec	3.5V	12		12		ns		4,8
			5.5V	12		12		ns		4,8
11	Tost	Oscillator Startup Time	3.5V		5TpC		5TpC			4,8
			5.5V		5TpC		5TpC			4,8
12	Twdt	Watch-Dog Timer Delay Time Before Timeout	3.5V	10		10		ms	D0 = 0	5,11
			5.5V	5		5		ms	D1 = 0	5,11
			3.5V	20		20		ms	D0 = 1	5,11
			5.5V	10		10		ms	D1 = 0	5,11
			3.5V	40		40		ms	D0 = 0	5,11
			5.5V	20		20		ms	D1 = 1	5,11
			3.5V	160		160		ms	D0 = 1	5,11
			5.5V	80		80		ms	D1 = 1	5,11

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request via Port 3 (P31-P33)
3. Interrupt request via Port 3 (P30)
4. SMR-D5 = 1, POR STOP Mode Delay is on
5. Reg. WDTMR
6. The V_{CC} voltage specification of 5.5V guarantees 5.0V \pm 0.5V and the V_{CC} voltage specification of 3.5V guarantees 3.5V only.
7. SMR D1 = 0
8. Maximum frequency for internal system clock is 2 MHz when using Low EMI OSC PCON Bit D7 = 0.
9. For RC and LC oscillator, and for oscillator driven by clock driver.
10. Standard Mode (not Low EMI output ports)
11. Using internal RC

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