

SN54LS113A, SN54S113, SN74LS113A, SN74S113A

Dual J-K Negative-Edge-Triggered Flip-Flops with Preset

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset input sets the outputs regardless of the levels of the other inputs. When preset (PRE) is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

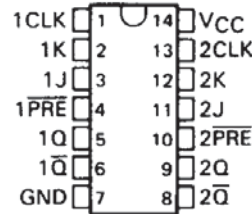
The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

SN54LS113A, SN54S113, SN74LS113A, SN74S113A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

D2661, APRIL 1982 - REVISED MARCH 1988

- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54LS113A, SN54S113 . . . J OR W PACKAGE
SN74LS113A, SN74S113A . . . D OR N PACKAGE
(TOP VIEW)

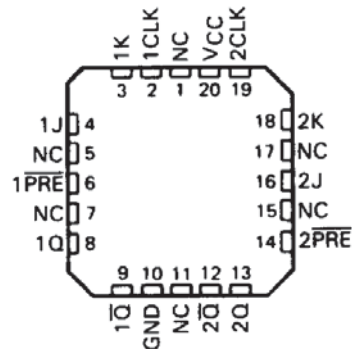


description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset input sets the outputs regardless of the levels of the other inputs. When preset ($\overline{\text{PRE}}$) is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

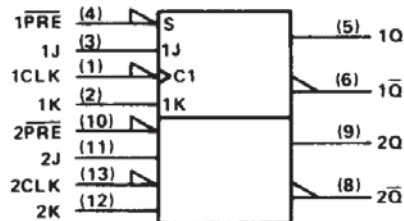
The SN54LS113A and SN54S113 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS113A and SN74S113A are characterized for operation from 0°C to 70°C .

SN54LS113A, SN54S113 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

FUNCTION TABLE (each flip-flop)

INPUTS				OUTPUTS	
PRE	CLK	J	K	Q	Q̄
L	X	X	X	H	L
H	↓	L	L	Q ₀	Q̄ ₀
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q ₀	Q̄ ₀

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

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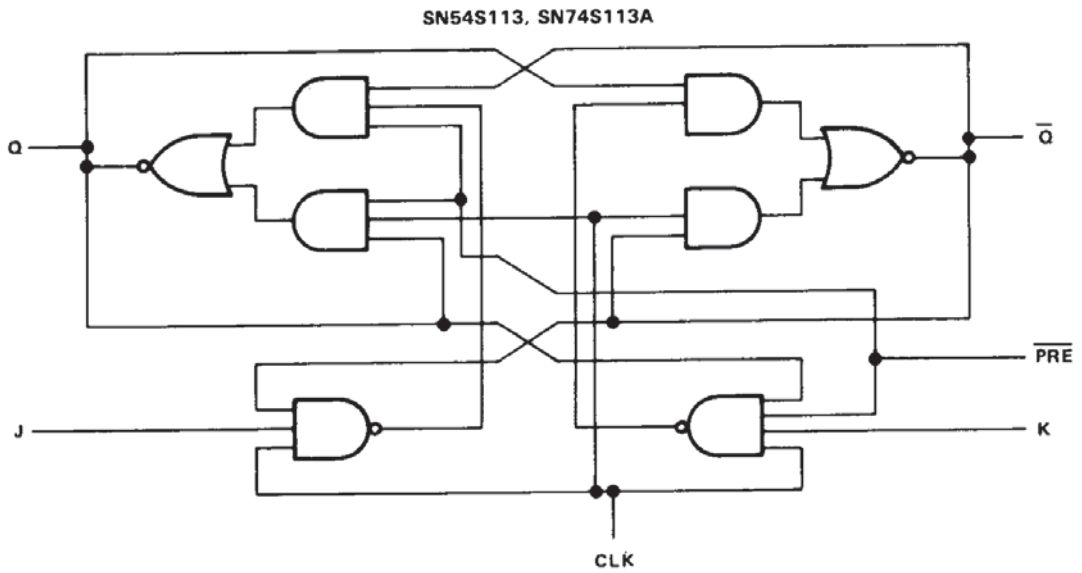
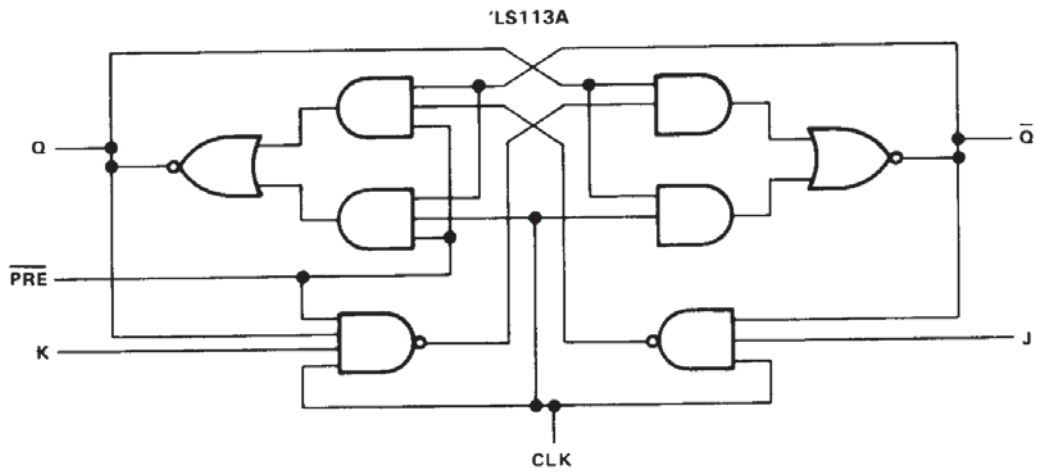
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TTL Devices

SN54LS113A, SN54S113, SN74LS113A, SN74S113A
DUAL J-K NEGATIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH PRESET

logic diagrams (positive logic)



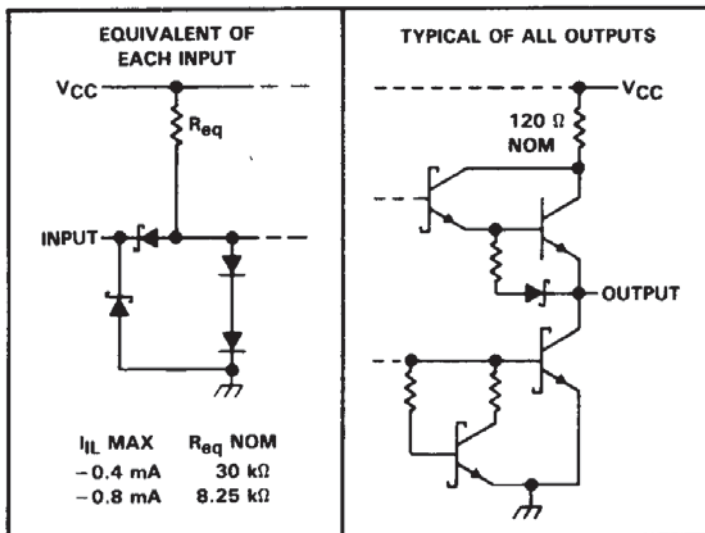
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TTL Devices

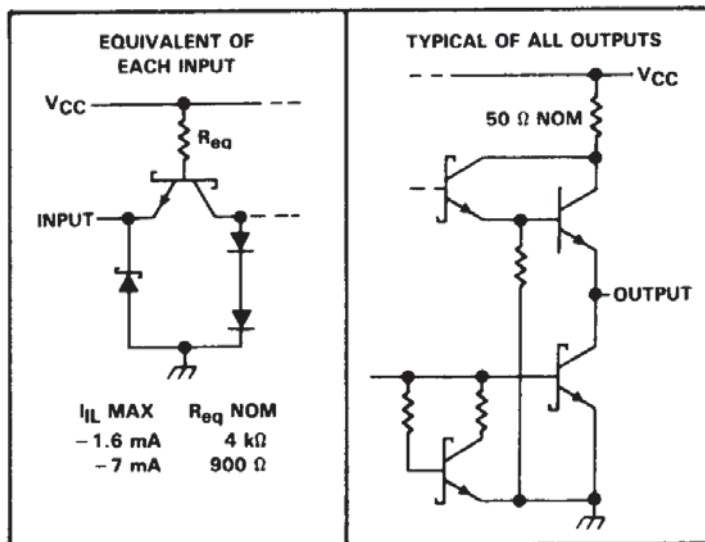
**SN54LS113A, SN74LS113A, SN54S113, SN74S113A
DUAL J-K NEGATIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH PRESET**

schematics of inputs and outputs

'LS113A



SN54S113, SN74S113A



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: 'LS113A	7 V
SN54S113, SN74S113A	5.5 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminals.

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TTL Devices

SN54LS113A, SN74LS113A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

recommended operating conditions

		SN54LS113A			SN74LS113A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			-0.4			-0.4	mA
I _{OL}	Low-level output current			4			8	mA
f _{clock}	Clock frequency	0		30	0		30	MHz
t _w	Pulse duration	CLK high		20			20	ns
		PRE or CLR low		25			25	
t _{su}	Set up time-before CLK↓	Data high or low		20			20	ns
		PRE inactive		20			20	
t _h	Hold time-data after CLK↓			0			0	ns
T _A	Operating free-air temperature	-55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TTL Devices

PARAMETER	TEST CONDITIONS†	SN54LS113A			SN74LS113A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -0.4 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 8 mA					0.35	0.5	
I _I	J or K			0.1			0.1	mA
	PRE	V _{CC} = MAX, V _I = 7 V		0.3			0.3	
	CLK			0.4			0.4	
I _{IH}	J or K			20			20	μA
	PRE	V _{CC} = MAX, V _I = 2.7 V		60			60	
	CLK			80			80	
I _{IL}	J or K			-0.4			-0.4	mA
	PRE or CLK	V _{CC} = MAX, V _I = 0.4 V		-0.8			-0.8	
I _{OS} §	V _{CC} = MAX, see Note 2	-20		-100	-20		-100	mA
I _{CC} (Total)	V _{CC} = MAX, see Note 3		4	6		4	6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTES: 2. For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the '54 family and the '74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

3. With all outputs open, I_{CC} is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.

SN54LS113A, SN74LS113A
DUAL J-K NEGATIVE-EDGE-TRIGGERED
FLIP-FLOPS WITH PRESET

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{\max}			$R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$	30	45		MHz
t_{PLH}	PRE or CLK	Q or \bar{Q}			15	20	ns
t_{PHL}					15	20	ns

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

SN54S113, SN74S113A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

recommended operating conditions

		SN54S113			SN74S113A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage	0.8			0.8			V
I _{OH}	High-level output current	-1			-1			mA
I _{OL}	Low-level output current	20			20			mA
t _w	Pulse duration	CLK high	6		6		ns	
		CLK low	6.5		6.5			
		PRE low	8		8			
t _{su}	Set up time-before CLK↓	Data high or low		7		ns		
t _h	Hold time-data after CLK↓	0		0		ns		
T _A	Operating free-air temperature	-55	125		0	70		°C

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TTL Devices

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S113			SN74S113A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA	-1.2			-1.2			V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -1 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA	0.5			0.5			V
I _I	V _{CC} = MAX, V _I = 5.5 V	1			1			mA
I _{IH}	J or K	50			50			μA
	PRE or CLK	100			100			
I _{IL}	J or K	-1.6			-1.6			mA
	PRE‡	-7			-7			
	CLK‡	-4			-4			
I _{OS} †	V _{CC} = MAX	-40	-100		-40	-100		mA
I _{CC} #	V _{CC} = MAX, see Note 3	15 25			15 25			mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Clear is tested with preset high and preset is tested with clear high.

¶ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

Values are average per flip-flop.

NOTE 3: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			R _L = 280 Ω, C _L = 15 pF	80	125		MHz
t _{PLH}	PRE	Q or \bar{Q}			4	7	ns
t _{PHL}	PRE (CLK high)	\bar{Q} or Q			5	7	ns
	PRE (CLK low)				5	7	
t _{PLH}	CLK	Q or \bar{Q}			4	7	ns
t _{PHL}						5	7

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.