40085B/74C85/54C85

4-BIT MAGNITUDE COMPARATOR

DESCRIPTION – The 40085B is a 4-Bit Magnitude Comparator which compares two 4-bit words (A, B), each word having four Parallel Inputs (A_0-A_3,B_0-B_3); A_3,B_3 being the most significant inputs. Operation is not restricted to binary codes, the device will work with any monotonic code. Three Outputs are provided: "A greater than B" ($O_{A>B}$), "A less than B" ($O_{A<B}$), "A equal to B" ($O_{A=B}$). Three Expander Inputs, $I_{A>B}$, $I_{A<B}$, $I_{A=B}$, allow cascading without external gates. For proper compare operation the Expander Inputs to the least significant position must be connected as follows: $I_{A<B} = I_{A>B} = L$, $I_{A=B} = H$. For serial (ripple) expansion, the $O_{A>B}$, $O_{A<B}$ and $O_{A=B}$ Outputs are connected respectively to the $I_{A>B}$, $I_{A<B}$, and $I_{A=B}$ inputs of the next most significant comparator, as shown in Figure 1. Refer to Applications section of data sheet for high speed method of comparing large words.

The Truth Table on the following page describes the operation of the 40085B under all possible logic conditions. The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a series expansion scheme. The lower five lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

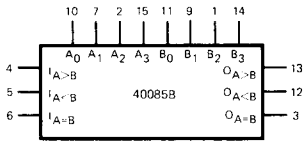
The 40085B is a direct replacement for the 74C85/54C85.

- **EASILY EXPANDABLE**
- **BINARY OR BCD COMPARISON**
- **$O_{A>B}$, $O_{A<B}$, AND $O_{A=B}$ OUTPUTS AVAILABLE**

PIN NAMES

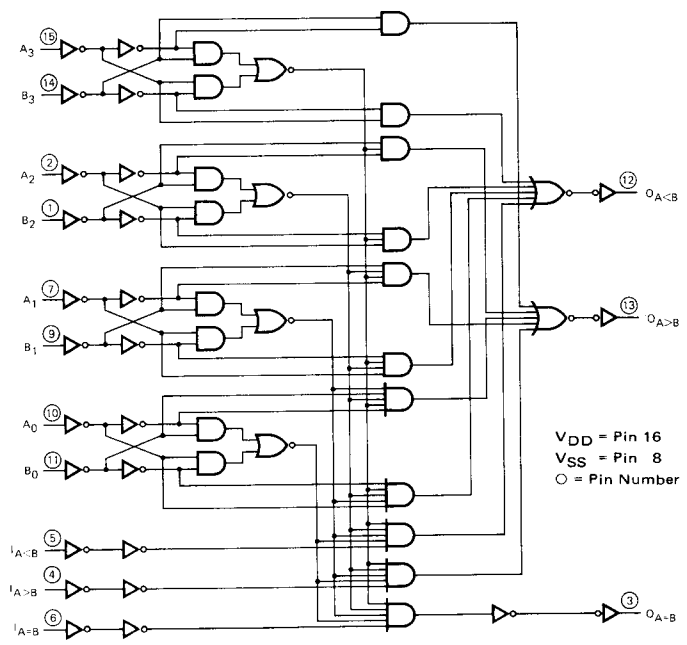
A_0-A_3	Word A Parallel Inputs
B_0-B_3	Word B Parallel Inputs
$I_{A>B}$, $I_{A<B}$, $I_{A=B}$	Expander Inputs
$O_{A>B}$	A Greater than B Output
$O_{A<B}$	A Less than B Output
$O_{A=B}$	A Equal to B Output

LOGIC SYMBOL



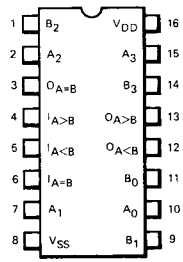
V_{DD} = Pin 16
V_{SS} = Pin 8

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

7

TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	H	L	H	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	H	H	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	H	H	H	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	H	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	L	L	L

H = HIGH Level
L = LOW Level
X = Don't Care

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

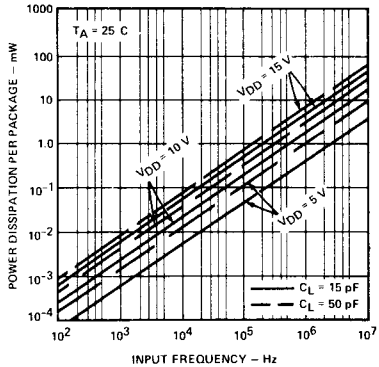
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		180	335		70	140		50	112	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PHL}	A_n or B_n to any Output		180	335		70	140		50	112		
t_{PLH}	Propagation Delay,		135	275		55	120		40	96	ns	
t_{PHL}	Any I to any Output		135	275		55	120		40	96		
t_{TLH}	Output Transition Time		60	135		30	70		20	45	ns	
t_{THL}			60	135		30	70		20	45		

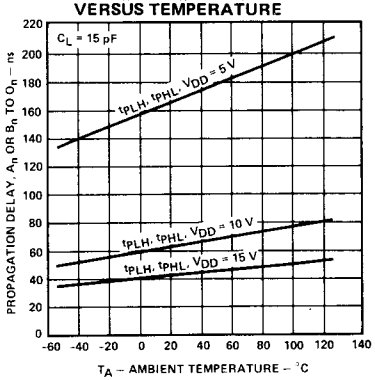
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

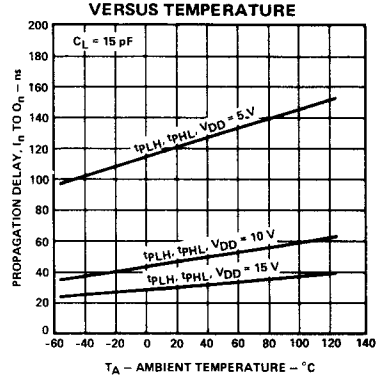
POWER DISSIPATION VERSUS FREQUENCY



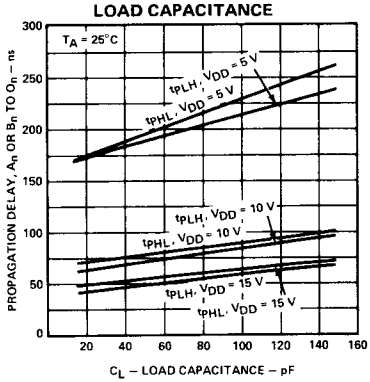
PROPAGATION DELAY A_n OR B_n TO O_n, VERSUS TEMPERATURE



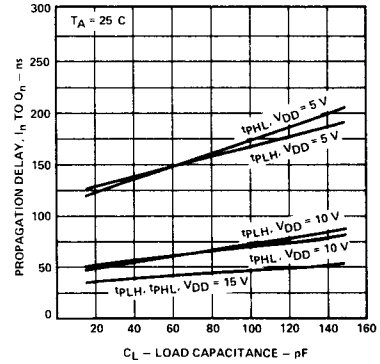
PROPAGATION DELAY I_n TO O_n VERSUS TEMPERATURE



PROPAGATION DELAY A_n OR B_n TO O_n VERSUS LOAD CAPACITANCE



PROPAGATION DELAY I_n TO O_n VERSUS LOAD CAPACITANCE



7

APPLICATIONS

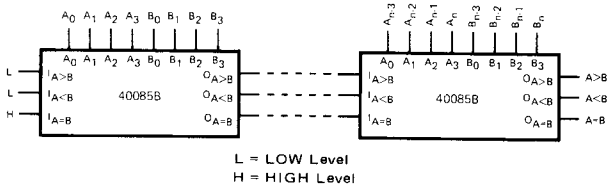


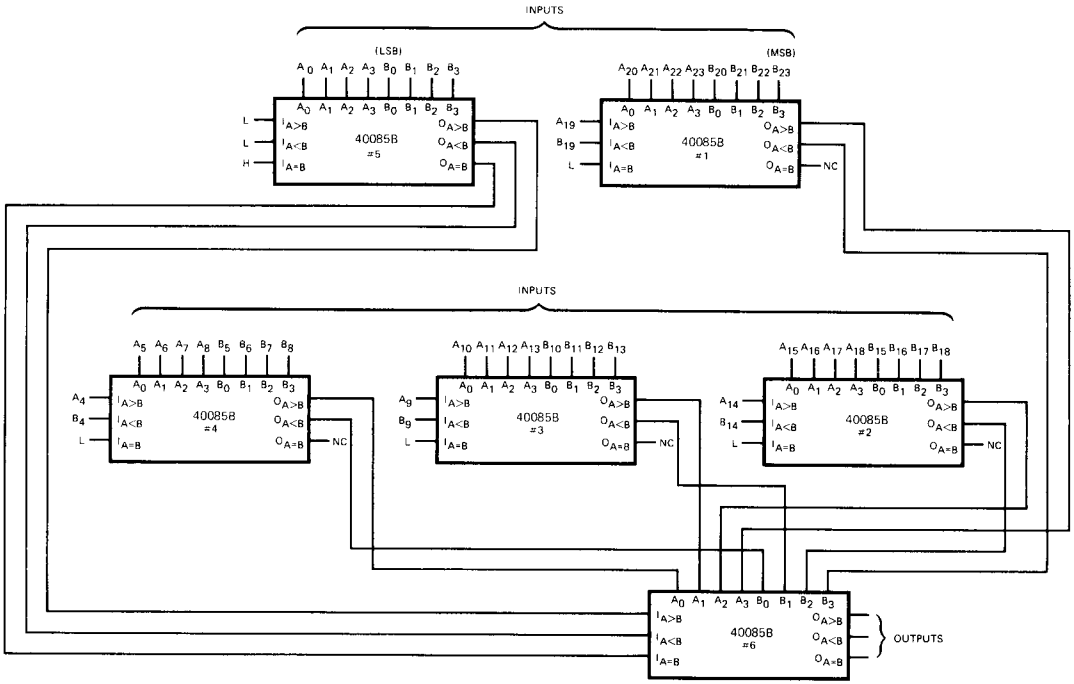
Fig. 1. COMPARING TWO n-BIT WORDS

Figure 2 shows a high speed method of comparing two 24-bit words with only two levels of device delay. With the technique shown in Figure 1, six levels of device delay result when comparing two 24-bit words. The parallel technique can be expanded to any number of bits, see Table I.

TABLE I

WORD LENGTH	NUMBER OF PKGS.
1-4 Bits	1
5-24 Bits	2 - 6
25-120 Bits	8 - 31

NOTE:
The F40085 can be used as a 5-bit comparator only when the outputs are used to drive the A_0-A_3 and B_0-B_3 inputs of another 40085B as shown in Figure 2 in positions #1, 2, 3, and 4.



MSB = Most Significant Bit
LSB = Least Significant Bit

L = LOW Level
H = HIGH Level
NC = No Connection

Fig. 2. COMPARISON OF TWO 24-BIT WORDS