STK1390

CMOS nvSRAM / RTC
8K x 8 Nonvolatile Static RAM with Real Time Clock

PRELIMINARY

FEATURES

- **Solid-state nonvolatile SRAM/RTC solution - no batteries required**
- **Ideal for metering applications**
- **25, 30, 35 and 45 ns SRAM read/write access**
- **NOVCEL™ technology - true nonvolatile RAM**
- **Software or hardware controlled nonvolatile cycles**
- **10 year data retention from each Store cycle**
- **Full-featured Real Time Clock on-chip**
- **RTC operates from external capacitor - typical 1 month operation from 0.47F supercap**
- **Uses standard 32.768kHz Watch Crystal**
- **Commercial and industrial temperature grades**
- **32-pin DIP or 400 mil SOIC package**

DESCRIPTION

The Simtek STK1390 contains both a fast static RAM with nonvolatile EEPROM shadow and a monolithic real time clock. The SRAM can be read and written an unlimited number of times while independent nonvolatile data resides in EEPROM. Transfers between the EEPROM and the SRAM are controlled by either hardware or software. The real time clock information consists of an additional 64 8-bit registers. The lower 12 registers are used for time information and RTC configuration. The upper 52 registers can be used for user information and are shadowed by EEPROM. The registers are accessible through the SRAM I/O pins by asserting the CK input in conjunction with the chip select pins. Addresses A_0 - A_5 are used for register selection.

The STK1390 is designed to support long-term, unpowered operation of the RTC from a capacitor, eliminating the need for batteries. When a low power condition is detected (VCC < 4.2V) the STK1390 switches its power source to the capacitor, isolating the RTC from the SRAM.

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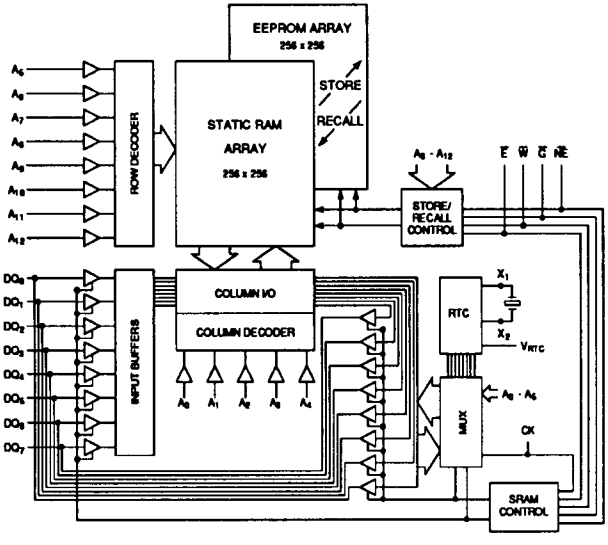
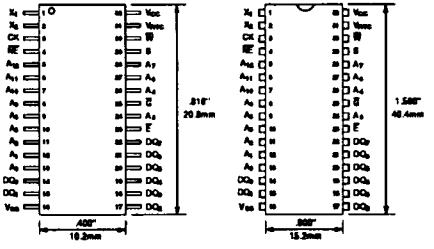
LOGIC BLOCK DIAGRAM



PINOUTS AND PACKAGES



A_0 - A_{12}	Address Inputs
$\overline{W}$	Write Enable
DQ_0 - DQ_7	Data In/Out
$\overline{E}$	Chip Enable
S	Chip Select
$\overline{NE}$	Nonvolatile Enable
$\overline{G}$	Output Enable
CK	RTC Control
V_{CC}	Power (+5V)
V_{SS}	Ground
V_{RTC}	Capacitor Input

ABSOLUTE MAXIMUM RATINGS[a]

Voltage on typical input relative to V_{SS} ..... –0.6V to 7.0V
Voltage on DQ_{0-7} and $\overline{G}$ ..... –0.5V to (V_{CC}+0.5V)
Temperature under bias ..... –55°C to 125°C
Storage temperature ..... –65°C to 150°C
Power dissipation 1W
DC output current 15mA
(One output at a time, one second duration)

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC_1}[b]	Average V_{CC} Current		85		95	mA	t_{AVAV} = 25ns
			80		85	mA	t_{AVAV} = 30ns
			75		80	mA	t_{AVAV} = 35ns
			65		75	mA	t_{AVAV} = 45ns
I_{CC_2}[d]	Average V_{CC} Current during *STORE* cycle		50		50	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ or $S \leq (V_{SS} + 0.2V)$ all others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{SB_1}[c]	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		30		34	mA	t_{AVAV} = 25ns
			27		30	mA	t_{AVAV} = 30ns
			23		27	mA	t_{AVAV} = 35ns
			20		23	mA	t_{AVAV} = 45ns $\overline{E} \geq V_{IH}$ or $S \leq V_{IL}$; all others cycling
I_{SB_2}[c]	Average V_{CC} Current (Standby, Stable CMOS Input Levels)		1		1	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ or $S \leq (V_{SS} + 0.2V)$ all others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current (Any Input)		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		±5		±5	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
V_{IH}	Input Logic "1" Voltage	2.2	V_{CC}+.5	2.2	V_{CC}+.5	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS}–.5	0.8	V_{SS}–.5	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	I_{OUT} = –4mA
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	I_{OUT} = 8mA
T_A	Operating Temperature	0	70	–40	85	°C	

Note b: I_{CC_1} is dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note c: Bringing $\overline{E} \geq V_{IH}$ or $S \leq V_{IL}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.
Note d: I_{CC_2} is the average current required for the duration of the store cycle (t_{STORE}) after the sequence (t_{WC}) that initiates the cycle.

AC TEST CONDITIONS

Input Pulse Levels ..... V_{ss} to 3V
Input Rise and Fall Times ..... ≤ 5ns
Input and Output Timing Reference Levels 1.5V
Output Load ..... See Figure 1

CAPACITANCE (T_A=25°C, f=1.0MHz)[e]

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note e: These parameters are guaranteed but not tested.

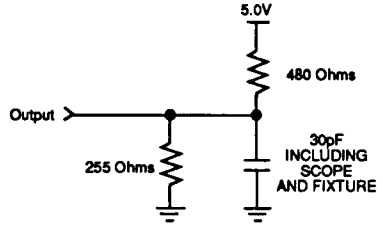


Figure 1: AC Output Loading

READ CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS		PARAMETER	STK13C68-25		STK13C68-30		STK13C68-35		STK13C68-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELQV}, t_{SHQV}	t_{ACS}	Chip Enable Access Time		25		30		35		45	ns
2	t_{AVAVR}[g]	t_{RC}	Read Cycle Time	25		30		35		45		ns
3	t_{AVQV}[h]	t_{AA}	Address Access time		25		30		35		45	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		12		15		20		25	ns
5	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		5		5		ns
6	t_{ELQX}, t_{SHQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		5		ns
7	t_{EHQZ}[i], t_{SLQZ}[i]	t_{HZ}	Chip Disable to Output Inactive	13		15		15		20		ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		0		ns
9	t_{GHQZ}[i]	t_{OHZ}	Output Disable to Output Inactive	13		15		15		20		ns
10	t_{ELICCH}[e], t_{SHICCH}[e]	t_{PA}	Chip Enable to Power Active	0		0		0		0		ns
11	t_{EHICCL}[c,e], t_{SLICCL}[c,e]	t_{PS}	Chip Disable to Power Standby		25		25		25		25	ns
11A	t_{WHQV}	t_{WR}	Write Recovery Time		30		35		45		55	ns

Note c: Bringing $\overline{E}$ high or S low will not produce standby currents until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.
Note e: Parameter guaranteed but not tested.
Note g: For READ CYCLE #1 and #2, $\overline{W}$ must be high for entire cycle.
Note h: Device is continuously selected with $\overline{E}$ low, S high and $\overline{G}$ low.
Note i: Measured ± 200mV from steady state output voltage.

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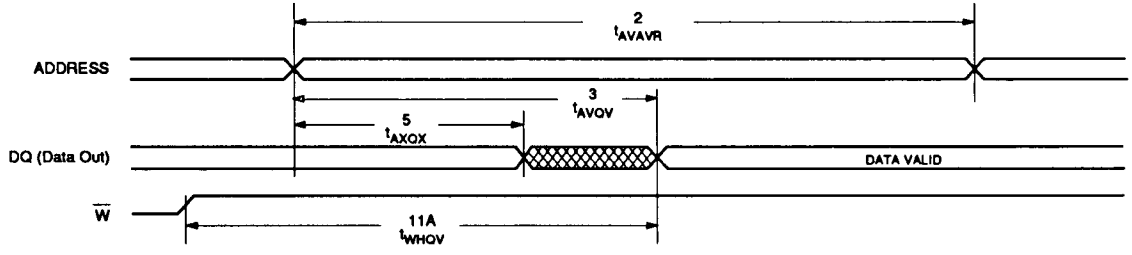
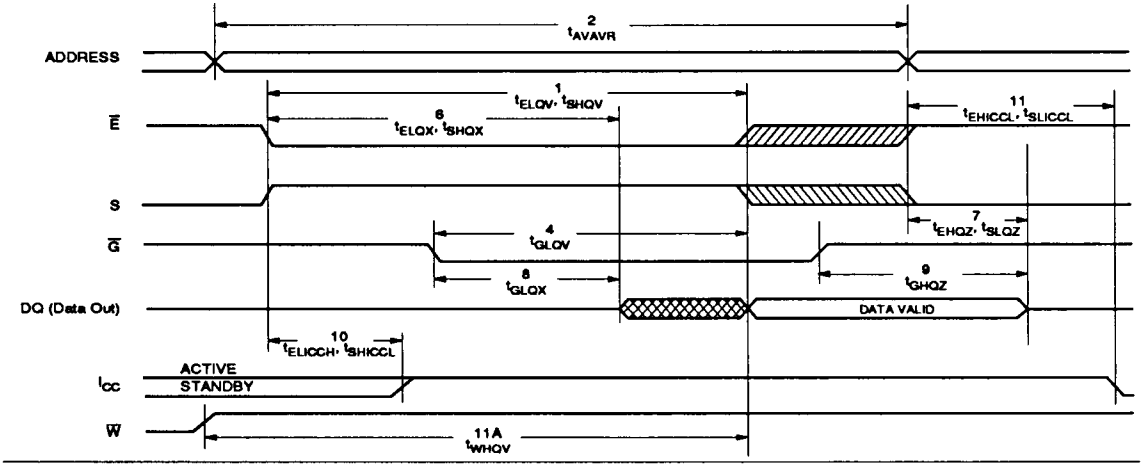
READ CYCLE #1 [g,h]



READ CYCLE #2 [g]



WRITE CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS			PARAMETER	STK13C68-25		STK13C68-30		STK13C68-35		STK13C68-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAVW}	t_{AVAVW}	t_{WC}	Write Cycle Time	25		30		35		45		ns
13	t_{WLWH}	t_{WLEH}, t_{WLSL}	t_{WP}	Write Pulse Width	20		25		30		35		ns
14	t_{ELWH}	t_{ELEH}, t_{SHSL}	t_{CW}	Chip Enable to End of Write	20		25		30		35		ns
15	t_{DVWH}	t_{DVEH}, t_{DVSL}	t_{DW}	Data Set-up to End of Write	12		15		15		20		ns
16	t_{WHDX}	t_{EHDX}, t_{SLDX}	t_{DH}	Data Hold After End of Write	0		0		0		0		ns
17	t_{AVWH}	t_{AVEH}, t_{AVSL}	t_{AW}	Address Set-up to End of Write	20		25		30		35		ns
18	t_{AVWL}	t_{AVEL}, t_{AVSH}	t_{AS}	Address Set-up to Start of Write	0		0		0		0		ns
19	t_{WHAX}	t_{EHAX}, t_{SLAX}	t_{WR}	Address Hold After End of Write	0		0		0		0		ns
20	t_{AVAVW}	t_{AVAVW}	t_{WC}	Write Cycle Time	45		45		45		45		ns
21	t_{WLWH}	t_{WLEH}, t_{WLSL}	t_{WP}	Write Pulse Width	35		35		35		35		ns
22	t_{WLOZ}[l,m]		t_{WZ}	Write Enable to Output Disable		35		35		35		35	ns
23	t_{WHQX}		t_{OW}	Output Active After End of Write	5		5		5		5		ns

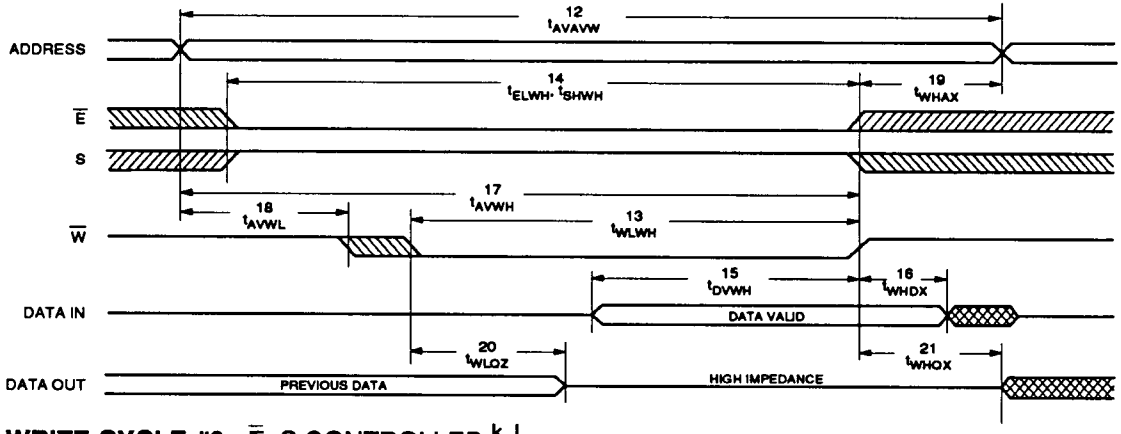
Note l: Measured ±200mV from steady state output voltage.

Note l: Spec. numbers 12 to 19 apply when $\overline{G}$ is high during the write cycle.

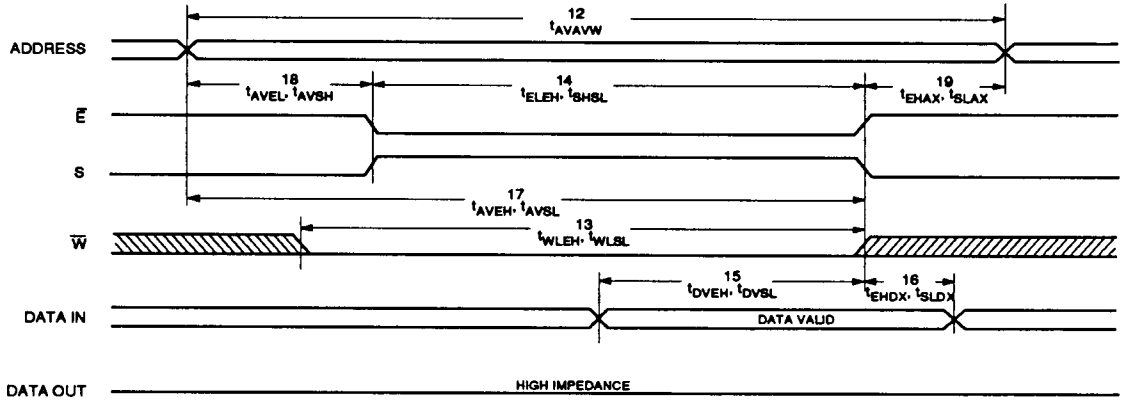
Note k: $\overline{E}$ or $\overline{W}$ must be ≥ high or S must be low during address transitions.

Note m: If $\overline{W}$ is low when either $\overline{E}$ goes low or S goes high, the outputs remain in the high impedance state.

WRITE CYCLE #1: $\overline{W}$ CONTROLLED [k, l]



WRITE CYCLE #2: $\overline{E}$, S CONTROLLED [k, l]



NONVOLATILE MEMORY OPERATION

MODE SELECTION

S	$\overline{E}$	$\overline{W}$	A_{12} - A_0(hex)	MODE	I/O	POWER	NOTES
L	X	X	X	Not Selected	Output High Z	Standby	
X	H	X	X	Not Selected	Output High Z	Standby	
H	L	H	X	Read SRAM	Output Data	Active	o
H	L	L	X	Write SRAM	Input Data	Active	
H	L	H	0000	Read SRAM	Output Data	Active	n,o
			1555	Read SRAM	Output Data		n,o
			0AAA	Read SRAM	Output Data		n,o
			1FFF	Read SRAM	Output Data		n,o
			10F0	Read SRAM	Output Data		n,o
			0F0F	Nonvolatile *STORE*	Output High Z	I_{CC_2}	n
H	L	H	0000	Read SRAM	Output Data	Active	n,o
			1555	Read SRAM	Output Data		n,o
			0AAA	Read SRAM	Output Data		n,o
			1FFF	Read SRAM	Output Data		n,o
			10F0	Read SRAM	Output Data		n,o
			0F0E	Nonvolatile *RECALL*	Output High Z		n

Note: n: The six consecutive addresses must be in order listed - (0000, 1555, 0AAA, 1FFF, 10F0, 70F) for a *STORE* cycle or (0000, 1555, 0AAA, 1FFF, 10F0, 0F0E for a *RECALL* cycle. $\overline{W}$ must be high during all six consecutive cycles. See *STORE* cycle and *RECALL* cycle tables and diagrams for further details.

Note o: I/O state assumes that $\overline{G} \leq V_{IL}$. Initiation and operation of nonvolatile cycles does not depend on the state of $\overline{G}$.

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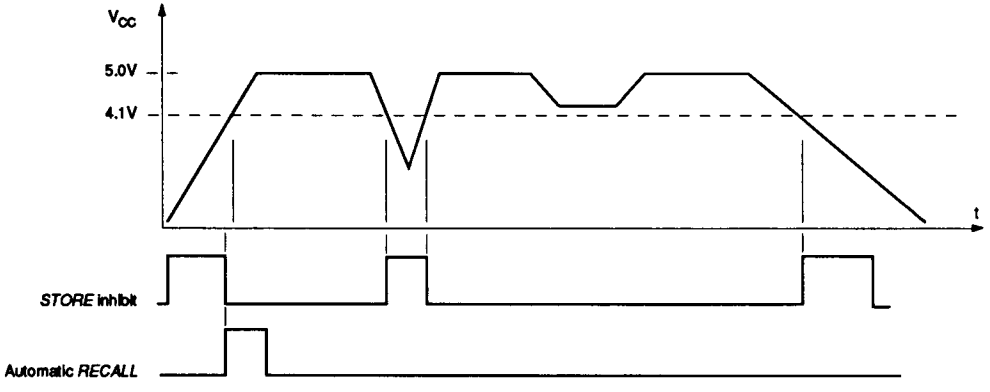
STORE CYCLE INHIBIT and AUTOMATIC POWER-UP *RECALL*



STORE/RECALL CYCLE

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS		PARAMETER	STK13C68-25		STK13C68-30		STK13C68-35		STK13C68-45		UNITS
	#1	#2		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
24	t_{AVAVN}	t_{RC}	*STORE/RECALL* Initiation Cycle Time	25		30		35		45		ns
25	t_{ELQZ}[p], t_{SHQZ}[p]		Chip Enable to Output Inactive		75		75		75		75	ns
26	t_{ELQXS}, t_{SHQXS}	t_{STORE}[q]	*STORE* Cycle Time		10		10		10		10	ms
27	t_{ELQXR}, t_{SHQXR}	t_{RECALL}[r]	*RECALL* Cycle Time		20		20		20		20	µs
28	t_{AVELN}[s], t_{AVSHN}	t_{AE}	Address Set-up to Chip Enable	0		0		0		0		ns
29	t_{ELEHN}[s,t], t_{SHSLN}	t_{EP}	Chip Enable Pulse Width	15		20		25		35		ns
30	t_{EHAXN}[s]	t_{EA}	Chip Disable to Address Change	0		0		0		0		ns

Note p: Once the software *STORE* or *RECALL* cycle is initiated, it completes automatically, ignoring all inputs.

Note q: Note th, t_{SLAXN}at *STORE* cycles (but not *RECALLs*) are aborted by V_{CC} < 4.1V (*STORE* inhibit).

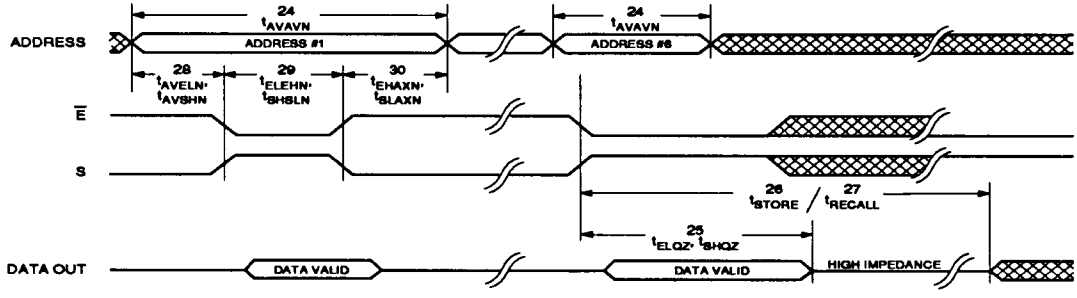
Note r: A *RECALL* cycle is initiated automatically at power up when V_{CC} exceeds 4.1V. t_{RECALL} is measured from the point at which V_{CC} exceeds 4.5V.

Note s: Noise on the $\overline{E}$ pin or S pin may trigger multiple read cycles from the same address and abort the address sequence.

Note t: If the Chip Enable Pulse Width is less than t_{ELQV} or t_{SHQV} (see READ CYCLE #2) but greater than or equal to t_{ELEHN} or t_{SHSLN}, then the data may not be valid at the end of the low pulse, however the *STORE* or *RECALL* will still be initiated.

Note u: $\overline{W}$ must be HIGH when $\overline{E}$ is LOW and S is high during the address sequence in order to initiate a nonvolatile cycle. $\overline{G}$ may be either HIGH or LOW throughout. Addresses #1 through #6 are found in the MODE SELECTION table. Address #6 determines whether the STK13C68 performs a *STORE* or *RECALL*.

STORE/RECALL CYCLE [u]



DEVICE OPERATION

The STK13C68 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as an ordinary static RAM. In nonvolatile operation, data is transferred from SRAM to EEPROM or from EEPROM to SRAM. In this mode SRAM functions are disabled.

SRAM READ

The STK13C68 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are LOW while $\overline{W}$ and S are HIGH. The address specified on pins A_{0-12} determines which of the 8192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ CYCLE #1). If the READ is initiated by S, $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{SHQV}, t_{ELQV} or t_{GLQV}, whichever is later (READ CYCLE #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought HIGH or S or $\overline{W}$ is brought LOW.

SRAM WRITE

A write cycle is performed whenever $\overline{E}$ and $\overline{W}$ are LOW and S is HIGH. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ go HIGH or S goes LOW at the end of the cycle. The data on pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} (t_{DVSL}) before the end of an $\overline{E}$ (S) controlled WRITE.

It is recommended that $\overline{G}$ be kept HIGH during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{G}$ is left LOW, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes LOW.

NONVOLATILE STORE

The STK13C68 *STORE* cycle is initiated by executing sequential READ cycles from six specific address locations. By relying on READ cycles only, the STK13C68 implements nonvolatile operation while remaining pin-for-pin compatible with standard 8Kx8 SRAMs. During the *STORE* cycle, an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile elements. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of reads from specific addresses is used for *STORE* initiation, it is important that no other read or write accesses intervene in the sequence or the sequence will be aborted and no *STORE* or *RECALL* will take place.

To initiate the *STORE* cycle the following READ sequence must be performed:

1.	Read address	0000 (hex)	Valid READ
2.	Read address	1555 (hex)	Valid READ
3.	Read address	0AAA (hex)	Valid READ
4.	Read address	1FFF (hex)	Valid READ
5.	Read address	10F0 (hex)	Valid READ
6.	Read address	0F0F (hex)	Initiate *STORE* Cycle

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\overline{G}$ be LOW for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

HARDWARE PROTECT

The STK13C68 offers hardware protection against inadvertent *STORE* cycles through V_{CC} Sense. A *STORE* cycle will not be initiated, and one in progress will discontinue, if V_{CC} goes below 4.1V. 4.1V is a typical, characterized value.

NONVOLATILE RECALL

A *RECALL* cycle of the EEPROM data into the SRAM is initiated with a sequence of READ operations in a manner similar to the *STORE* initiation. To initiate the *RECALL* cycle the following sequence of READ operations must be performed:

1.	Read address	0000 (hex)	Valid READ
2.	Read address	1555 (hex)	Valid READ
3.	Read address	0AAA (hex)	Valid READ
4.	Read address	1FFF (hex)	Valid READ
5.	Read address	10F0 (hex)	Valid READ
6.	Read address	0F0E (hex)	Initiate *RECALL* Cycle

Internally, *RECALL* is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. The *RECALL* operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

On power-up, once V_{CC} exceeds the V_{CC} sense voltage of 4.1V, a *RECALL* cycle is automatically initiated. The voltage on the V_{CC} pin must not drop below 4.1V once it has risen above it in order for the *RECALL* to operate properly. Due to this automatic *RECALL*, SRAM operation cannot commence until t_{RECALL} after V_{CC} exceeds 4.1V. 4.1V is a typical, characterized value.

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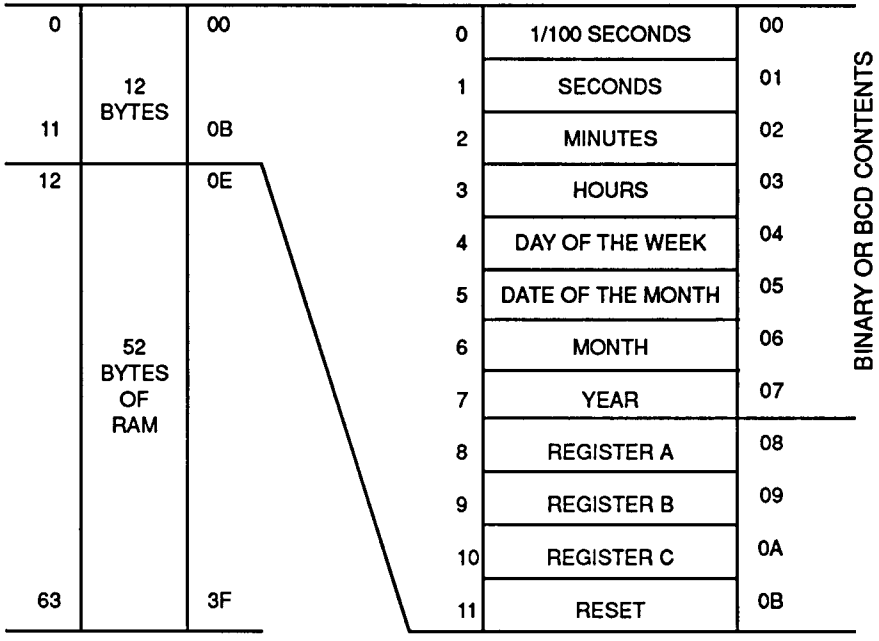
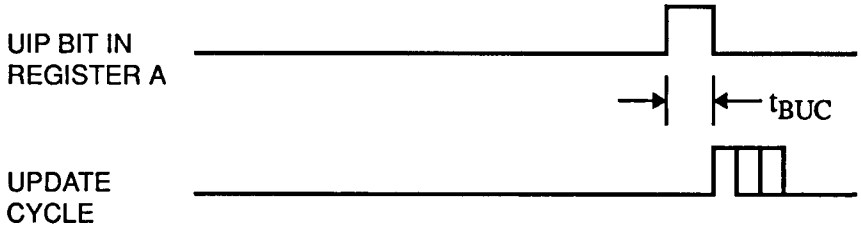


Note: Only address lines A_5-A_0 are used. Addresses A_{12}-A_6 are ignored.

TIME AND CALENDAR DATA MODES

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	1/100 Seconds	0-99	00-63	00-99
1	Seconds	0-59	00-3B	00-59
2	Minutes	0-59	00-3B	00-59
3	Hours - 12-hr Mode	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	Hours - 24-hr Mode	0-23	00-17	00-23
4	Day of the Week Sunday=1	1-7	01-07	01-07
5	Date of the Month	1-31	01-1F	01-31
6	Month	1-12	01-0C	01-12
7	Year	0-99	00-63	00-99

UPDATE CYCLE RELATIONSHIP



t_{BUC} = Delay Time Before Update Cycle (250µs)

REGISTERS

The STK1390 has 4 control registers which are accessible at all times, even during the update cycle.

REGISTER A

MSB							LSB
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
UIP	NVV	TEST	0	0	0	0	0

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UIP - The Update In Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is a '1', the update transfer will soon occur. When UIP is a '0', the update transfer will not occur for at least 250us. The time and calendar information is fully available for access when the UIP bit is '0'. The UIP bit is read only and is not affected by RESET. Writing the SET bit in Register B to a '1' inhibits any update transfer and clears the UIP status bit.

NVV - The Non-Volatile Valid (NVV) bit is a status flag that indicates whether both the 8Kx8 SRAM and the 52 general purpose RAM contents are the same as their shadowed nvSRAM contents. A '0' indicates that the SRAM and nvSRAM contents are not the same, and a '1' indicates that they are identical. The NVV bit is read only and is not affected by RESET.

TEST - A '1' written into this TEST bit puts the device into test mode. This allows setting of the oscillator frequency as well as rapid testing of the device. For normal operation the TEST bit must be a '0'.

BIT4 TO BIT0 - These are unused bits are always read '0' and cannot be written.

REGISTER B

MSB							LSB
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
SET	0	0	0	0	DM	24/12	DSE

SET - When the SET bit is a '0', the update cycle functions normally by advancing the counts once per 1/100 second. When the SET bit is written to a '1', the 1/100 seconds byte is cleared to 0 and any update cycle is inhibited and the program can initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in

a similar manner. SET is a read/write bit that is not modified by RESET or internal functions of the device.

BIT6 TO BIT3 - These are unused bits are always read '0' and cannot be written.

DM - The Data Mode (DM) bit indicates whether time and calendar information is in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by RESET or internal functions of the device. A '1' in DM signifies binary data, while a '0' in DM specifies Binary Coded Decimal (BCD) data.

24/12 - The 24/12 control bit establishes the format of the hours bytes. A '1' indicates the 24-hour mode and a '0' indicates the 12-hour mode. This is a read/write bit and is not affected by RESET or internal functions.

DSE - The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is '1'. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a '0'. This bit is not affected by RESET or internal functions.

REGISTER C

MSB							LSB
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
VRT	0	0	0	0	0	0	0

VRT - The Valid RAM and Time (VRT) bit indicates the condition of the contents of the time/calendar and control/status registers (locations 00H to 0BH). A '0' appears when the power supply to the real time clock has dropped to less than 2V or when the oscillator has stopped, and that both the contents of the time/calendar and control/status registers are questionable. The processor program can set the VRT bit when the time and calendar are initialized to indicate that the time/calendar and registers are valid. The VRT is a read only bit which is not modified by RESET. The VRT bit can only be set by reading Register C.

BIT6 TO BIT0 - These are unused bits are always read '0' and cannot be written.

RESET REGISTER

Writing any data to location 0BH causes the 1/100 seconds through minutes bytes and the year byte to be reset to 0. The day of week, date of month and month bytes are set to 1. The hour byte is cleared to 0 if the 24/12 bit is a '1', and is set to 1 if the 24/12 bit is a '0'.

ADDRESS MAP

The address map is shown in Figure 1. The memory map consists of 52 bytes of user RAM, 8 bytes of RAM that contain the RTC time and calendar data, and 4 control and status bytes. All 64 bytes can be directly written or read except the following:

1.The 1/100 seconds byte is read only.

2.Bit 7 and 6 of register A is read only.

3.Register C is read only.

4.The reset register is write only.

The contents of the 3 registers (abound C) and the reset register are described in the REGISTERS section.

TIME AND CALENDAR LOCATIONS

The time and calendar information is obtained by reading the appropriate locations. The time and calendar are set or initialized by writing the appropriate locations. The contents of the 8 time and calendar bytes can be either binary or binary-coded decimal (BCD) format.

Before initializing the internal time and calendar registers, the SET bit in Register B should be set to a '1' to prevent time/calendar updates from occurring while access is being attempted. In addition to writing the 7 time and calendar registers in the selected format (binary or BCD), the data mode (DM) bit of Register B must be set to the appropriate logic level. All the time and calendar bytes must used the same data mode. The SET bit may now be cleared to allow the real time clock to update the time and calendar bytes. Once initialized, the real time clock makes all updates in the selected data mode. The data mode cannot be changed without reinitializing the 7 data bytes.

Table 1 shows the binary and BCD formats of the 8 time and calendar locations. The 24/12 bit in Register B establishes whether the hours location represent 1-to-12 or 0-to-24. The 24/12 bit cannot be changed without reinitializing the hours location. When the 12-hour format is selected, the high-order bit of the hours byte represents PM when it is a '1'.

The time and calendar bytes are not always accessible by the processor program. Once-per-1/100 second the 8 bytes are switched to the update logic to be advanced by one 1/100 second. If any of the 8 bytes are read at this time, the data outputs are undefined.

CMOS STATIC RAM

The 52 general purpose RAM bytes are not dedicated to any special function. They can be used by the processor program, and are fully available during the update cycle. These are nvSRAM bytes that are located together with the 8Kx8 nvSRAM.

UPDATE CYCLE

The STK1390 executes an update cycle once per 1/100 second, assuming that the SET bit in Register B is clear. The SET bit in the '1' state permits the program to initialize the time and calendar bytes by stopping an existing update and preventing a new one from occurring.

The primary function of the update cycle is to increment the 1/100 seconds byte, check for overflow, increment the seconds byte when appropriate and so forth through to the year byte.

Since this update cycle occurs asynchronously to the reading of the time and calendar bytes, it is possible to read these bytes while they are being incremented. This may result in an incorrect reading. Thus to ensure a correct reading of the time and calendar bytes, the access method of using the update-in-progress (UIP) bit in Register A to determine if the update cycle is in progress is recommended.The UIP bit will pulse once per 1/100 second. After the UIP goes high, the update transfer occurs 250us later. If a low is read on the UIP bit, the user has at least 250us before the time/calendar data will be changed. Therefore, the user should avoid subroutines that would cause the time needed to read valid time/calendar data to exceed 250us.