Synchronous BCD Decade Up/Down Counter
LS192

Synchronous 4-Bit Binary Up/Down Counter
LS193

FEATURES
- Separate clock inputs for count-up, count-down
- Asynchronous parallel load and clear
- Cascadable

DESCRIPTION

These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The LS192 is a BCD counter and the LS193 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.
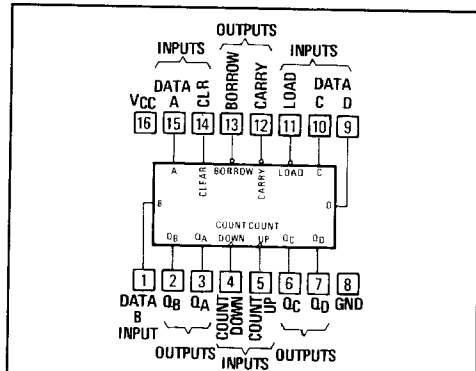
A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.
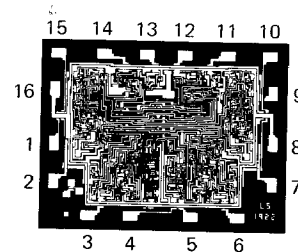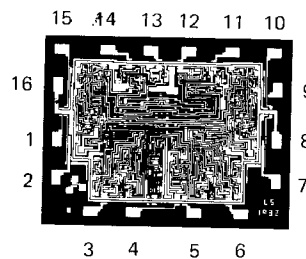
PIN-OUT DIAGRAM

Low input to load sets $Q_A = A$, $Q_B = B$,
$Q_C = C$, and $Q_D = D$

LS192

LS193

Die Size .100 x .077 (both types)

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Count frequency, f_{count}	0		25	0		25	MHz
Width of any input pulse, t_w	20			20			ns
Data setup time, t_{setup} (see Figure 1)	20			20			ns
Data hold time, t_{hold}	0			0			ns
Operating free-air temperature range, T_A	−55		125	0		70	°C

LOGIC DIAGRAM

LS192

RAYTHEON

LOGIC DIAGRAM
LS193

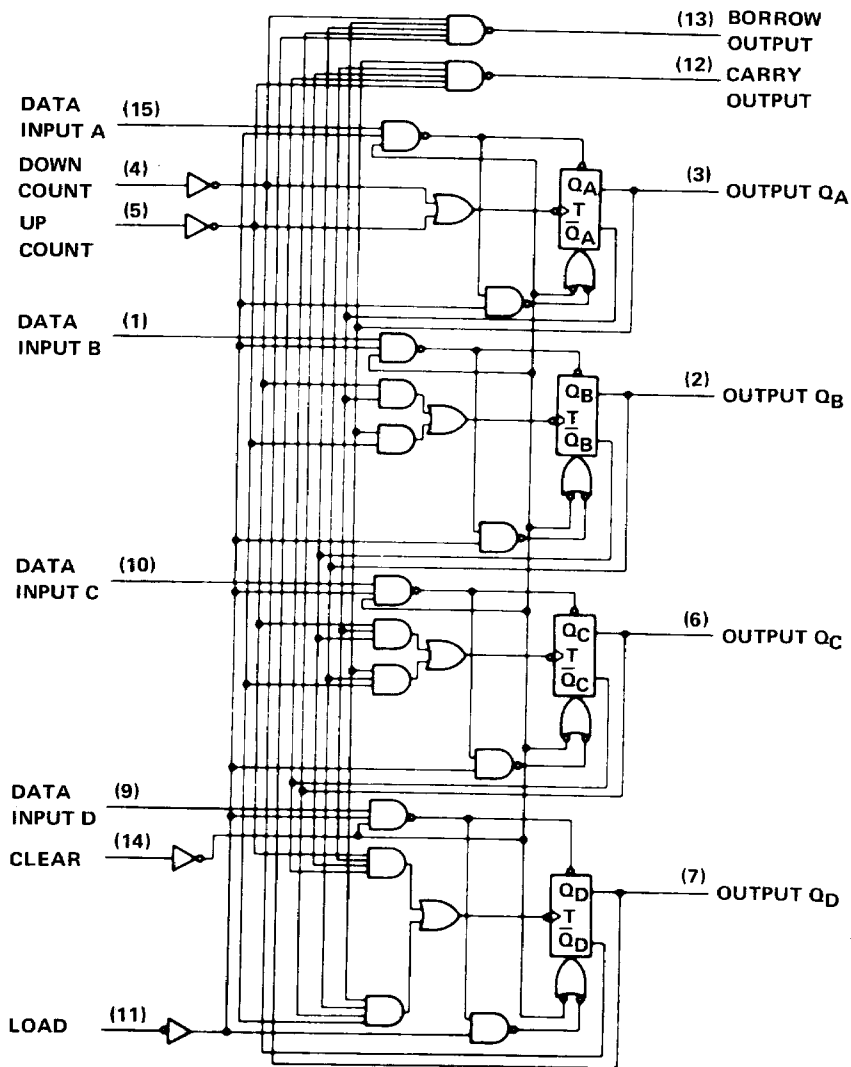**LS192**   **Synchronous BCD Decade Up/Down Counter**

LS193   **Synchronous 4-Bit Binary Up/Down Counter**

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*	9LS/54LS Min	9LS/54LS Typ**	9LS/54LS Max	9LS/74LS Min	9LS/74LS Typ**	9LS/74LS Max	Unit
V_{IH}		2			2			V
V_{IL}				0.7			0.8	V
V_I	V_{CC}=MIN, I_I=−18			−1.5			−1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=−400µA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max I_{OL}=4mA		0.25	0.40		0.25	0.40	V
	I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7V			0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V			20			20	µA
I_{IL}	V_{CC}=MAX, V_I=0.4V			−0.4			−0.4	mA
I_{OS}†	V_{CC}=MAX	−15		−100	−15		−100	mA
I_{CC}††	V_{CC}=MAX		19	34		19	34	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
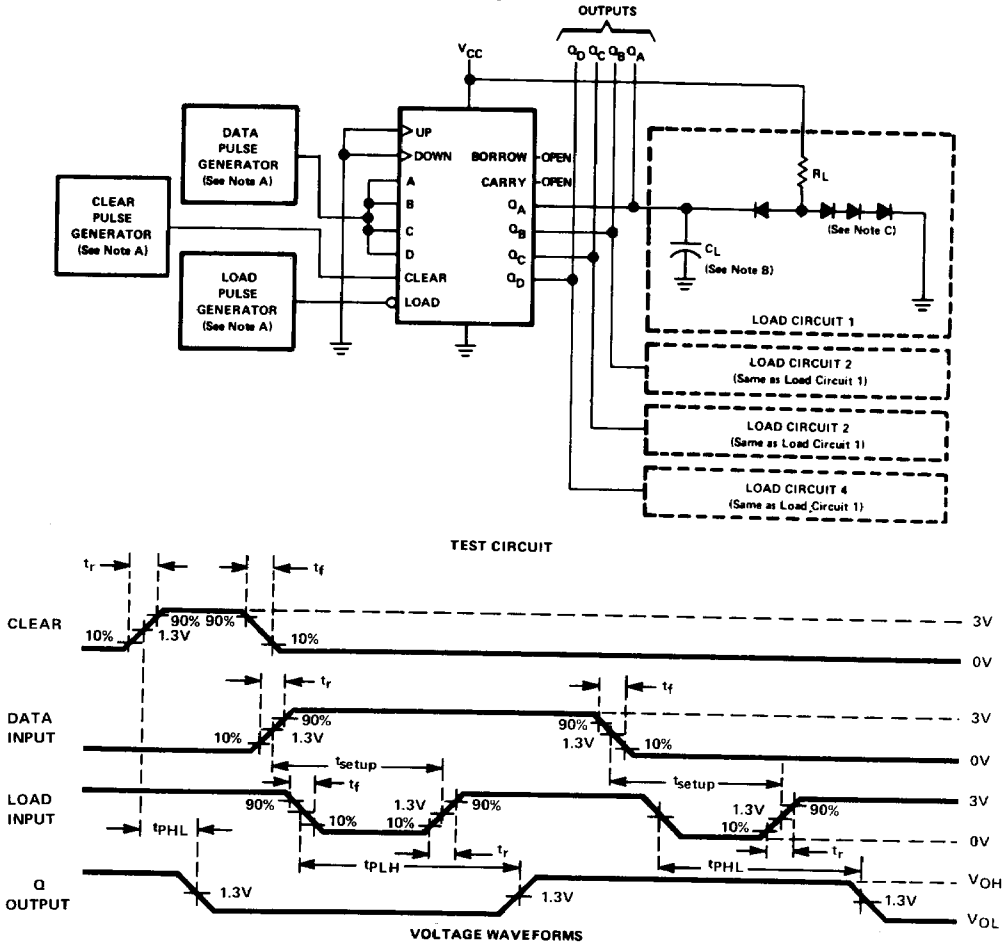†Not more than one output should be shorted at a time.
††I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (input)	To (output)	−55°C Min	−55°C Typ	−55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Typ	+125°C Max	Unit
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. 1 and 2)												
f_{max}						25	32					MHz
t_{PLH}	Count-up	Carry		19	29		17	26		19	29	ns
t_{PHL}				18	28		16	24		18	28	
t_{PLH}	Count-down	Borrow		18	28		16	24		18	28	ns
t_{PHL}				18	28		16	24		18	28	
t_{PLH}	Either Count	Q		27	42		25	38		27	42	ns
t_{PHL}				33	51		31	47		33	51	
t_{PLH}	Load	Q		29	44		27	40		29	44	ns
t_{PHL}				31	44		29	40		31	44	
t_{PHL}	Clear	Q		24	39		22	35		24	39	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. 1 and 2)												
												MHz
t_{PLH}	Count-up	Carry		23	34		21	31		23	34	ns
t_{PHL}				22	32		20	30		22	32	
t_{PLH}	Count-down	Borrow		22	32		20	30		22	32	ns
t_{PHL}				22	32		20	30		22	32	
t_{PLH}	Either Count	Q		31	47		29	43		31	47	ns
t_{PHL}				37	56		34	51		37	56	
t_{PLH}	Load	Q		33	49		31	44		33	49	ns
t_{PHL}				35	49		33	45		35	49	
t_{PHL}	Clear	Q		28	44		26	40		28	44	ns

Note: AC specification shown under −55°C and +125°C are for 9LS devices only.
All 50pF specifications are for 9LS only.

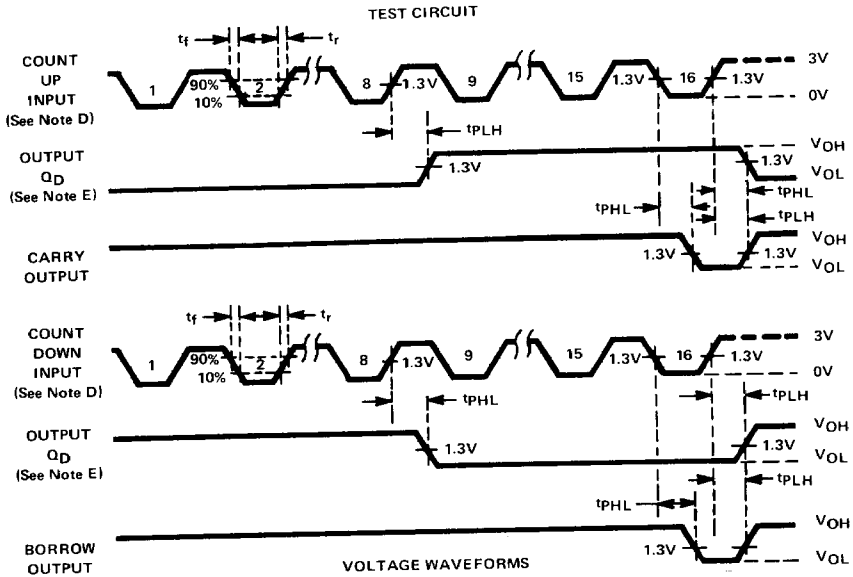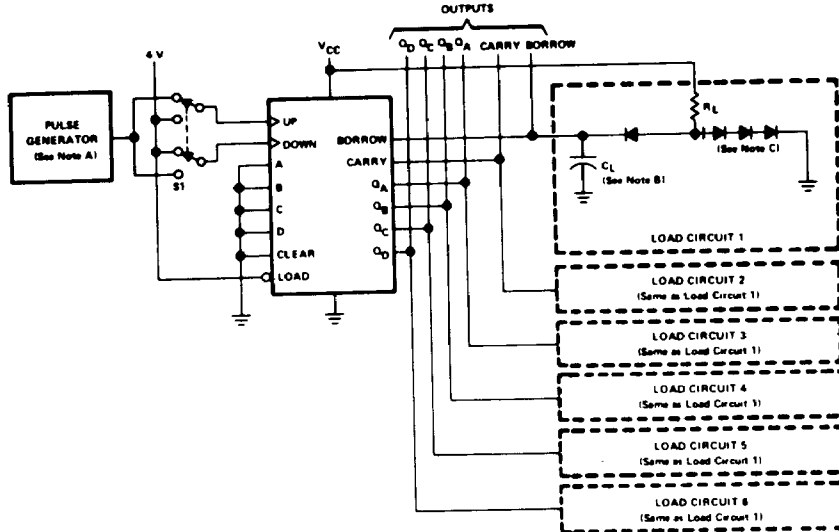## PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES:
A. The pulse generators have the following characteristics: Z_{out} = 50Ω and for the data pulse generator PRR < 500KHz, duty cycle = 50%; for the load pulse generator PRR is two times data PRR, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. Diodes are 1N3064.
D. t_r and t_f ⩽ 7 ns.

FIGURE 1 — CLEAR, SETUP, AND LOAD TIMES

PARAMETER MEASUREMENT INFORMATION (Continued)

TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES:
A. The pulse generator has the following characteristics: PRR ≤ 1MHz, Z_{out} = 50Ω, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. Diodes are 1N3064.
D. Count-up and count-down pulse shown is for the LS193 binary counter. Count cycle for LS192 decade counter is 1 through 10.
E. Waveforms for outputs Q_A, Q_B, and Q_C are omitted to simplify the drawing.
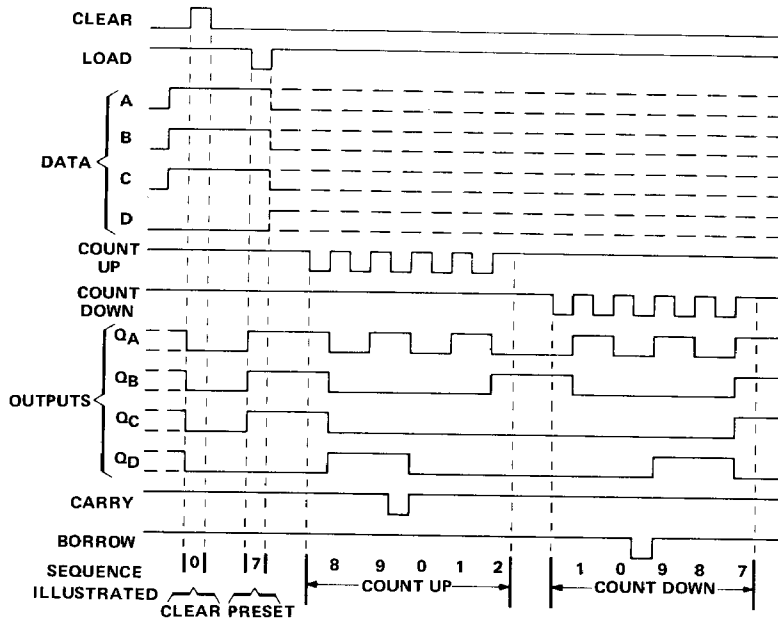F. t_r and t_f ≤ 7ns.

FIGURE 2—PROPAGATION DELAY TIMES

RAYTHEON

TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES
LS192

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
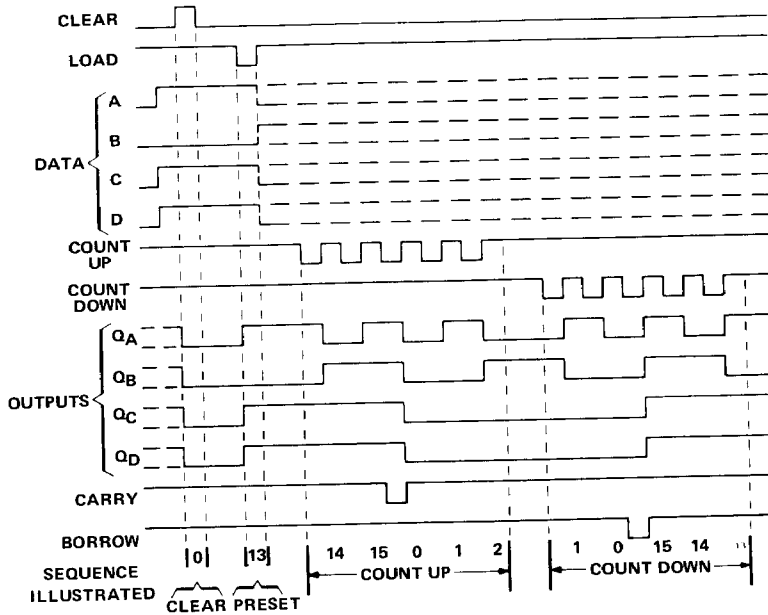4. Count down to one, zero, borrow, nine, eight, and seven.

NOTES:

A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting
down, count-up input must be high.

TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES
LS193

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

NOTES:
A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.