

# 2N7000/BS170L

# N-Channel Enhancement-Mode MOS Transistor

### PRODUCT DESCRIPTION

The ALPHA Semiconductor 2N7000 utilizes ALPHA's vertical DMOS technology. This device is well suited for switching applications where B<sub>V</sub> of 60V and low on resistance (under 5 ohms) are required. The 2N7000 is housed in a plastic TO-92 package.

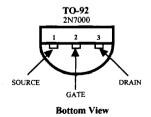
### ORDERING INFORMATION

Part Number	Temperature Range	Package Type
2N7000N	-55°C to +150°C	Plastic TO-92
BS170LN	-55°C to +150°C	Plastic TO-92
2N7000X	-55°C to +150°C	Sorted Chips in Carriers

### **PRODUCT SUMMARY**

Part Number	V <sub>(BR)DSS</sub> (V)	$r_{DS(ON)} \ (\Omega)$	I <sub>D</sub> (A)
2N7000	60	5	0.2
BS170	60	5	0.5

#### **Pin Connections**



DRAIN GATE SOURCE

TO-92

## ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = +25°C, unless otherwise specified.)

Parameter	Conditions	Limits	Units	
Drain-Source Voltage		60	V	
Gate-Source Voltage	-	±40	V	
Continuous Drain Current	$T_A = 25$ °C $T_A = 100$ °C	0.2 0.13		
Pulsed Drain Current <sup>1</sup>		0.5	A	
Power Dissipation <sup>1</sup>	$T_{A} = 25^{\circ}C$ $T_{A} = 100^{\circ}C$	0.4 0.16	w	
Operation Junction Temperature Range		-55 to 150	°C	
Storage Temperature Range		-55 to 150	°C	
Lead Temperature		300	°C	

Thermal Resistance	Limits	Units		
Junction-to-Ambient	312.5	K/W		

NOTE: 1. Pulse width limited by maximum junction temperature.

## SPECIFICATIONS1

Parameter	Conditions	Min	Тур.	Max	Units	
STATIC						
Drain-Source Breakdown Voltage	$l_{\rm p} = 10 \mu A, V_{\rm OS} = 0 V$	60	70		V	
Gate-Threshold Voltage	$V_{DS} = V_{GS}, l_D = lmA$	0.8	1.9	3	V	
Gate-Body Leakage	$V_{QS} = \pm 15V, V_{DS} = 0V$			±10	nA	
Zero Gate Voltage Drain Current	$V_{DS} = 48V, V_{GS} = 0V$ $T_{C} = 125^{\circ}C$			1 1000	μА	
On-State Drain Current <sup>3</sup>	$V_{DS} = 48V, V_{GS} = 0V$	75	210		mA	
Drain-Source On-Resistance <sup>3</sup>	$^{4}V_{GS} = 4.5V, I_{D} = 75\text{mA}$ $V_{GS} = 10V, I_{D} = 0.5\text{A}$ $T_{C} = 125^{\circ}\text{C}$		4.8 2.5 4.4	5.3 5 9	Ω	
Drain-Source On-Voltage <sup>3</sup>	$^{4}V_{GS} = 4.5V, l_{D} = 75\text{mA}$ $V_{GS} = 10V, l_{D} = 0.5A$ $T_{C} = 125^{\circ}C$		0.36 1.25 2.2	0.4 2.5 4.5	V	
Forward Transconductance <sup>3</sup>	$V_{DS} = 10V, l_D = 0.2A$	100	170		mS	
Common Source Ouput Conductance <sup>3,4</sup>	$V_{DS} = 5V, l_D = 50mA$		500		μS	
	DYNAMIC				·	
Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V, f = 1MHz$		16	60	pF	
Output Capacitance4	$V_{DS} = 25V, V_{GS} = 0V, f = 1MHz$		11	25	pF	
Reverse Transfer Capacitance	$V_{DS} = 25V, V_{GS} = 0V, f = 1MHz$		2	5	pF	
	SWITCHING					
Turn-On Time	$V_{DD} = 15V$ , $R_{L} = 25\Omega$ , $I_{D} = 0.5A$ $V_{GEN} = 10V$ , $R_{G} = 25\Omega$ (Switching time is essentially independent of operating temperature)		7	10	nS	
Turn-Off Time	$V_{DD} = 15V$ , $R_{L} = 25\Omega$ , $I_{D} = 0.5A$ $V_{GEN} = 10V$ , $R_{G} = 25\Omega$ (Switching time is essentially independent of operating temperature)		7	10	nS	

- T<sub>A</sub> = 25°C unless otherwise specified
   For design aid only, not subject to production testing.
- 3. Pulse test; PW =  $\leq 300 \mu$ S, duty cycle  $\leq 3\%$ .
- 4. This parameter not registered with JEDEC.