mosaic

Mosaic Semiconductor Inc.

4Meg x 1 Monolithic DRAM

MDM14001-80/10/12

Issue 1.2 : December 1992

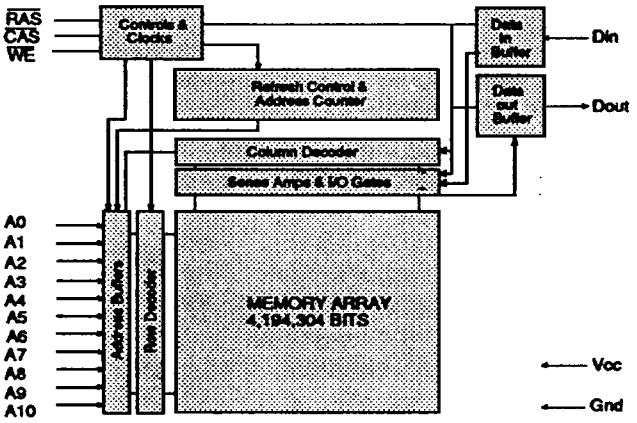
ADVANCE PRODUCT INFORMATION

4,194,304 x 1 CMOS High Speed Dynamic RAM

Features

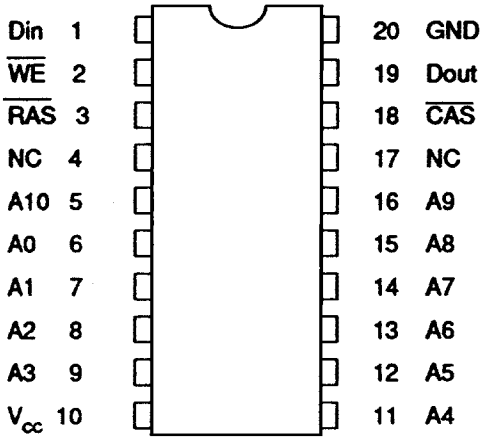
- Row Access Time of 80,100,120 ns
- Available in 20 Pin DIP, 20 & 24 Pin VIL
- 5 Volt Supply ± 10%
- 1024 Refresh Cycles (16 ms)
- $\overline{CAS}$ before $\overline{RAS}$ Refresh
- $\overline{RAS}$ only Refresh
- Hidden Refresh
- Nibble Mode Capability
- Test Function Available
- Directly TTL Compatible
- May Be Processed to MIL-STD-883 Method 5004, non-compliant.

Block Diagram



Pin Definition

Package Type: 'K','V','G', 'W','J'



Package Type: 'VX' - Page 10.

Pin Functions

A0-A10	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
Din	Data Input
Dout	Data Output
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
GND	Ground
NC	No Connect

Package Details Dimensions in inches(mm). Tolerance on all dimensions ±.010(.254).

Pin Count	Description	Package Type	Material	Pinout
20	400 mil Dual-in-Line(DIP)	K	Ceramic	JEDEC
20	100 mil Vertical-in-Line(VIL)	V	Ceramic	JEDEC
24	100 mil Vertical-in-Line(VIL)	VX	Ceramic	ASIC
20	Leadless Chip Carrier(LCC)	W	Ceramic	JEDEC
20	Ceramic Flatpack	G	Ceramic	JEDEC
20	Leaded CSOJ	J	Ceramic	JEDEC

Package Dimensions and details on page 9,10.

VIL is a trademark of Mosaic Semiconductor Inc., Patent No. D316251

Absolute Maximum Ratings

Voltage on any pin relative to V_{SS}	V_t	-1 V to +7	V
Power Dissipation	P_t	1.0	W
Storage Temperature	T_{stg}	-65 to +150	°C
Short circuit output current	I_{osc}	50	mA

Recommended Operating Conditions

		min	typ	max	
Supply Voltage	V_{CC}	4.50	5.0	5.50	V
Input High Voltage	V_{IH}	2.4	-	6.5	V
Input Low Voltage	V_{IH}	-1.0	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (14001I)
	T_{AM}	-55	-	125	°C (14001M,MB,MC)

Capacitance (V_{cc}=5V±10%,T_a=25°C)

Parameter		*Symbol*	*typ*	*max*	*Unit*	*Notes*
Input Capacitance:	Address	C_{I1}	-	5	pF	1
Input Capacitance:	Clocks	C_{I2}	-	7	pF	1
I/O Capacitance:	Data-in/out	$C_{I/O}$	-	7	pF	1,2

Notes: 1. Capacitance calculated, not measured.
2. $\overline{CAS}$=V_{IH} to disable Dout.

DC Electrical Characteristics

Parameter	*Symbol*	*Test Condition*	*-80* min	*-80* max	*-10* min	*-10* max	*-12* min	*-12* max	*Unit*	*Notes*
Operating Current	I_{CC1}	$\overline{RAS}$,$\overline{CAS}$ Cycling: t_{RC}=min.	-	90	-	80	-	70	mA	1,2
Refresh Current	I_{CC3}	$\overline{RAS}$ only Refresh, t_{RC}=min.	-	90	-	80	-	70	mA	
Refresh Current	I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh tRC = min	-	90	-	80	-	70	mA	
Page Mode Supply Current	I_{CC7}	$\overline{RAS}$=V_{IL},$\overline{CAS}$ Cycling, t_{PC}=min.	-	90	-	80	-	70	mA	
Standby Current	I_{CC2}	$\overline{RAS}$,$\overline{CAS}$=V_{IH},Dout Disabled	-	2	-	2	-	2	mA	2
	I_{CC4}	$\overline{RAS}$,$\overline{CAS}$,≥ Vcc-0.2V, Dout Disabled, CMOS Levels	-	1	-	1	-	1	mA	2
Input Leakage	I_{LI}	V_{IN}=0 to +7V	-10	10	-10	10	-10	10	µA	2
Output Leakage	I_{LO}	V_{OUT}=0 to +7V, Dout is disabled.	-10	10	-10	10	-10	10	µA	2
Output Levels	V_{OH}	I_{OUT}=-5mA	2.4	-	2.4	-	2.4	-	V	2
	V_{OL}	I_{OUT}=4.2mA	-	0.4	-	0.4	-	0.4	V	2

Notes 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max. is specified at the output open condition.
2. These parameters are 100% tested.

AC Test Conditions

* Input pulse levels: 0.8 to 2.4V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: 2 TTL gates + 100pF

Electrical Characteristics & Recommended AC Operating Conditions (1,12)

Parameter	Symbol	-80 min	-80 max	-10 min	-10 max	-12 min	-12 max	Unit	Note
Access Time from $\overline{RAS}$	t_{RAC}	-	80	-	100	-	120	ns	2,3
Access Time from $\overline{CAS}$	t_{CAC}	-	25	-	25	-	30	ns	3,4
Output Buffer Turn-off Delay	t_{OFF}	0	20	0	25	0	30	ns	6
Transition Time (Rise & Fall)	t_T	3	50	3	50	3	50	ns	7
Random Read or Write Cycle Time	t_{RC}	150	-	180	-	210	-	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	-	70	-	80	-	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	60	25	75	25	90	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	20	-	25	-	30	-	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	-	100	-	120	-	ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	40	20	55	25	65	ns	9
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	-	45	-	55	-	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	-	10	-	10	-	ns	13
Row Address Setup Time	t_{ASR}	0	-	0	-	0	-	ns	
Row Address Hold Time	t_{RAH}	12	-	15	-	20	-	ns	
Column Address Setup Time	t_{ASC}	0	-	0	-	0	-	ns	8
Column Address Hold Time	t_{CAH}	15	-	20	-	25	-	ns	
Access Time From Address	t_{AA}	-	40	-	45	-	55	ns	
Write Command Setup Time	t_{WCS}	0	-	0		0	-	ns	3,4,10
Write Command Hold Time	t_{WCH}	15	-	20	-	25	-	ns	
Write Command Pulse Width	t_{WP}	15	-	20	-	25	-	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	-	25	-	30	-	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25	-	25	-	30	-	ns	
Data in Setup Time	t_{DS}	0	-	0	-	0	-	ns	11
Data in Hold Time	t_{DH}	15	-	20	-	25	-	ns	11
Read Command Setup Time	t_{RCS}	0	-	0	-	0	-	ns	13
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0	-	0	-	0	-	ns	13
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	0	-	0	-	0	-	ns	13
Refresh Period (1024 Cycles)	t_{REF}	-	16	-	16	-	16	ms	
Read-Modify-Write Cycle Time	t_{RWC}	180	-	210	-	245	-	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	-	100	-	120	-	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	25	-	25	-	30	-	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	40	-	45	-	50	-	ns	10
$\overline{CAS}$ Setup Time	t_{CSR}	10	-	10	-	10	-	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	20	-	20	-	25	-	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	-	10	-	10	-	n	
Test Mode $\overline{WE}$ Setup Time	t_{WS}	0	-	0	-	0	-	ns	13
Test Mode $\overline{WE}$ Hold Time	t_{WH}	10	-	10	-	10	-	ns	13
$\overline{CAS}$ Precharge in Counter Test Cycle	t_{CPT}	40	-	50	-	60	-	ns	13
Nibble Mode Access Time	t_{NAC}	-	20	-	20	-	25	ns	
Nibble Mode Cycle Time	t_{NC}	45	-	45	-	45	-	ns	
Nibble Mode $\overline{CAS}$ Precharge Time	t_{NCP}	10	-	10	-	10	-	ns	13
Nibble Mode $\overline{CAS}$ Pulse Width	t_{NAS}	25	-	25	-	25	-	ns	
Nibble Mode $\overline{RAS}$ Hold Time	t_{NRSH}	25	-	25	-	25	-	ns	13

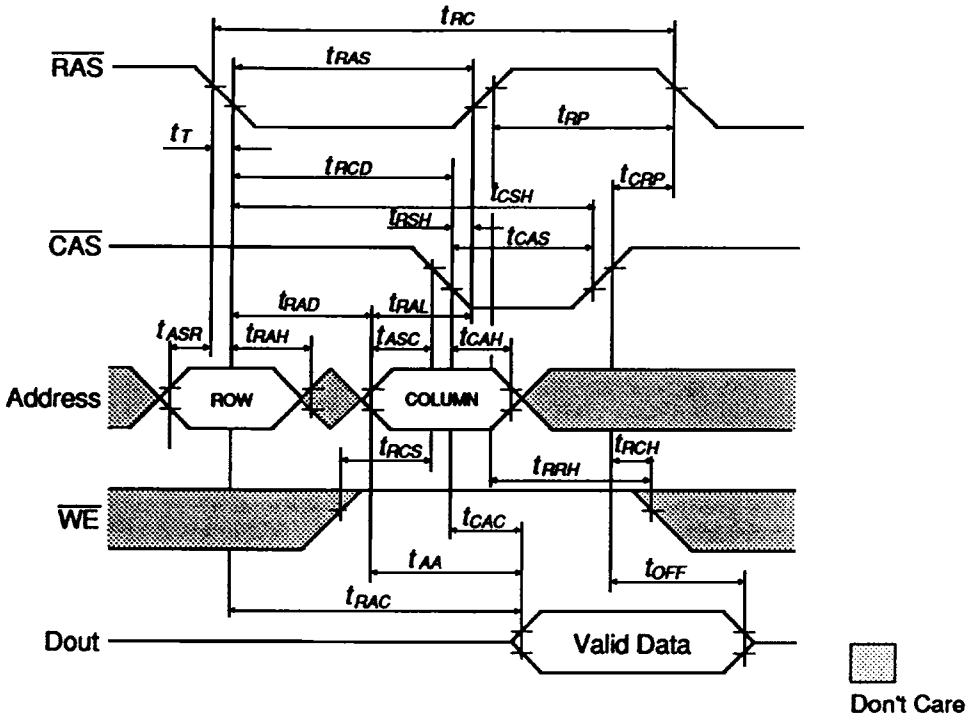
Electrical Characteristics & Recommended AC Operating Conditions Continued (1,12)

		-80		-10		-12			
Parameter	*Symbol*	*min*	*min*	*max*	*max*	*min*	*max*	*Unit*	*Note*
Nibble Mode Read-Modify-Write Cycle Time	t_{NRWC}	75	-	75	-	75	-	ns	
Nibble Mode Write Command to $\overline{CAS}$ Lead Time	t_{NCWL}	25	-	25	-	25	-	ns	
Nibble Mode $\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{NCWD}	25	-	25	-	25	-	ns	

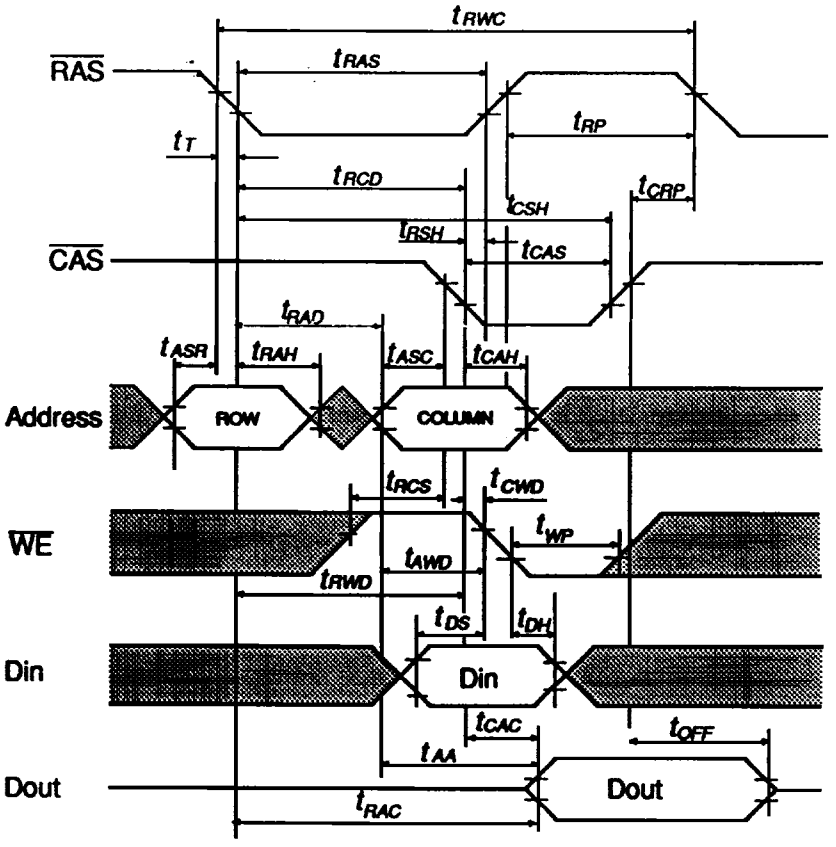
Notes:

1. AC measurements assume t_T=5ns.
2. Assumes that t_{RCD} is less than or equal to t_{RCD} (max.).If t_{RCD} is greater than the max. recommended value shown in this table,t_{RAC} exceeds the value shown.
3. Measured with a load current equivalent to two TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max.) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RCD} (max.) is specified as a reference point only, if t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RAD} (max.) is specified as a reference point only, if t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameter.They are included in the Data Sheet as Electrical Characteristics only.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed or read-modify-write cycle.
12. An initial pause of 100µs is required after power-up. Then execute at least 8 initialization ($\overline{RAS}$) cycles.
13. This parameter is not tested.

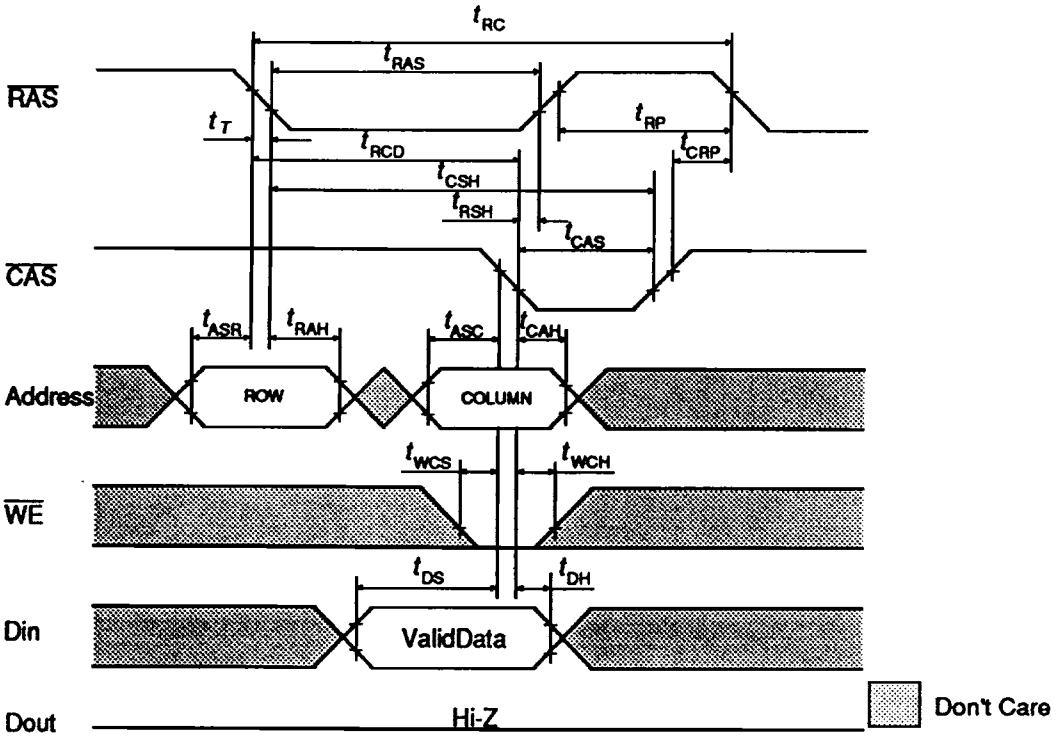
Read Cycle Timing Diagram



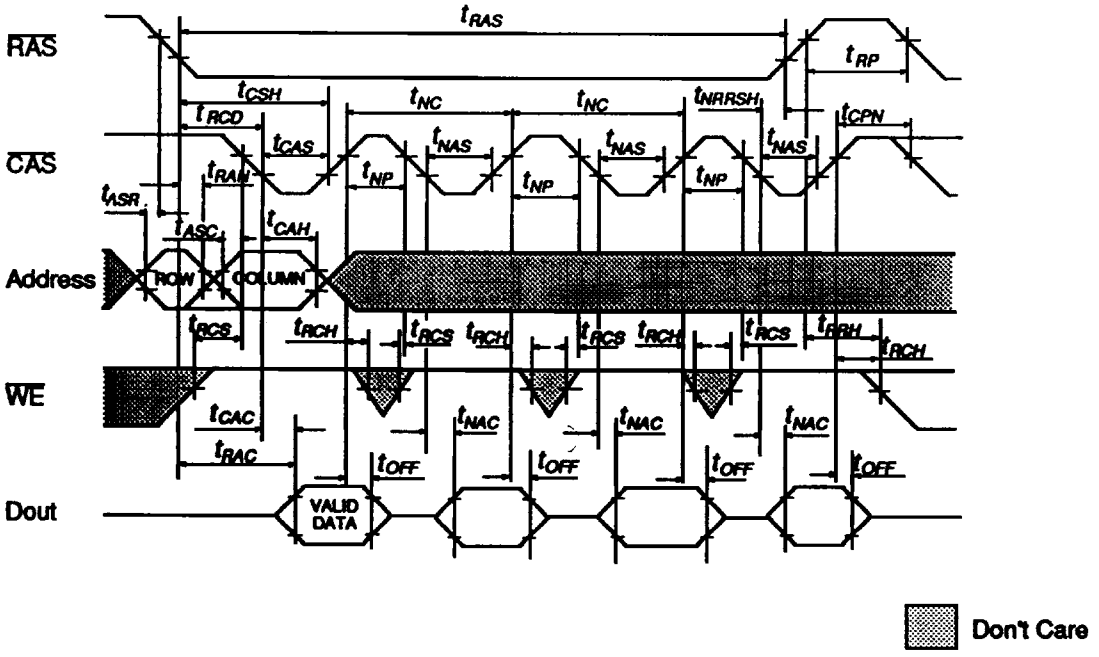
Read-Modify-Write Cycle Timing Diagram



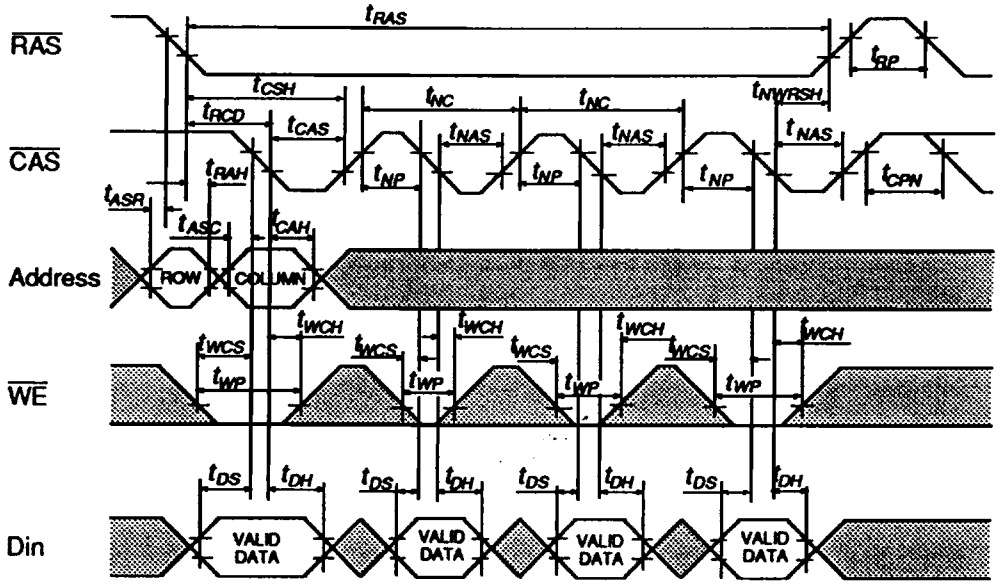
Early Write Cycle



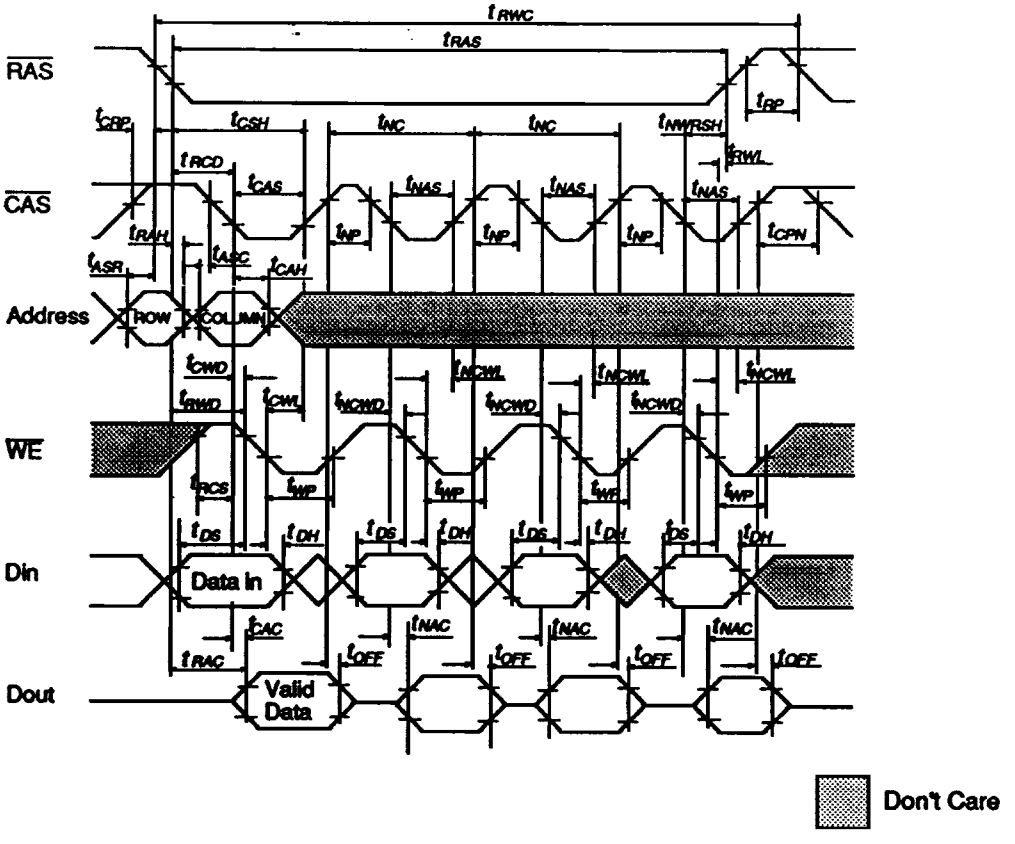
Nibble Mode Read Cycle



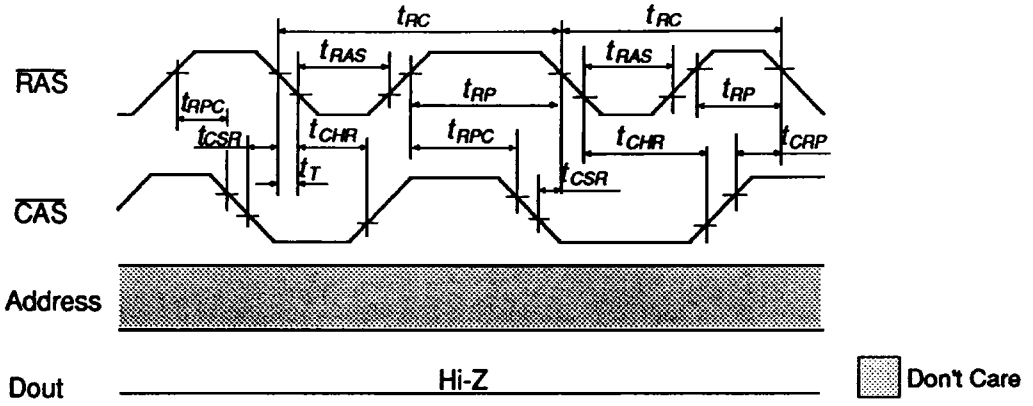
Nibble Mode Early Write Cycle



Nibble Mode Read-Modify-Write Cycle

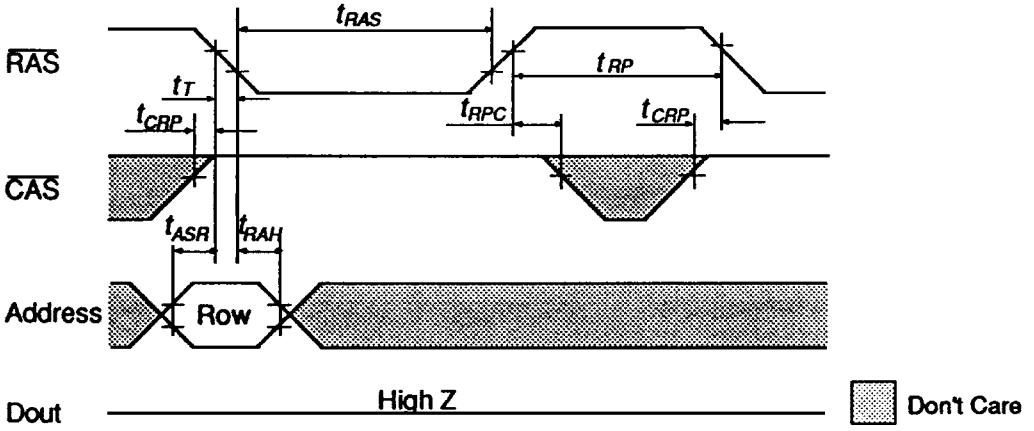


$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

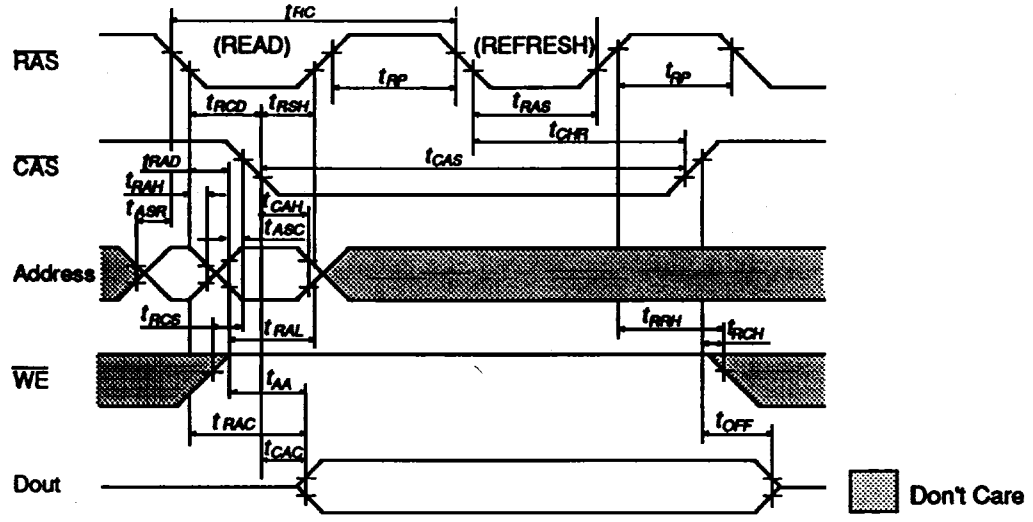


Note: $\overline{WE}$ must equal V_{IH} during the $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

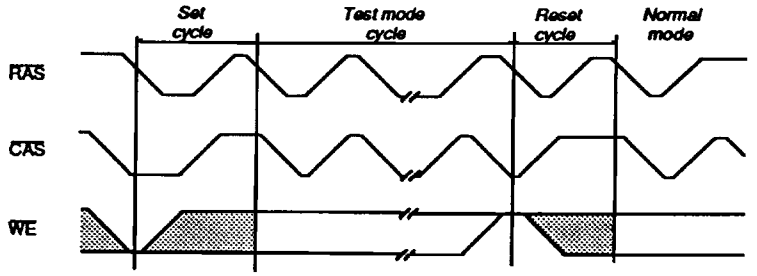
$\overline{RAS}$ Only Refresh Cycle



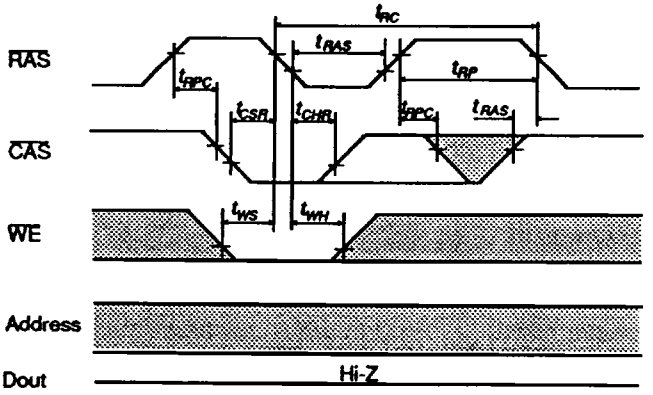
Hidden Refresh Cycle



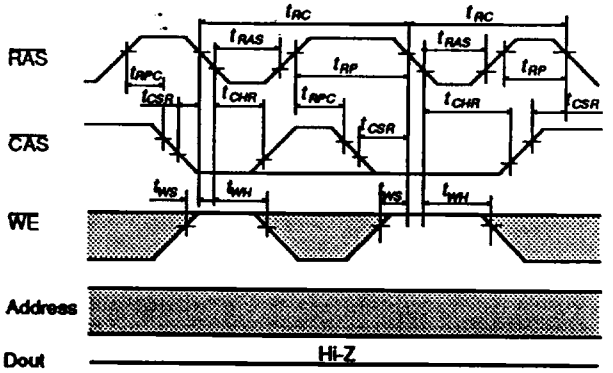
Test Mode Cycle



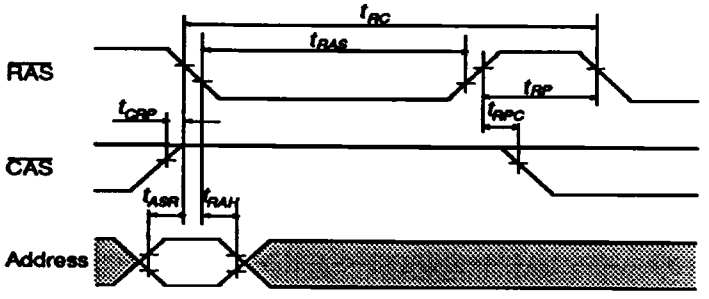
Test Mode Set Cycle



Test Mode Reset Cycle: $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

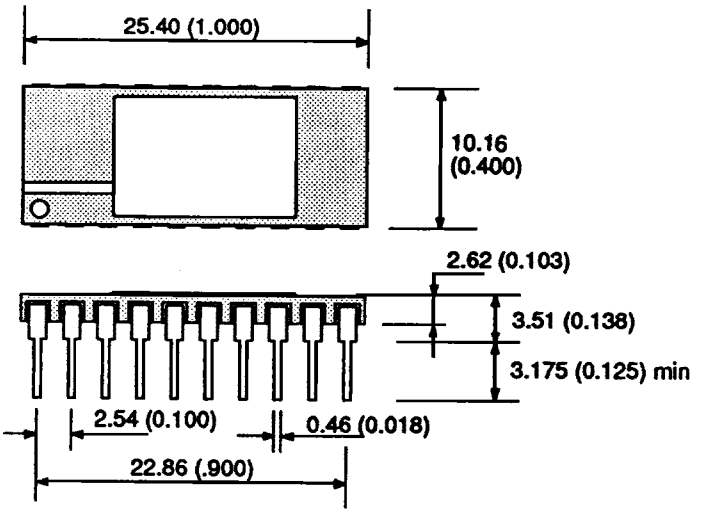


$\overline{RAS}$ Only Refresh Cycle

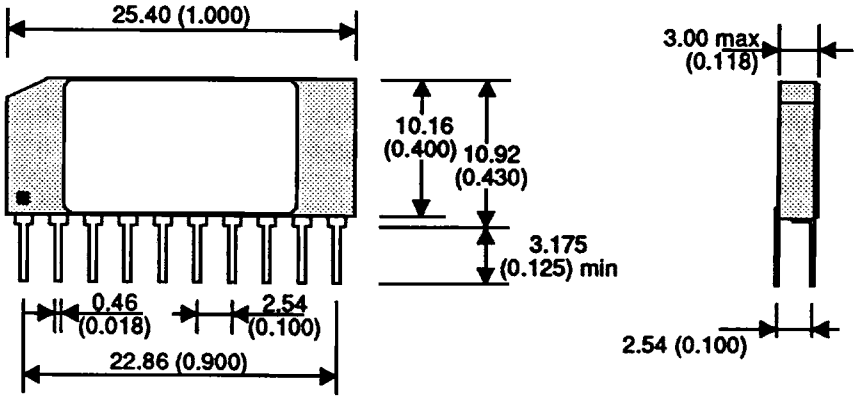


Package Details Dimensions in mm (inches).Tolerance on all dimensions ±0.254(0.010).

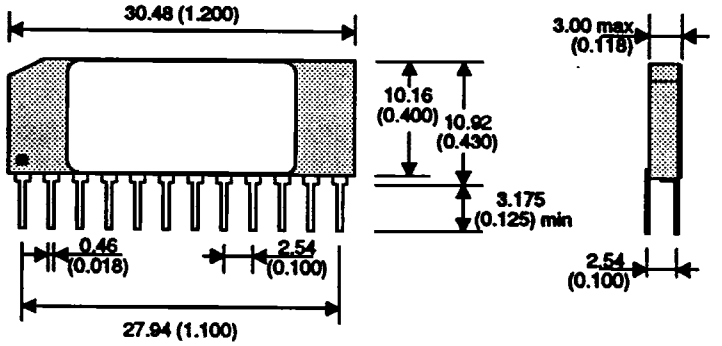
20 Pin Dual-In-Line ('K' Package)



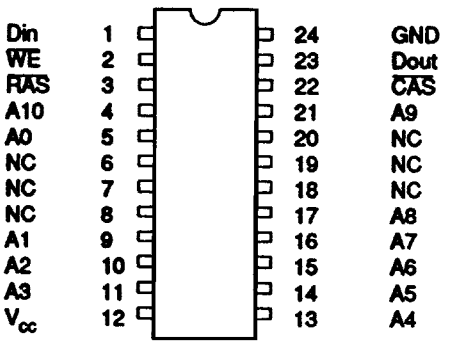
20 Pin Vertical-In-Line (VIL) ('V' Package)



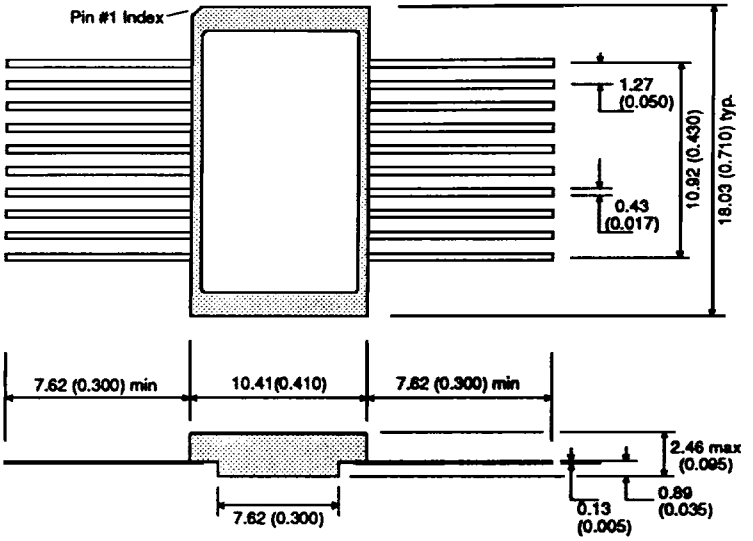
24 Pin Vertical-In-Line (VIL™) ('VX' Package)



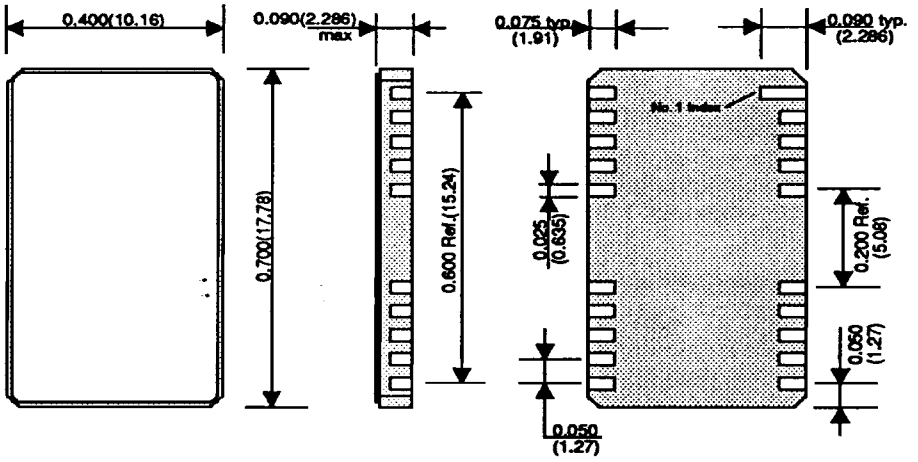
Pin Definition



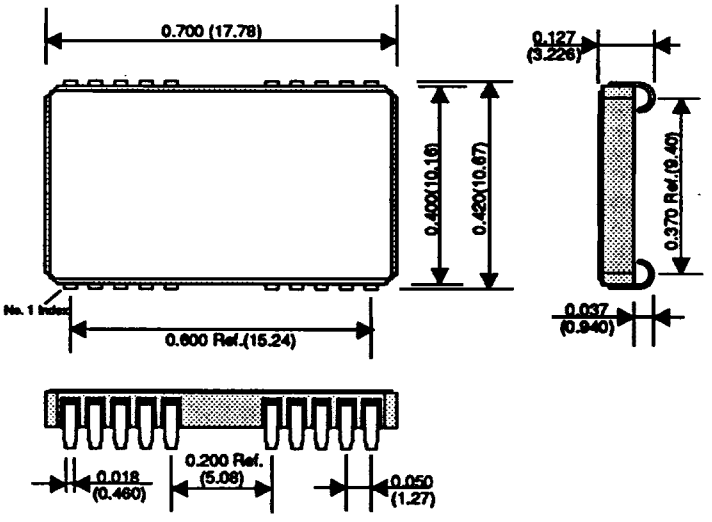
20 Pin Ceramic Flatpack ('G' Package)



20 Pad Ceramic Leadless Chip Carrier ('W' Package)



20 Pin Ceramic Leaded CSOJ ('J' Package)



Ordering Information

MDM14001WMB-80

Speed	80,100,120 ns	
Temp. range/screening	Blank	= Commercial Temp.
	I	= Industrial Temp.
	M	= Military Temp.
	MB	= Processed to MIL-STD-883 Method 5004, non-compliant.
Package	K	= 20 Pin 400 mil DIP
	V	= 20 Pin 100 mil Vertical-in-Line
	VX	= 24 Pin 100 mil Vertical-in-Line
	G	= 20 Pin Ceramic Flatpack
	W	= 20 Pad Ceramic LCC
	J	= 20 Pin Ceramic SOJ

Note: For more information regarding screening flows contact Mosaic Semiconductor Inc. for a 'Screening Flow Applications Note.'

The policy of the company is one of continuous development and while the information presented in this data sheet is believed to be accurate, no liability is assumed for any data contained within. The company reserves the right to make changes without notice at any time.

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