

# 512MB – 64Mx72 DDR2 SDRAM RDIMM, VLP, w/PLL

## FEATURES

- Registered VLP (very low profile) 240-pin, dual in-line memory module
- Fast data transfer rates: PC2-6400\*, PC2-5300, PC2-4300 and PC2-3200
- Utilizes 800\*, 667, 533 and 400 MT/s DDR2 SDRAM components
- $V_{CC} = V_{CCQ} = 1.8V$
- $V_{CCSPD} = 1.7V$  to  $3.6V$
- JEDEC standard 1.8V I/O (SSTL\_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- Multiple internal device banks for concurrent operation
- Programmable CAS# latency (CL): 3, 4, 5 and 6\*
- Adjustable data-output or drive strength
- On-die termination (ODT)
- Posted CAS# additive latency: (AL)
- Serial Presence Detect (SPD) with EEPROM
- Auto & Self Refresh (64ms: 8,192 cycle refresh)
- Gold edge contacts
- Single Rank
- RoHS compliant
- Package option
  - 240 Pin RDIMM (VLP)
  - PCB – 18.29mm (0.720") TYP

## DESCRIPTION

The W3HG64M72AER is a 64Mx72 Double Data Rate DDR2 SDRAM high density module. This memory module consists of eighteen 64Mx4 bit with 4 banks DDR2 SDRAMs in FBGA packages, mounted on a 240-pin RDIMM FR4 substrate.

\* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

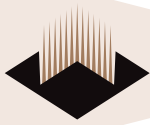
NOTE: Consult factory for availability of:

- Vendor source control options
- Industrial temperature option

## OPERATING FREQUENCIES

	PC2-3200	PC2-4300	PC2-5300	PC2-6400*
Clock Speed	200MHz	266MHz	333MHz	400MHz
CL-trcd-trp	3-3-3	4-4-4	5-5-5	6-6-6

\* Consult factory for availability



## PIN CONFIGURATION

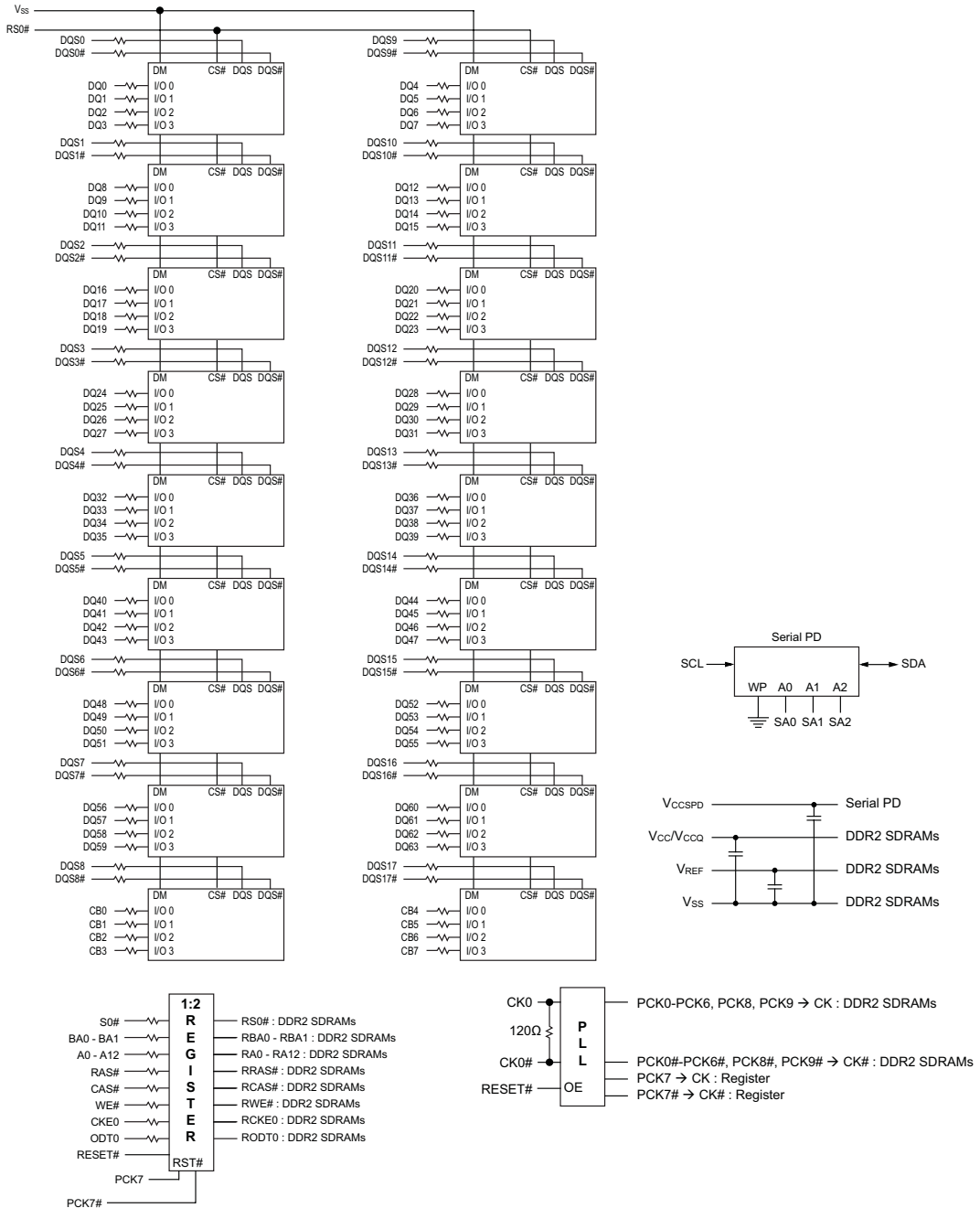
Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	VREF	61	A4	121	VSS	181	VCCQ
2	VSS	62	VCCQ	122	DQ4	182	A3
3	DQ0	63	A2	123	DQ5	183	A1
4	DQ1	64	VCC	124	VSS	184	VCC
5	VSS	65	VSS	125	DQS9	185	CK0
6	DQS0#	66	VSS	126	DQS9#	186	CK0#
7	DQS0	67	VCC	127	VSS	187	VCC
8	VSS	68	NC	128	DQ6	188	A0
9	DQ2	69	VCC	129	DQ7	189	VCC
10	DQ3	70	A10/AP	130	VSS	190	BA1
11	VSS	71	BA0	131	DQ12	191	VCCQ
12	DQ8	72	VCCQ	132	DQ13	192	RAS#
13	DQ9	73	WE#	133	VSS	193	S0#
14	VSS	74	CAS#	134	DQS10	194	VCCQ
15	DQS1#	75	VCCQ	135	DQS10#	195	ODT0
16	DQS1	76	NC	136	VSS	196	NC
17	VSS	77	NC	137	NC	197	VCC
18	RESET#	78	VCCQ	138	NC	198	VSS
19	NC	79	VSS	139	VSS	199	DQ36
20	VSS	80	DQ32	140	DQ14	200	DQ37
21	DQ10	81	DQ33	141	DQ15	201	VSS
22	DQ11	82	VSS	142	VSS	202	DQS13
23	VSS	83	DQS4#	143	DQ20	203	DQS13#
24	DQ16	84	DQS4	144	DQ21	204	VSS
25	DQ17	85	VSS	145	VSS	205	DQ38
26	VSS	86	DQ34	146	DQS11	206	DQ39
27	DQS2#	87	DQ35	147	DQS11#	207	VSS
28	DQS2	88	VSS	148	VSS	208	DQ44
29	VSS	89	DQ40	149	DQ22	209	DQ45
30	DQ18	90	DQ41	150	DQ23	210	VSS
31	DQ19	91	VSS	151	VSS	211	DQS14
32	VSS	92	DQS5#	152	DQ28	212	DQS14#
33	DQ24	93	DQS5	153	DQ29	213	VSS
34	DQ25	94	VSS	154	VSS	214	DQ46
35	VSS	95	DQ42	155	DQS12	215	DQ47
36	DQS3#	96	DQ43	156	DQS12#	216	VSS
37	DQS3	97	VSS	157	VSS	217	DQ52
38	VSS	98	DQ48	158	DQ30	218	DQ53
39	DQ26	99	DQ49	159	DQ31	219	VSS
40	DQ27	100	VSS	160	VSS	220	NC
41	VSS	101	SA2	161	CB4	221	NC
42	CB0	102	NC	162	CB5	222	VSS
43	CB1	103	VSS	163	VSS	223	DQS15
44	VSS	104	DQS6#	164	DQS17	224	DQS15#
45	DQS8#	105	DQS6	165	DQS17#	225	VSS
46	DQS8	106	VSS	166	VSS	226	DQ54
47	VSS	107	DQ50	167	CB6	227	DQ55
48	CB2	108	DQ51	168	CB7	228	VSS
49	CB3	109	VSS	169	VSS	229	DQ60
50	VSS	110	DQ56	170	VCCQ	230	DQ61
51	VCCQ	111	DQ57	171	NC	231	VSS
52	CKE0	112	VSS	172	VCC	232	DQS16
53	VCC	113	DQS7#	173	NC	233	DQS16#
54	NC	114	DQS7	174	NC	234	VSS
55	NC	115	VSS	175	VCCQ	235	DQ62
56	VCCQ	116	DQ58	176	A12	236	DQ63
57	A11	117	DQ59	177	A9	237	VSS
58	A7	118	VSS	178	VCC	238	VCCSPD
59	VCC	119	SDA	179	A8	239	SA0
60	A5	120	SCL	180	A6	240	SA1

## PIN NAMES

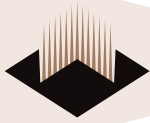
Pin Name	Function
CK0,CK0#	Clock Inputs
CKE0	Clock Enable
CB0-CB7	Check Bits
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
S0#	Chip Select
A0-A12	Address Inputs
BA0,BA1	Bank Address Inputs
ODT0	On-die termination control
DQ0-DQ63	Data Input/Output
DQS0-DQS17	Data strobes
DQS0#-DQS17#	Data strobes complement
VCC	Core and I/O Power (1.8V)
VSS	Ground
VREF	Input/Output Reference
VCCSPD	SPD Power
SCL	Serial Presence Detect (SPD) Clock Input
SDA	SPD Data Input/Output
SA0-SA2	SPD address Inputs
NC	Spare pins, No connect
RESET#	Register Reset Input



FUNCTIONAL BLOCK DIAGRAM



NOTE: All resistor values are 22 ohms unless otherwise specified.



**DC OPERATING CONDITIONS**

All voltages referenced to V<sub>SS</sub>

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply Voltage	V <sub>CC</sub>	1.7	1.8	1.9	V	3
I/O Reference Voltage	V <sub>REF</sub>	0.49 x V <sub>CC</sub>	0.50 x V <sub>CC</sub>	0.51 x V <sub>CC</sub>	V	1
I/O Termination Voltage	V <sub>TT</sub>	V <sub>REF</sub> -0.04	V <sub>REF</sub>	V <sub>REF</sub> +0.04	V	2
SPD Supply Voltage	V <sub>CCSPD</sub>	1.7	-	3.6	V	

Notes:

- V<sub>REF</sub> is expected to equal V<sub>CC/2</sub> of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V<sub>REF</sub> may not exceed +/-1 percent of the DC value. Peak-to-peak AC noise on V<sub>REF</sub> may not exceed +/-2 percent of V<sub>REF</sub>. This measurement is to be taken at the nearest V<sub>REF</sub> bypass capacitor.
- V<sub>TT</sub> is not applied directly to the device. V<sub>TT</sub> is a system supply for signal termination resistors, is expected to be set equal to V<sub>REF</sub> and must track variations in the DC level of V<sub>REF</sub>.
- V<sub>CCQ</sub> of all IC's are tied to V<sub>CC</sub>.

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Min	Max	Units	
V <sub>CC</sub>	Voltage on V <sub>CC</sub> pin relative to V <sub>SS</sub>	-0.5	2.3	V	
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on any pin relative to V <sub>SS</sub>	-0.5	2.3	V	
T <sub>STG</sub>	Storage Temperature	-55	100	°C	
I <sub>L</sub>	Input leakage current; Any input 0V<V <sub>IN</sub> <V <sub>CC</sub> ; V <sub>REF</sub> input 0V,V <sub>IN</sub> ,0.95V; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#,	-10	10	μA
		CK, CK#	-10	10	μA
I <sub>oz</sub>	Output leakage current; 0V<V <sub>IN</sub> <V <sub>CC</sub> ; DQs and ODT are disable	DQ, DQS, DQS#	-10	10	μA
I <sub>VREF</sub>	V <sub>REF</sub> leakage current; V <sub>REF</sub> = Valid V <sub>REF</sub> level		-46	46	μA



**OPERATING TEMPERATURE CONDITION**

Parameter	Symbol	Rating	Units	Notes
Operating Case Temperature (Commercial)	TOPER	0 to +85°C	°C	1, 2

NOTE:

1. Operation temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51.2
2. At 0 - 85°C, operation temperature range, all DRAM specification will be supported.

**INPUT DC LOGIC LEVEL**

All voltages referenced to V<sub>SS</sub>

Parameter	Symbol	Min	Max	Unit
Input High (Logic 1) Voltage	V <sub>IH</sub> (DC)	V <sub>REF</sub> + 0.125	V <sub>CC</sub> + 0.300	V
Input High (Logic 0) Voltage	V <sub>IL</sub> (DC)	-0.300	V <sub>REF</sub> - 0.125	V

**INPUT AC LOGIC LEVEL**

All voltages referenced to V<sub>SS</sub>

Parameter	Symbol	Min	Max	Unit
AC Input High (Logic 1) Voltage DDR2-400 & DDR2-533	V <sub>IH</sub> (AC)	V <sub>REF</sub> + 0.250	-	V
AC Input High (Logic 1) Voltage DDR2-667	V <sub>IH</sub> (AC)	V <sub>REF</sub> + 0.200	-	V
AC Input High (Logic 0) Voltage DDR2-400 & DDR2-533	V <sub>IL</sub> (AC)	-	V <sub>REF</sub> - 0.250	V
AC Input High (Logic 0) Voltage DDR2-667	V <sub>IL</sub> (AC)	-	V <sub>REF</sub> - 0.200	V

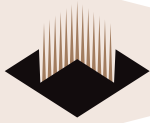


**DDR2 I<sub>CC</sub> SPECIFICATIONS AND CONDITIONS**

Includes DDR2 SDRAM components only

Symbol	Proposed Conditions	806	665	534	403	Units	
I <sub>CC0</sub>	Operating one bank active-precharge current; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ), t <sub>RC</sub> = t <sub>RC</sub> (I <sub>CC</sub> ), t <sub>RAS</sub> = t <sub>RASmin</sub> (I <sub>CC</sub> ); CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TDB	1,116	990	900	mA	
I <sub>CC1</sub>	Operating one bank active-read-precharge current; I <sub>OUT</sub> = 0mA; BL = 4, CL = CL(I <sub>CC</sub> ), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ), t <sub>RC</sub> = t <sub>RC</sub> (I <sub>CC</sub> ), t <sub>RAS</sub> = t <sub>RASmin</sub> (I <sub>CC</sub> ), t <sub>RCD</sub> = t <sub>RCD</sub> (I <sub>CC</sub> ); CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I <sub>DAD6W</sub>	TDB	1,278	1,080	990	mA	
I <sub>CC2P</sub>	Precharge power-down current; All banks idle; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ); CE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TDB	90	81	81	mA	
I <sub>CC2Q</sub>	Precharge quiet standby current; All banks idle; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ); CE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TDB	540	450	360	mA	
I <sub>CC2N</sub>	Precharge standby current; All banks idle; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ); CE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TDB	810	630	504	mA	
I <sub>CC3P</sub>	Active power-down current; All banks open; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ); CE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	TDB	342	288	234	mA
		Slow PDN Exit MRS(12) = 1	TDB	90	81	81	mA
I <sub>CC3N</sub>	Active standby current; All banks open; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ), t <sub>RAS</sub> = t <sub>RASmax</sub> (I <sub>CC</sub> ), t <sub>RP</sub> = t <sub>RP</sub> (I <sub>CC</sub> ); CE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TDB	810	630	540	mA	
I <sub>CC4W</sub>	Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(I <sub>CC</sub> ), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ), t <sub>RAS</sub> = t <sub>RASmax</sub> (I <sub>CC</sub> ), t <sub>RP</sub> = t <sub>RP</sub> (I <sub>CC</sub> ); CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TDB	2,070	1,710	1,350	mA	
I <sub>CC4R</sub>	Operating burst read current; All banks open, Continuous burst reads, I <sub>OUT</sub> = 0mA; BL = 4, CL = CL(I <sub>CC</sub> ), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ), t <sub>RAS</sub> = t <sub>RASmax</sub> (I <sub>CC</sub> ), t <sub>RP</sub> = t <sub>RP</sub> (I <sub>CC</sub> ); CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I <sub>DAD6W</sub>	TDB	1,980	1,620	1,260	mA	
I <sub>CC5B</sub>	Burst auto refresh current; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ); Refresh command at every t <sub>RFC</sub> (I <sub>CC</sub> ) interval; CE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TDB	1,710	1,620	1,530	mA	
I <sub>CC6</sub>	Self refresh current; CK and CK# at 0V; CE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	TDB	81	81	81	mA	
I <sub>CC7</sub>	Operating bank interleave read current; All bank interleaving reads, I <sub>OUT</sub> = 0mA; BL = 4, CL = CL(I <sub>CC</sub> ), AL = t <sub>RCD</sub> (I <sub>CC</sub> ) - 1 * t <sub>CK</sub> (I <sub>CC</sub> ); t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ), t <sub>RC</sub> = t <sub>RC</sub> (I <sub>CC</sub> ), t <sub>RRD</sub> = t <sub>RRD</sub> (I <sub>CC</sub> ), t <sub>RCD</sub> = 1 * t <sub>CK</sub> (I <sub>CC</sub> ); CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as I <sub>DAD6R</sub> ; Refer to the following page for detailed timing conditions	TDB	2,484	2,430	2,250	mA	

Note: I<sub>CC</sub> specification is based on QIMONDA components. Other DRAM Manufacturers specification may be different.

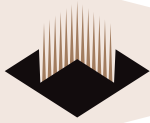


**DDR2 SDRAM COMPONENT AC TIMING PARAMETERS & SPECIFICATIONS**

AC CHARACTERISTICS			SYMBOL	806		665		534		403		UNIT
PARAMETER				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Clock	Clock cycle time	CL = 6	t <sub>CK</sub> (6)	TBD	TBD							ps
		CL = 5	t <sub>CK</sub> (5)	TBD	TBD	3,000	8,000	3,750	8,000	5,000	8,000	ps
		CL = 4	t <sub>CK</sub> (4)	TBD	TBD	3,750	8,000	3,750	8,000	5,000	8,000	ps
		CL = 3	t <sub>CK</sub> (3)	TBD	TBD	5,000	8,000	5,000	8,000	5,000	8,000	ps
	CK high-level width		t <sub>CH</sub>	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	t <sub>CK</sub>
	CK low-level width		t <sub>CL</sub>	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	t <sub>CK</sub>
Half clock period		t <sub>HP</sub>	TBD	TBD	MIN (t <sub>CH</sub> , t <sub>CL</sub> )		MIN (t <sub>CH</sub> , t <sub>CL</sub> )		MIN (t <sub>CH</sub> , t <sub>CL</sub> )		ps	
Data	DQ output access time from CK/CK#		t <sub>AC</sub>	TBD	TBD	-450	+450	-500	+500	-600	+600	ps
	Data-out high-impedance window from CK/CK#		t <sub>HZ</sub>	TBD	TBD		t <sub>AC</sub> MAX		t <sub>AC</sub> MAX		t <sub>AC</sub> MAX	ps
	Data-out low-impedance window from CK/CK#		t <sub>LZ</sub>	TBD	TBD	2x t <sub>AC</sub> MIN	t <sub>AC</sub> MAX	2x t <sub>AC</sub> MIN	t <sub>AC</sub> MAX	2x t <sub>AC</sub> MIN	t <sub>AC</sub> MAX	ps
	DQ and DM input setup time relative to DQS		t <sub>DS</sub>	TBD	TBD	100		100		150		ps
	DQ and DM input hold time relative to DQS		t <sub>DH</sub>	TBD	TBD	175		225		275		ps
	A DQ and DM input pulse width (for each input)		t <sub>DLPW</sub>	TBD	TBD	0.35		0.35		0.35		t <sub>CK</sub>
	Data hold skew factor		t <sub>QHS</sub>	TBD	TBD	340			400		450	ps
	DQ - DQS hold, DQS to first DQ to go nonvalid, per access		t <sub>QH</sub>	TBD	TBD	t <sub>HP</sub> - t <sub>QHS</sub>		t <sub>HP</sub> - t <sub>QHS</sub>		t <sub>HP</sub> - t <sub>QHS</sub>		ps
Data Strobe	DQS input high pulse width		t <sub>DQSH</sub>	TBD	TBD	0.35		0.35		0.35		t <sub>CK</sub>
	DQS input low pulse width		t <sub>DQSL</sub>	TBD	TBD	0.35		0.35		0.35		t <sub>CK</sub>
	DQS output access time from CK/CK#		t <sub>DQSCK</sub>	TBD	TBD	-400	+400	-450	+450	-500	+500	ps
	DQS falling edge to CK rising - setup time		t <sub>DSS</sub>	TBD	TBD	0.2		0.2		0.2		t <sub>CK</sub>
	DQS falling edge from CK rising - hold time		t <sub>DSH</sub>	TBD	TBD	0.2		0.2		0.2		t <sub>CK</sub>
	DQS - DQ skew, DQS to last DQ valid, per group, per access		t <sub>DQSQ</sub>	TBD	TBD		240		300		350	ps
	DQS read preamble		t <sub>RPRE</sub>	TBD	TBD	0.9	1.1	0.9	1.1	0.9	1.1	t <sub>CK</sub>
	DQS read postamble		t <sub>RPST</sub>	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>CK</sub>
	DQS write preamble		t <sub>WPRE</sub>	TBD	TBD	0.35		0.35		0.35		t <sub>CK</sub>
	DQS write postamble		t <sub>WPST</sub>	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>CK</sub>
	Write command to first DQS latching transition		t <sub>DQSS</sub>	TBD	TBD	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	t <sub>CK</sub>

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Note: AC specification is based on QIMONDA components. Other DRAM manufactures specification may be different



**DDR2 SDRAM COMPONENT AC TIMING PARAMETERS & SPECIFICATIONS (cont'd)**

AC CHARACTERISTICS		SYMBOL	806		665		534		403		UNIT
PARAMETER			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Command and Address	Address and control input pulse width for each input	tIPW	TBD	TBD	0.6		0.6		0.6		tCK
	Address and control input setup time	tIS	TBD	TBD	200		250		350		ps
	Address and control input hold time	tIH	TBD	TBD	275		375		475		ps
	CAS# to CAS# command delay	tCCD	TBD	TBD	2		2		2		tCK
	ACTIVE to ACTIVE (same bank) command	trc	TBD	TBD	60		60		55		ns
	ACTIVE bank a to ACTIVE bank b command	trRD	TBD	TBD	7.5		7.5		7.5		ns
	ACTIVE to READ or WRITE delay	trCD	TBD	TBD	15		15		15		ns
	ACTIVE to PRECHARGE command	trAS	TBD	TBD	45	70,000	45	70,000	40	70,000	ns
	Internal READ to precharge command delay	trTP	TBD	TBD	7.5		7.5		7.5		ns
	6 Write recovery time	tWR	TBD	TBD	15		15		15		ns
	Auto precharge write recovery + precharge time	tDAL	TBD	TBD	tWR + trP		tWR + trP		tWR + trP		ns
	Internal WRITE to READ command delay	tWTR	TBD	TBD	7.5		7.5		7.5		ns
	PRECHARGE command period	trP	TBD	TBD	15		15		15		ns
	LOAD MODE command cycle time	tMRD	TBD	TBD	2		2		2		tCK
	OCD Drive mode delay	toIT	TBD	TBD	0	12	0	12	0	12	ns
CKE low to CK,CK# uncertainty	tDELAY	TBD	TBD	tIS + tCK + tIH		tIS + tCK + tIH		tIS + tCK + tIH		ns	
Refresh	REFRESH to REFRESH command interval	trFC	TBD	TBD	75		75		75		ns
	Average periodic refresh interval	trEFI	TBD	TBD		7.8		7.8		7.8	µs
Self Refresh	Exit self refresh to non-READ command	txSNR	TBD	TBD	trFC + 10		trFC + 10		trFC + 10		ns
	Exit self refresh to READ command	txSRD	TBD	TBD	200		200		200		tCK

Continued on next page

Note: AC specification is based on QIMONDA components. Other DRAM manufactures specification may be different





**DDR2 SDRAM COMPONENT AC TIMING PARAMETERS & SPECIFICATIONS (cont'd)**

	AC CHARACTERISTICS		806		665		534		403		UNIT
	PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
ODT	ODT turn-on delay	t <sub>AO</sub> ND	TBD	TBD	2	2	2	2	2	2	t <sub>CK</sub>
	ODT turn-on	t <sub>AO</sub> N	TBD	TBD	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX) + 700	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX) + 1,000	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX) + 1,000	ps
	ODT turn-off delay	t <sub>AO</sub> FD	TBD	TBD	2.5	2.5	2.5	2.5	2.5	2.5	t <sub>CK</sub>
	ODT turn-off	t <sub>AO</sub> F	TBD	TBD	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX) + 600	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX) + 600	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX) + 600	ps
	ODT turn-on (power-down mode)	t <sub>AO</sub> NP	TBD	TBD	t <sub>AC</sub> (MIN) + 2,000	2 x t <sub>CK</sub> + t <sub>AC</sub> (MAX) + 1,000	t <sub>AC</sub> (MIN) + 2,000	2 x t <sub>CK</sub> + t <sub>AC</sub> (MAX) + 1,000	t <sub>AC</sub> (MIN) + 2,000	2 x t <sub>CK</sub> + t <sub>AC</sub> (MAX) + 1,000	ps
	ODT turn-off (power-down mode)	t <sub>AO</sub> FP	TBD	TBD	t <sub>AC</sub> (MIN) + 2,000	2.5 x t <sub>CK</sub> + t <sub>AC</sub> (MAX) + 1,000	t <sub>AC</sub> (MIN) + 2,000	2.5 x t <sub>CK</sub> + t <sub>AC</sub> (MAX) + 1,000	t <sub>AC</sub> (MIN) + 2,000	2.5 x t <sub>CK</sub> + t <sub>AC</sub> (MAX) + 1,000	ps
	ODT to power-down entry latency	t <sub>AN</sub> PD	TBD	TBD	3		3		3		t <sub>CK</sub>
	ODT power-down exit latency	t <sub>AX</sub> PD	TBD	TBD	8		8		8		t <sub>CK</sub>
	Power-Down	Exit active power-down to READ command, MR[bit12=0]	t <sub>XAR</sub> D	TBD	TBD	2		2		2	
Exit active power-down to READ command, MR[bit12=1]		t <sub>XAR</sub> DS	TBD	TBD	7 - AL		6 - AL		6 - AL		t <sub>CK</sub>
A Exit precharge power-down to any non-READ command.		t <sub>X</sub> P	TBD	TBD	2		2		2		t <sub>CK</sub>
CKE minimum high/low time		t <sub>CKE</sub>	TBD	TBD	3		3		3		t <sub>CK</sub>

Note: AC specification is based on Q1MONDA components. Other DRAM manufactures specification may be different.



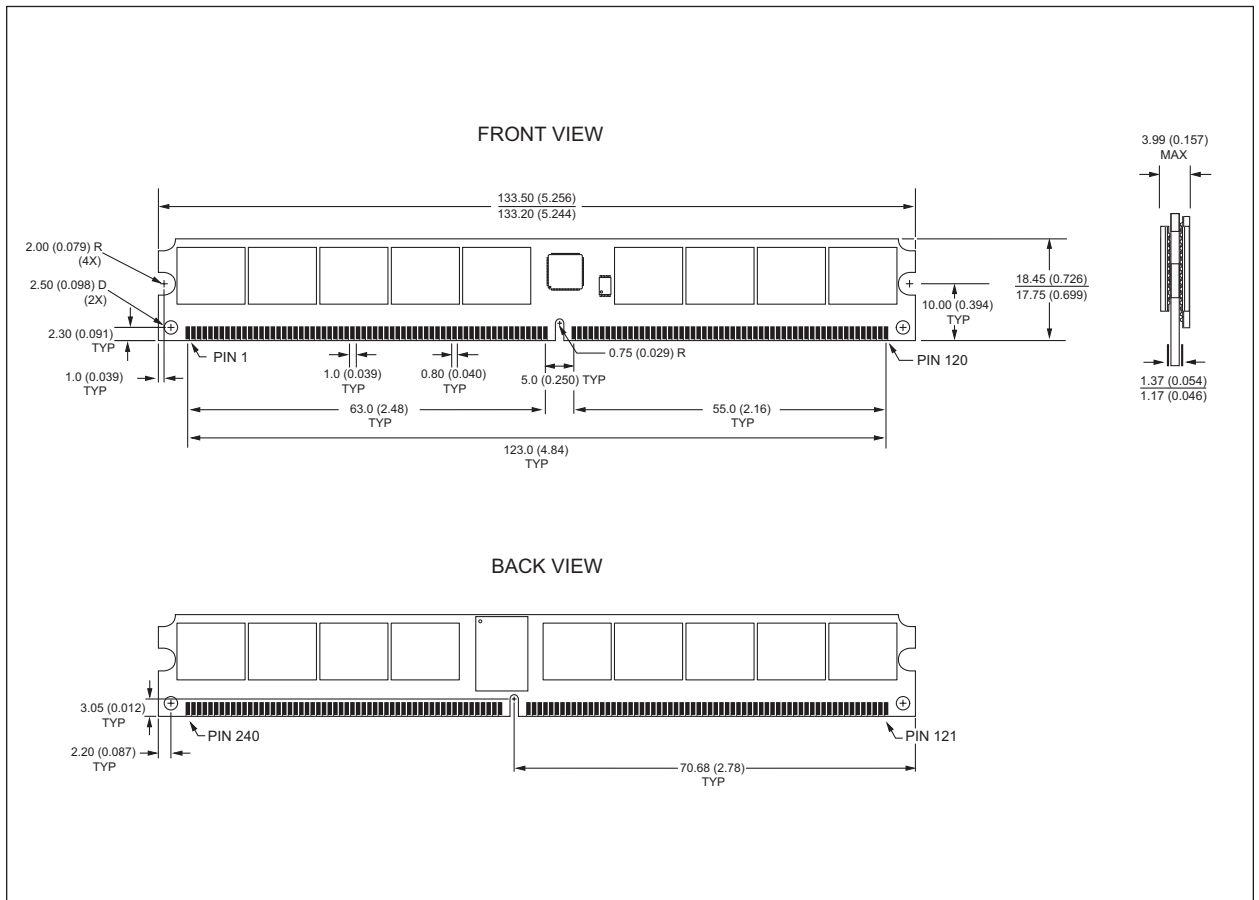
ORDERING INFORMATION FOR AD6

Part Number	Speed	CAS Latency	t <sub>RC</sub> D	t <sub>RP</sub>	Height*
W3HG64M72AER806AD6xxG	400MHz/800Mb/s	6	6	6	18.29mm (0.72") TYP
W3HG64M72AER665AD6xxG	333MHz/667Mb/s	5	5	5	18.29mm (0.72") TYP
W3HG64M72AER534AD6xxG	266MHz/533Mb/s	4	4	4	18.29mm (0.72") TYP
W3HG64M72AER403AD6xxG	200MHz/400Mb/s	3	3	3	18.29mm (0.72") TYP

NOTES:

- For part numbering interpretation, please see "part numbering guide" on page 11.

PACKAGE DIMENSIONS FOR AD6

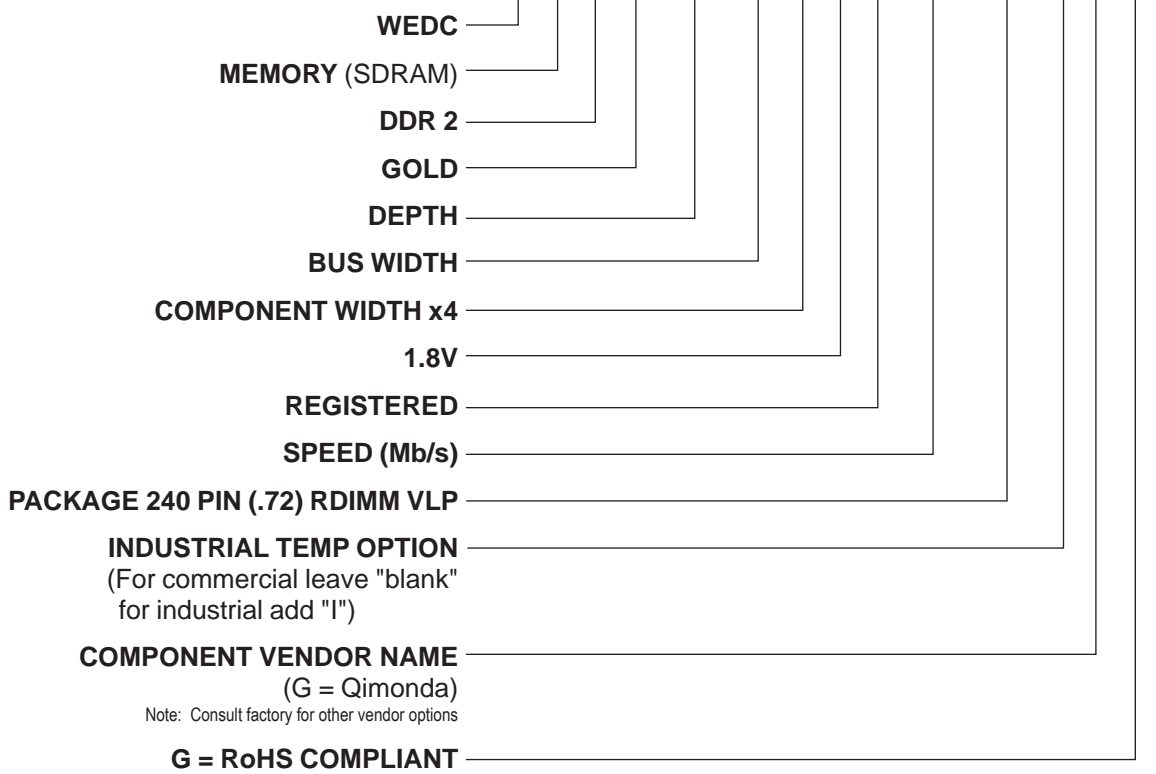


\* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)



PART NUMBERING GUIDE

W 3 H G 64M 72 A E R xxx AD6 x x G





## Document Title

512MB – 64Mx72 DDR2 SDRAM RDIMM, VLP, w/PLL

## DRAM DIE OPTIONS:

- QIMONDA: A-Die

## Revision History

<b>Rev #</b>	<b>History</b>	<b>Release Date</b>	<b>Status</b>
Rev 0	Created	January 2007	Concept
Rev 1	1.0 Updated Icc, AC and operating specifications	February 2007	Advanced
	1.1 Updated packing diagram		
	1.2 Moved from concept to advanced		