Z86C30/C31

CMOS Z8® 8-BIT CCP™ CONSUMER CONTROLLER PROCESSORS

FEATURES

- The Z86C30/C31 Devices Have the Following General Characteristics:

Part	ROM	RAM	Speed
Z86C30	4 Kbyte	236 Bytes	12 MHz
Z86C31	2 Kbyte	124 Bytes	8 MHz

- 28-Pin Package Styles (DIP, SOIC, PCB Chip Carrier)
- 3.0 to 5.5 Volt Operating Range
- Operating Temperature: –40° to +105°C
- Low Power Consumption: 50 mW (Typical)
- Fast Instruction Pointer: 1.5 µs @ 8 MHz (Z86C31), 1.0 µs @ 12 MHz (Z86C30)
- Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler
- Two Standby Modes: STOP and HALT
- ROM Protect Option
- RAM Protect Option (Z86C30 Only)
- 24 Input/Output Lines (Two with Comparator Inputs)
- Seven Digital Inputs CMOS Levels, Schmitt-Triggered
- Three Digital Inputs CMOS Levels
- Three Expanded Register File Control Registers
- Low Voltage Protection
- Watch-Dog/Power-On Reset Timers
- Two Comparators with Programmable Interrupt Polarity
- Six Vectored, Priority Interrupts from Six Different Sources
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive.
- Software Programmable Low EMI Mode
- Open-Drain Mode on Three Ports
- Auto Latches

GENERAL DESCRIPTION

The Z86C30/C31 CCP™ (Consumer Controller Processors) are members of Zilog's the Z8® single-chip microcontroller family with enhanced wake-up circuitry, programmable watch-dog timers and low noise/EMI options. These enhancements result in a more efficient, cost-effective design and provide the user with increased design flexibility over the standard Z8 microcontroller core. With 4K/2K bytes of ROM and 236/124 bytes of RAM for the Z86C30 and Z86C31, respectively, these low cost, low power consumption CMOS microcontrollers offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

The Z86C30/C31 architecture is characterized by Zilog's 8-bit microcontroller core with an Expanded Register File to allow easy access to register mapped peripheral and I/O circuits. These devices offer a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many industrial, automotive, and industrial applications.

For applications demanding powerful I/O capabilities, the Z86C30/C31 provides 24 pins dedicated to input and output. These lines are grouped into three ports, eight lines per port, and are configurable under software control to provide timing, status signals, and parallel I/O with or without handshake.

GENERAL DESCRIPTION (Continued)

Three basic address spaces are available to support this wide range of configurations: Program Memory, Register File, and Expanded Register File. The Register File is composed of 236/124 bytes of general-purpose registers, three I/O port registers and 15 control and status registers. The Expanded Register File consists of three Control registers.

To unburden the system from coping with real-time tasks, such as counting/timing and input/output data communication, the Z86C30/C31 offers two on-chip counter/timers with a large number of user-selectable modes, and on-board comparators to process analog signals with a common reference voltage (Figure 1).

With powerful peripheral features such as on-board comparators, counter/timer(s), Watch-Dog Timer (WDT), the Z86C30/C31 meets the needs of a variety of sophisticated controller applications.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

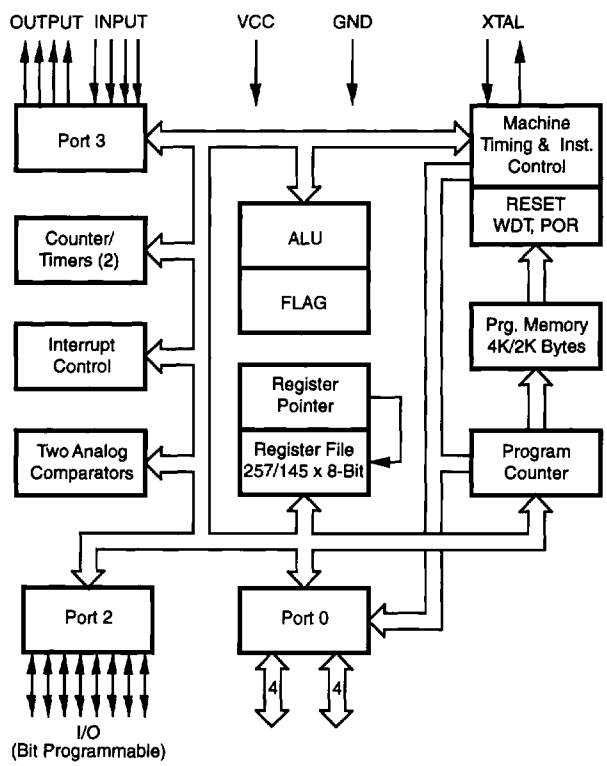

Figure 1. Z86C30/C31 Functional Block Diagram

PIN DESCRIPTION

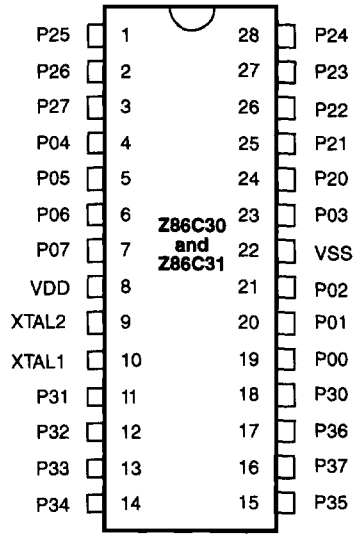

Figure 2. 28-Pin DIP* Pin Configuration

Table 1. 28-Pin DIP* Pin Identification

Pin #	Symbol	Function	Direction
1-3	P25-27	Port 2, Pins 5,6,7	In/Output
4-7	P04-07	Port 0, Pins 4,5,6,7	In/Output
8	V_{CC}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P04-07	Port 3, Pins 1,2,3	Fixed Input
14-15	P34-35	Port 3, Pins 4,5	Fixed Output
16	P37	Port 3, Pin 7	Fixed Output
17	P36	Port 3, Pin 6	Fixed Output
18	P30	Port 3, Pin 0	Fixed Input
19-21	P00-02	Port 0, Pins 0,1,2	In/Output
22	GND	Ground	
23	P03	Port 0, Pins 3	In/Output
24-28	P20-24	Port 2, Pins 0,1,2,3,4	In/Output

Note:
* SOIC style package is identical in pin identification and configuration.

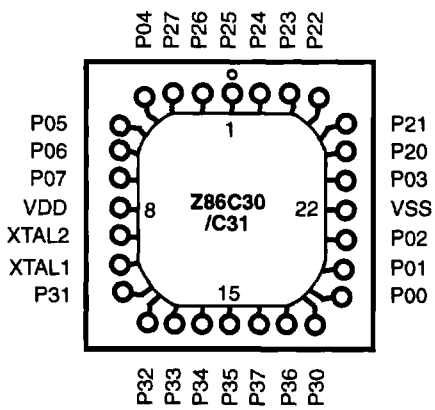

Figure 3. 28-Pin PCB Chip Carrier Pin Configuration

Table 2. 28-Pin PCB Chip Carrier Pin Identification

Pin #	Symbol	Function	Direction
1-3	P25-27	Port 2, Pins 5,6,7	In/Output
4-7	P04-07	Port 0, Pins 4,5,6,7	In/Output
8	V_{CC}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P04-07	Port 3, Pins 1,2,3	Fixed Input
14-15	P34-35	Port 3, Pins 4,5	Fixed Output
16	P37	Port 3, Pin 7	Fixed Output
17	P36	Port 3, Pin 6	Fixed Output
18	P30	Port 3, Pin 0	Fixed Input
19-21	P00-02	Port 0, Pins 0,1,2	In/Output
22	GND	Ground	
23	P03	Port 0, Pins 3	In/Output
24-28	P20-24	Port 2, Pins 0,1,2,3,4	In/Output

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PIN FUNCTIONS

XTAL1. *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network or external single-phase clock to the on-chip oscillator input.

XTAL2. *Crystal 2* (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network to the on-chip oscillator output.

Port 0 (P07-P00). Port 0 is an 8-bit, bi-directional, CMOS compatible I/O port. These eight I/O lines can be nibble programmed as P03-P00 input/output and P07-P04 input/output, separately. The input buffers are Schmitt-Triggered and nibbles programmed as outputs can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 can also be used as a handshake I/O port.

In Handshake Mode, Port 3 lines P32 and P35 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to Port 0's upper nibble. The lower nibble must have the same direction as the upper nibble (Figure 4).

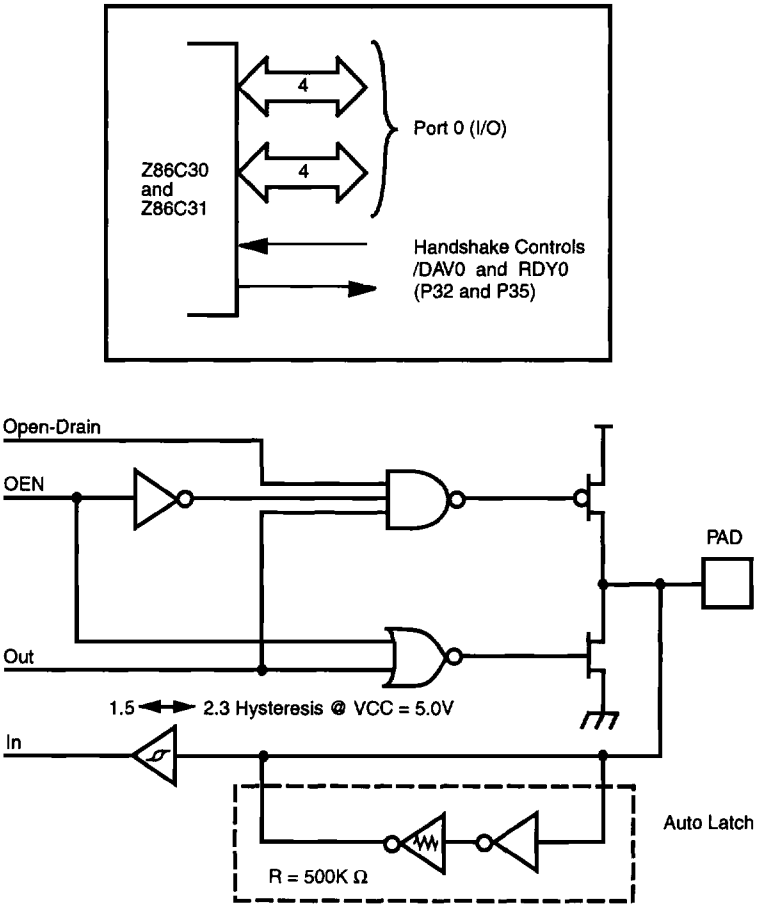

Figure 4. Port 0 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit, bi-directional, CMOS compatible I/O port. These eight I/O lines can be configured under software control as inputs or outputs, independently. All input buffers are Schmitt-Triggered. Bits programmed as outputs may be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. When used as an I/O port, Port 2 can be placed under handshake control. In Handshake Mode, Port 3 lines P31 and P36 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to bit 7 of Port 2 (Figure 5)

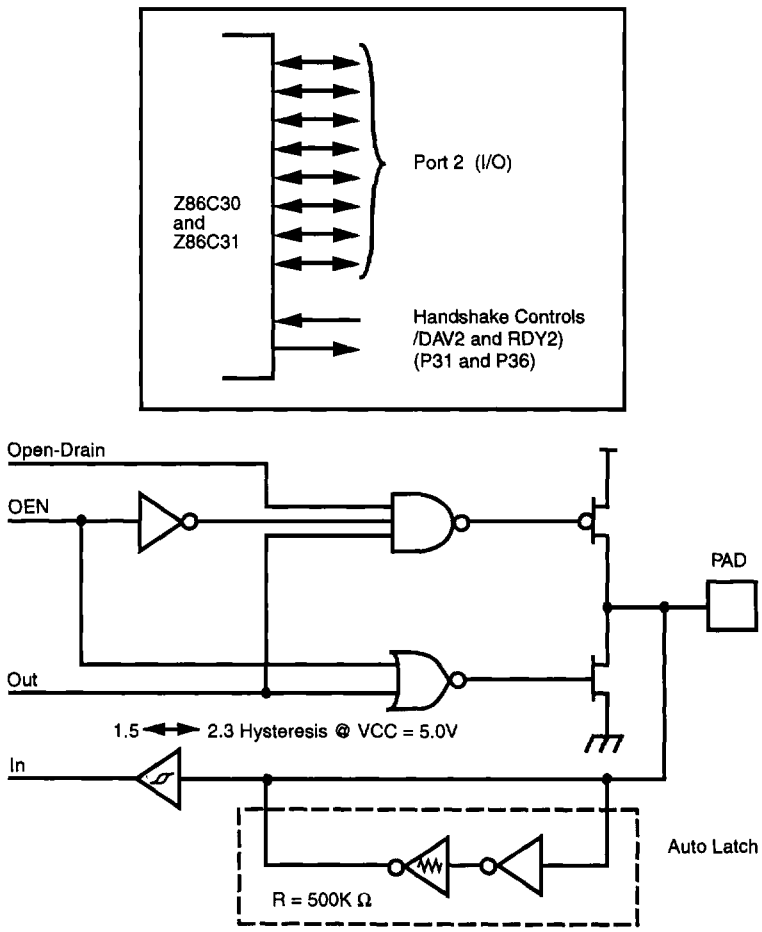

Figure 5. Port 2 Configuration

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PIN FUNCTIONS (Continued)

Port 3 (P37-P30). Port 3 is an 8-bit, CMOS compatible port. These eight lines consist of four fixed inputs (P33-P30) and four fixed outputs (P37-P34), and can be configured under software for interrupt and port handshake functions. Port 3 pin 0 input is Schmitt-triggered. Pins P31, P32 and P33 are standard CMOS inputs (no auto latches) and pins P34, P35, P36, P37 are push-pull output lines. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The comparator output can be outputted from P34 and P37, respectively, by setting PCON register (PCON) bit D0 to 1. The analog function is enabled by programming the Port 3 Mode Register (P3M) (bit D1) for interrupt function. P30 and P33 are falling edge interrupt inputs. P31 and P32 are programmable as falling, rising, or both edge triggered interrupts (IRQ register bits 6 and 7). In Analog Mode, P33 is the comparator reference voltage input.

Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Ports 0 and 2 are available on P3 pin 1 through 6 (Figure 6).

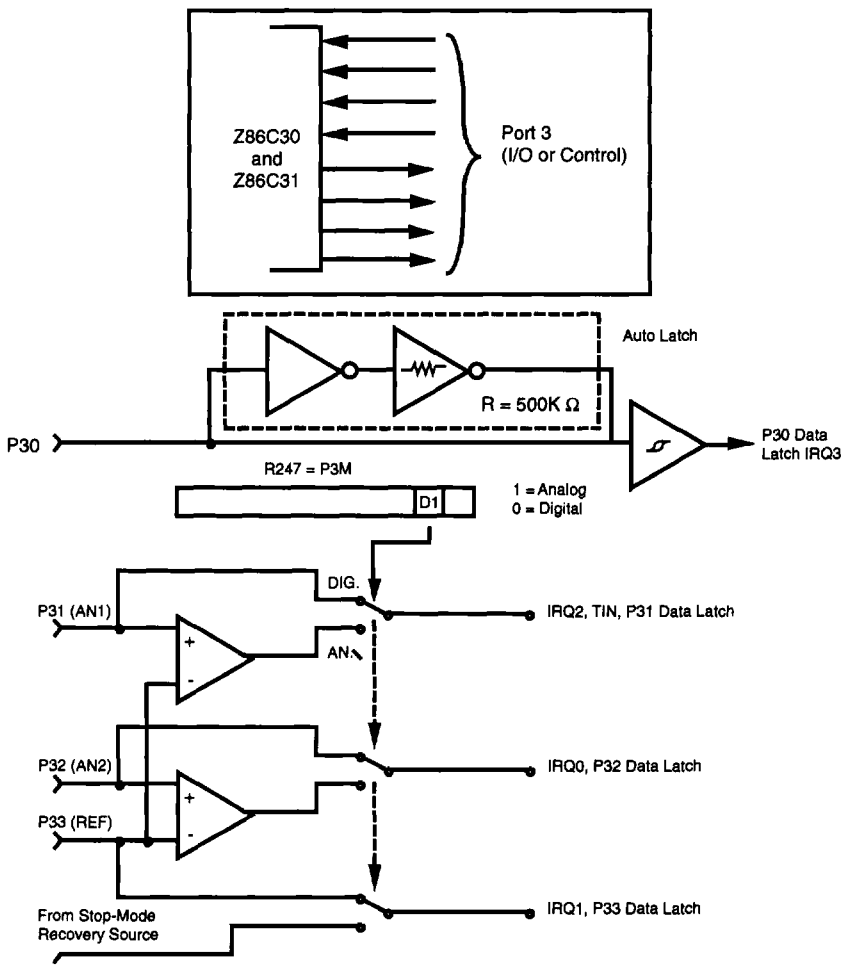

Figure 6. Port 3 Configuration

Table 3. Port 3 Pin Assignments

Pin	I/O	CTC1	Analog	Int.	P0 HS	P2 HS
P30	IN			IRQ3		
P31	IN	T_{IN}	AN1	IRQ2		D/R
P32	IN		AN2	IRQ0	D/R	
P33	IN		REF	IRQ1		
P34	OUT		AN1-OUT			
P35	OUT				R/D	
P36	OUT	T_{OUT}				R/D
P37	OUT		AN2-OUT			

Notes:
HS = Handshake Signals
D = DAV
R = RDY

Comparator Inputs. Port 3 Pin P31 and P32 each have a comparator front end. The comparator reference voltage, Pin P33, is common to both comparators. In analog mode, the P31 and P32 are the positive inputs to the comparators, and P33 is the reference voltage supplied to both comparators. In analog mode, the P31 and P32 are the positive inputs to the comparators, and P33 is the reference voltage supplied to both comparators. In digital mode, pin P33 can be used as a P33 register input or IRQ1 source. The comparator outputs can be programmed out on P34 and P37 by setting the PCON register bit D0 to a 1 state.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. Whether this is 0 or 1, cannot be determined. A valid CMOS level, rather than a floating mode, reduces excessive supply current flow is the input buffer.

Note: Deletion of all port pin auto latches is available as a ROM mask option. The auto latch delete option is selected by the customer when the ROM code is submitted. P01M reg. bit D4 and D3 must be "0" with the Auto Latch Delete option.

Low EMI Emission. The Z86C30/C31 can be programmed to operate in a low EMI emission mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 200 Ohms (typical).
- Low EMI Oscillator.
- Internal SCLK/TCLK = XTAL operation limited to a maximum of 4 MHz - 250 ns cycle time, when Low EMI Oscillator is selected and system clock (SCLK = XTAL, SMR Reg. Bit D1 =1).

FUNCTIONAL DESCRIPTION

The following special functions have been incorporated into the Z86C30/C31 CCPs to enhance the standard Z8® core architecture to provide the user with increased design flexibility.

Reset. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- Stop-Mode Recovery Source
- Low Voltage Recovery

Having the auto Power-on Reset circuitry built-in, the Z86C30/C31 does not require an external reset circuit. The reset time is 5 ms (typical), plus 18 clock cycles.

The Z86C30/C31 does not re-initialize WDTMR, SMR, P2M, PCON and P3M registers to their reset values on a Stop-Mode Recovery operation.

Program Memory. The Z86C30/C31 can address up to 4K/2K bytes of internal program memory (Figure 7). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six, 16-bit vectors that correspond to the six available interrupts. Address 12 to 4095/2047 are reserved for the user ROM Program. After reset, the program counter points to the program start address at 000CH.

ROM Protect. The 4K/2K bytes of program memory is mask programmable. **A ROM protect feature prevents "dumping" of the ROM contents by inhibiting execution of LDC and LDCI instructions to program memory in ALL modes. A ROM look up table cannot be used with this feature selected.**

The ROM protect option is mask-programmable and is selected by the customer when the ROM code is submitted.

Expanded Register File (ERF). The register file has been expanded to allow for additional system control registers, mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 8). These register groups are known as the Expanded Register File (ERF).

Bits 3-0 of the Register Pointer (RP) select the active ERF group. Bits 7-4 of register RP select the working register group (Figure 9). Three system configuration registers reside in the Expanded Register File at bank F (PCON, SMR, WDTMR). The rest of the Expanded Register is not physically implemented and is open for future expansion.

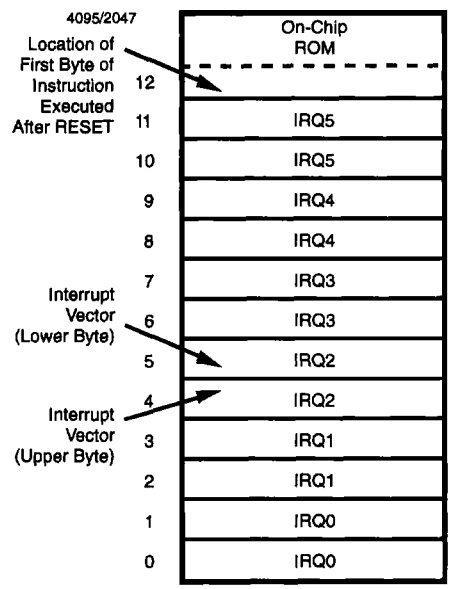

Figure 7. Program Memory Map

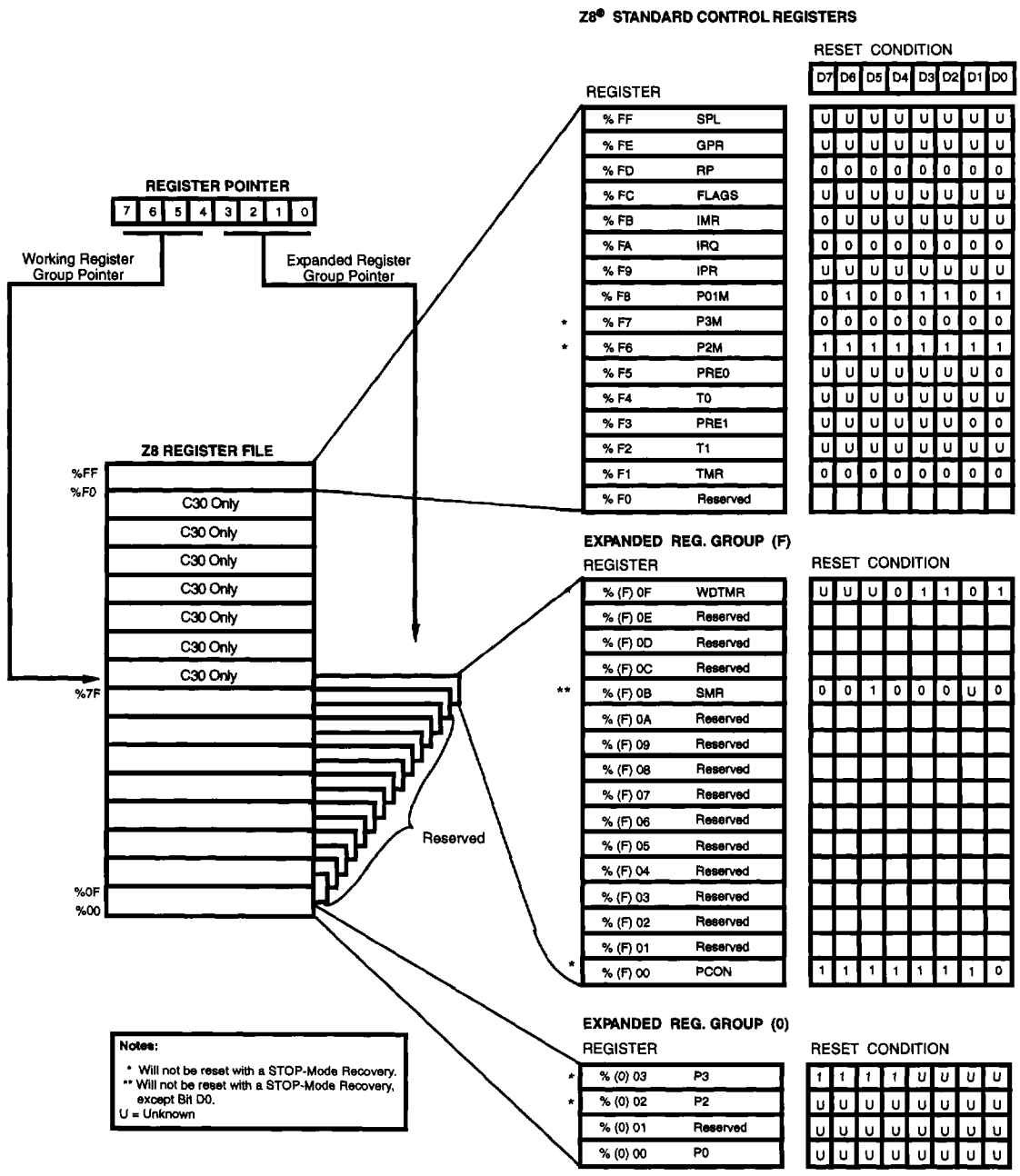

Figure 8. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)

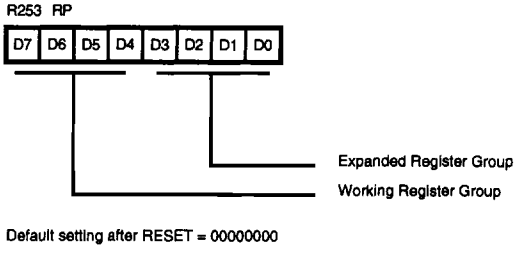

Figure 9. Register Pointer Register

Register File. The register file consists of three I/O port registers, 236/124 general-purpose registers and 15 control and status registers and three system configuration registers in the expanded register group (See Figure 8). The instructions can access registers directly or indirectly through an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 9 and 10). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group. The general-purpose registers on device power-up are undefined.

Note: Register Bank E0-EF can only be accessed through working register and indirect addressing modes. (This bank is available in Z86C30 only.)

General Purpose Register (GPR). The general purpose registers are undefined after the device is powered-up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general purpose register.

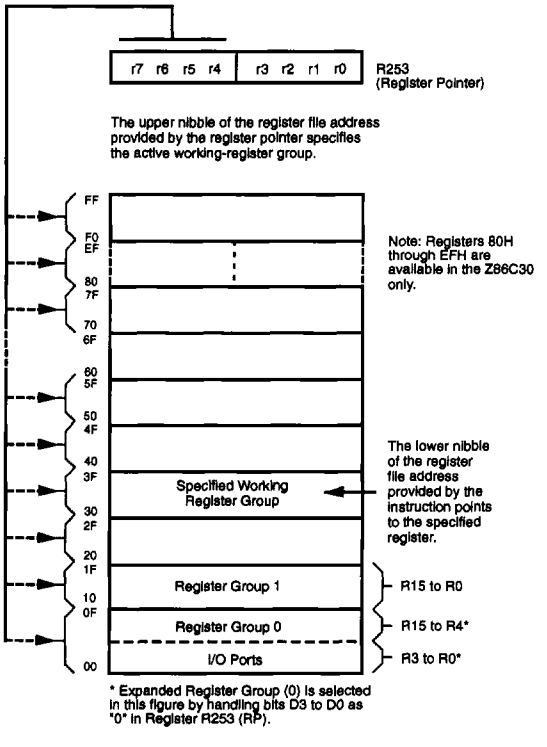

Figure 10. Register Pointer

RAM Protect (Z86C30 Only). The upper portion of the RAM's address spaces %80 to %EF (excluding the control registers) can be protected from reading and writing. The RAM Protect bit option is mask-programmable and is selected by the customer when the ROM code is submitted. After the mask option is selected, the user can activate from the internal ROM code to turn off/on the RAM Protect by loading a bit D6 in the IMR register to either a 0 or a 1, respectively. A 1 in D6 indicates RAM Protect enabled.

Stack. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236/124 general-purpose registers.

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 11).

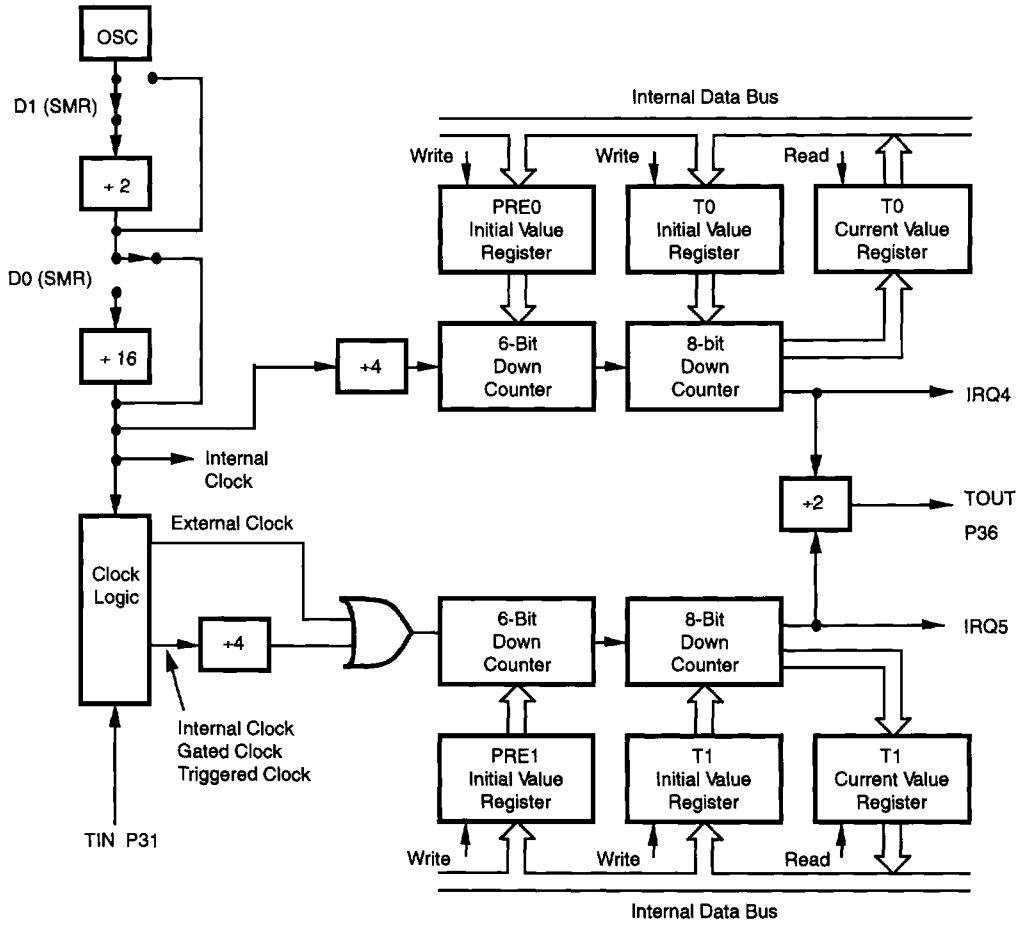

Figure 11. Counter/Timer Block Diagram

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FUNCTIONAL DESCRIPTION (Continued)

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock; a trigger input that can be retriggerable or not-retriggerable; or as a gate input for the internal clock. Port 3 line P36 serves as a timer output (T_{OUT}) through which T0, T1 or the internal clock are output. The counter/timers can be cascaded by connecting the T0 output to the input of T1. T_{IN} Mode is enabled by setting R243 PRE1 Bit D1 to 0.

Interrupts. The Z86C30/C31 has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 12). The six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30 and two in counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 4).

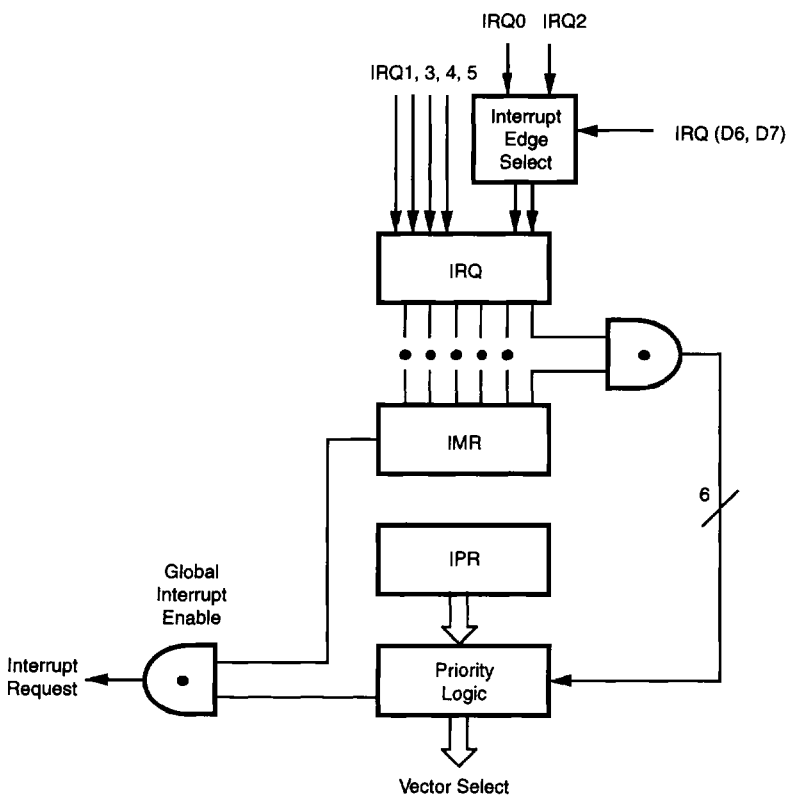

Figure 12. Interrupt Block Diagram

Table 4. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rising/Falling Edge Triggered
IRQ1,	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	/DAV2, IRQ2, T_{IN}	4, 5	External (P31), Rising/Falling Edge Triggered
IRQ3	IRQ3	6, 7	External (P30), Falling Edge Triggered
IRQ4	T0	8, 9	Internal
IRQ5	T1	10, 11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted; it disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86C30/C31 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling or both edge triggered, and are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is shown in Table 5.

Table 5. IRQ Register

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

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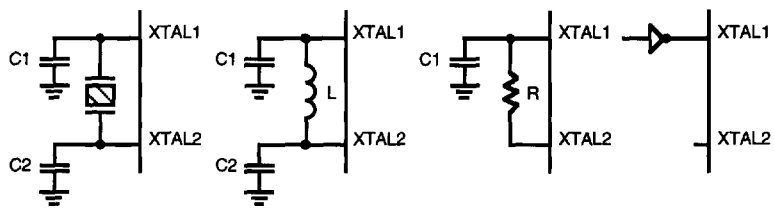
FUNCTIONAL DESCRIPTION (Continued)

Clock. The Z86C30/C31 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 kHz to 12 MHz max., with a series resistance (RS) less than, or equal to, 100 Ohms. (**Note:** The Z86C31 is 8 MHz max.)

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitors values from each pin directly to Ground, pin 22. This is to reduce ground noise injection. The RC oscillator option is mask-programmable, to be selected by the customer at the time ROM code is submitted. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to Ground (Figure 13).



Ceramic Resonator or Crystal	LC	RC	External Clock
C1, C2 = 47 pf TYP *	C1, C2 = 22 pf	@ 5V VCC (TYP)	
F = 8 MHz	L = 130 uH *	C1 = 33 pf *	
	F = 3 MHz *	R = 1K *	
		F = 9.5 MHz *	

* Preliminary Value Including Pin Parasitics

Figure 13. Oscillator Configuration

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR timer allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power-fail to Power-OK status
2. Stop-Mode Recovery (if D5 of SMR=1)
3. WDT time-out

The POR time is T_{POR}. Bit 5 of the STOP mode register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, and RC/LC oscillators with fast start up time).

HALT. Turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupt IRQ0, IRQ1, IRQ2 and IRQ3, remain active. The device may be recovered by interrupts, either external or internal generated.

In order to enter STOP or HALT mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=FFH) immediately before the appropriate sleep instruction, i.e.:

```
FF  NOP   ; clear the pipeline
6F  STOP  ; enter STOP mode
          or
FF  NOP   ; clear the pipeline
7F  HALT  ; enter HALT mode
```

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current. The STOP mode is terminated by a RESET only, either by WDT time-out, POR; or SMR recovery. This causes the processor to restart the application program at address 000C (HEX).

Port Configuration Register (PCON). The Port Configuration Register (PCON) configures the ports individually: Comparator Output on Port 3, Open-Drain on Port 0, Low EMI Noise on Ports 0, 2, and 3, and Low EMI Noise Oscillator. The PCON Register is located in the Expanded Register File at bank F, location 00 (Figure 14).

Comparator Output Port 3 (D0). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34 and P37 and a 0 releases the Port to its standard I/O configuration.

Port 0 Open-Drain (D2). Port 0 is configured as an open-drain by resetting this bit (D2=0) and configured as Pull-up Active by setting D2 = 1. The default value is 1.

Low EMI Port 0 (D3). Port 0 is configured as a Low EMI Port by resetting this bit (D3=0) and configured as a Standard Port by setting D3=1. The default value is 1.

Low EMI Port 2 (D5). Port 2 is configured as a Low EMI Port by resetting this bit (D5=0) and configured as a Standard Port by setting D5=1. The default values is 1.

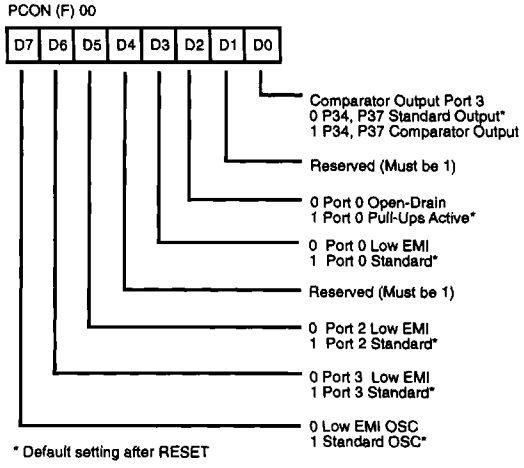


Figure 14. Port Configuration Register (Write Only)

Low EMI Port 3 (D6). Port 3 is configured as a Low EMI Port by resetting this bit (D6=0) and configured as a Standard Port by setting D6=1. The default values is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A 1 in this location configures the oscillator with standard drive, while a 0 configures the oscillator with low-noise drive, it does not affect the relationship of SCLK and XTAL.

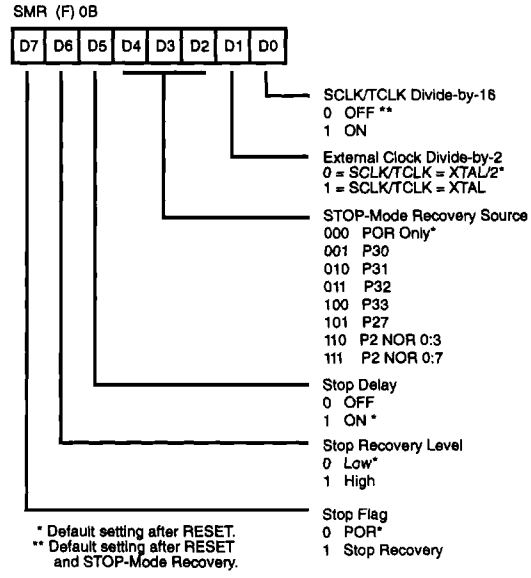


Figure 15. Stop-Mode Recovery Register (Write Only Except Bit D7 Which is Read Only)

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FUNCTIONAL DESCRIPTION (Continued)

STOP-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 15). All bits are Write Only, except Bit 7 which is a Read Only. Bit 7 is a flag bit that is hardware set on the condition of STOP Recovery and reset by a power- on cycle. Bit 6 controls whether a low level or high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR register specify the source of the STOP-Mode Recovery signal. Bits 0 and 1 determine the time-out period of the WDT (Table 7). The SMR is located in bank F of the Expanded Register Group at address OBH.

SCLK/TCLK Divide-by-16 Select (D0). D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (TCLK sources, counter/timers, and interrupt logic). The default setting after either a Reset or a Stop-Mode Recovery is 0.

External Clock Divide-by-2 (D1). This bit can eliminate the oscillator divide-by-2 circuitry. When this bit is 0. SCLK (System Clock) and TCLK (Timer Clock) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1 = 1). Using this bit, together with D7 of PCON, further helps lower EMI [i.e., D7 (PCON) = 0, D1 (SMR) = 1]. The default setting is 0.

STOP-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR specify the wake-up source of the STOP-Mode Recovery (Figure 16).

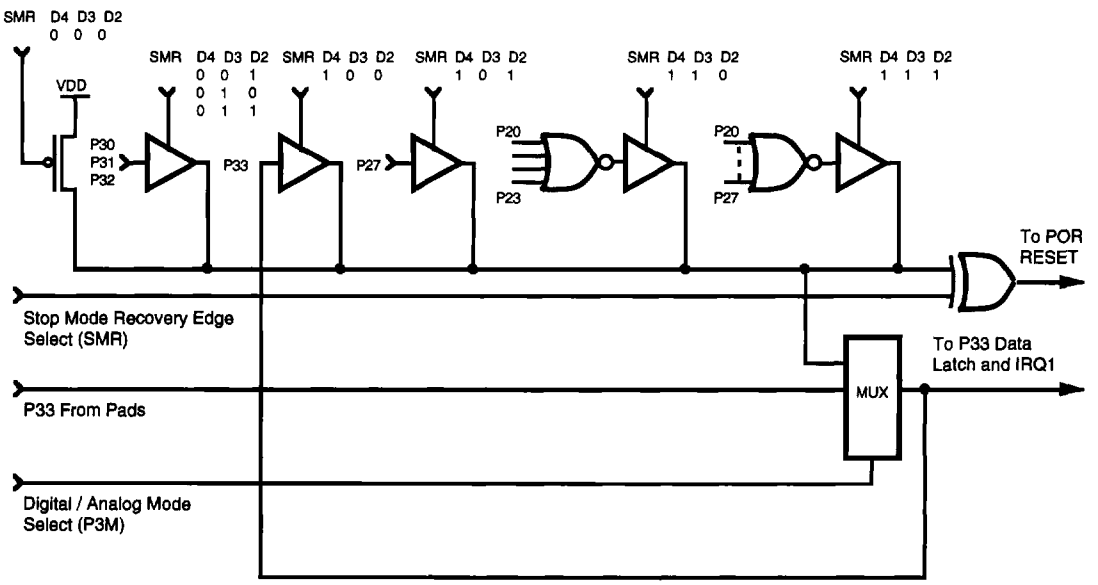

Figure 16. STOP-Mode Recovery Source

Table 6. STOP-Mode Recovery Source

SMR D4	SMR D3	SMR D2	Operation Description of action
0	0	0	POR recovery only
0	0	1	P30 transition
0	1	0	P31 transition (Not in Analog Mode.)
0	1	1	P32 transition (Not in Analog Mode.)
1	0	0	P33 transition (Not in Analog Mode.)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2, bits 0-3
1	1	1	Logical NOR of Port 2, bits 0-7

STOP-Mode Recovery Delay Select (D5). This bit disables the 5 ms RESET delay after STOP-Mode Recovery. The default condition of this bit is 1. If the "fast" wake up is selected, the STOP-Mode Recovery source needs to be kept active for at least 5 TpC.

STOP-Mode Recovery Level Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the Z86C30/C31 from STOP mode. A 0 indicates low level recovery. The default is 0 on POR (Figure 16).

Cold or Warm Start (D7). This bit is set by the device upon entering STOP mode. A 0 in this bit (cold) indicates that the device was reset by POR RESET. A 1 in this bit (warm) indicates that the device awakens by a SMR source.

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that will reset the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT cannot be disabled after it has been initially enabled. The WDT circuit is driven by an on-board RC oscillator or external oscillator from XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register.

Note: Execution of the WDT instruction affects the Z (zero), S (sign), V (overflow) flags.

WDT Time Select (D0, D1). Bits 0 and 1 control a tap circuit that determines the time-out period. Table 6 shows the different values that can be obtained. The default value of D0 and D1 are 1 and 0, respectively.

Table 7. Time-out Period of the WDT

D1	D0	Time-out of Internal RC OSC	Time-out of XTAL clock
0	0	5 ms min	256 TpC
0	1	15 ms min	512 TpC
1	0	25 ms min	1024 TpC
1	1	100 ms min	4096 TpC

Notes:
TpC = XTAL clock cycle
The default on reset is 15 ms.
The values given are for V_{CC} = 5.0V

WDT During HALT (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1.

WDT During STOP (D3). This bit determines whether or not the WDT is active during STOP mode. A 1 indicates active during STOP. A 0 will disable the WDT during STOP mode. Since the on-board OSC is stopped during STOP mode, the WDT clock source has to select the on-board RC OSC for the WDT to recover from STOP mode. The default is 1.

Clock Source for WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator.

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FUNCTIONAL DESCRIPTION (Continued)

WDTMR Register Accessibility. The WDTMR register (Figure 17) is accessible only during the first 64 system clock cycles from the execution of the first instruction after Power-On Reset, Watch-Dog Timer reset or a STOP-Mode Recovery. After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register Group at address location 0FH (Figure 18).

Note: The WDT can be permanently enabled through a mask programming option on the Z86C30/C31. This option is selected by the customer at the time of ROM code submittal. In this mode, WDT is always activated when the device comes out of reset. Execution of the WDT instruction serves to refresh the WDT time-out period. WDT operation in the HALT and STOP modes is controlled by WDTMR programming. If this mask option is not selected at the time of ROM code submission, the WDT must be activated by the user through the WDT instruction and is always disabled by any reset to the device.

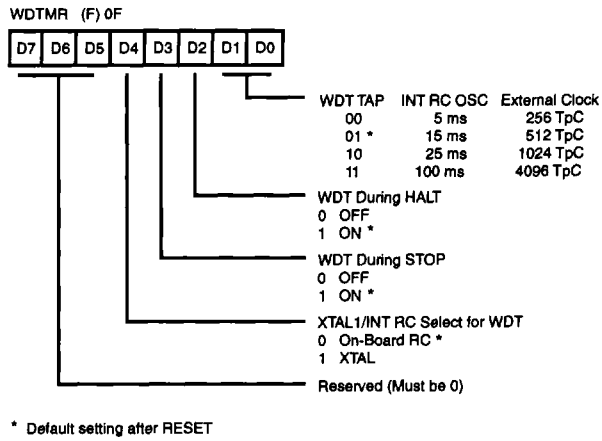

Figure 17. Watch-Dog Timer Mode Register (Write Only)

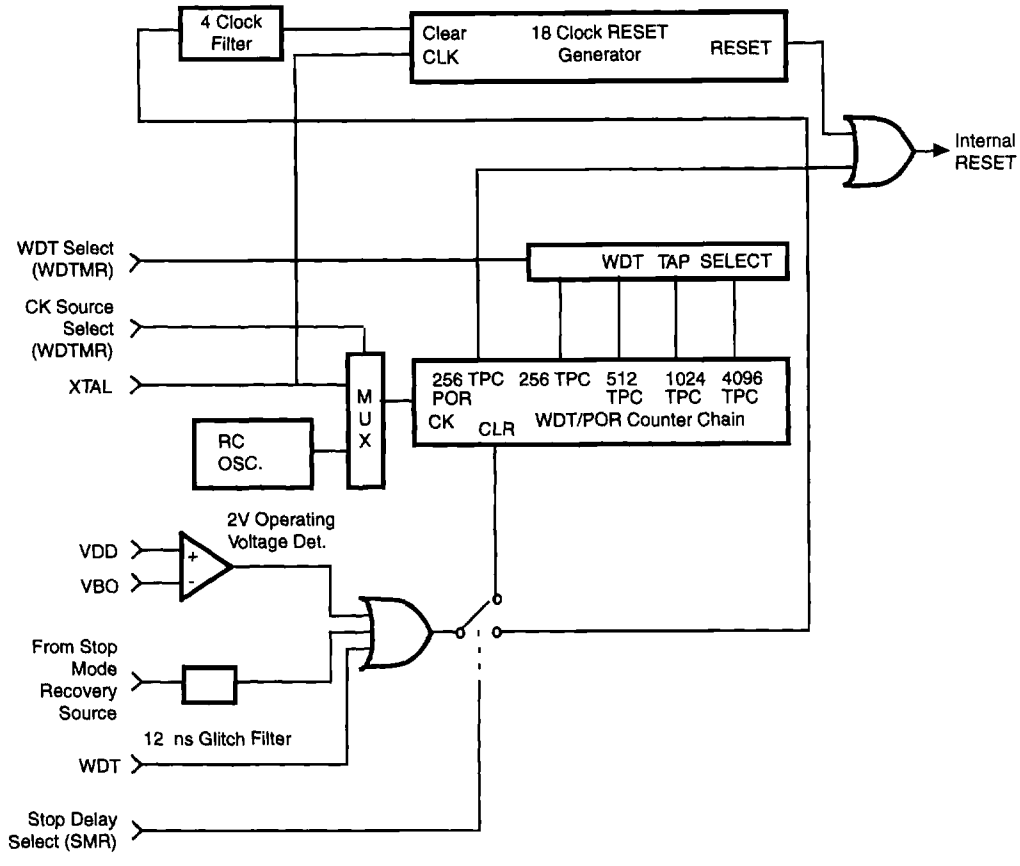

Figure 18. Resets and WDT

FUNCTIONAL DESCRIPTION (Continued)

Low Voltage Protection. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below the referenced Low Voltage Protection trip point voltage. The minimum operating voltage for functionality varies with temperature and operating frequency, while the Low Voltage Protection trip point voltage (V_{LV}) varies with temperature only.

The Low Voltage Protection trip voltage (V_{LV}) is less than 3 volts and above 1.4 volts under the following conditions.

Maximum (V_{VL}) Conditions:

Case 1: T_A = -40°C to +105°C, Internal Clock (SCLK) Frequency equal or less than 1 MHz

Case 2: T_A = -40°C to +85°C, Internal Clock (SCLK) Frequency equal to or less than 2 MHz

Note: The internal clock frequency (SCLK) is determined by SMR (F) 0B bit D1.

The Z86C30/C31 functions normally at or above 3.0V under all conditions. Below 3.0V, the devices are guaranteed to function normally until the Low Voltage Protection trip point (V_{LV}) is reached for the temperatures and operating frequencies in Case 1 and Case 2 above. The actual Low Voltage Protection trip point is a function of temperature and process parameters (Figure 19).

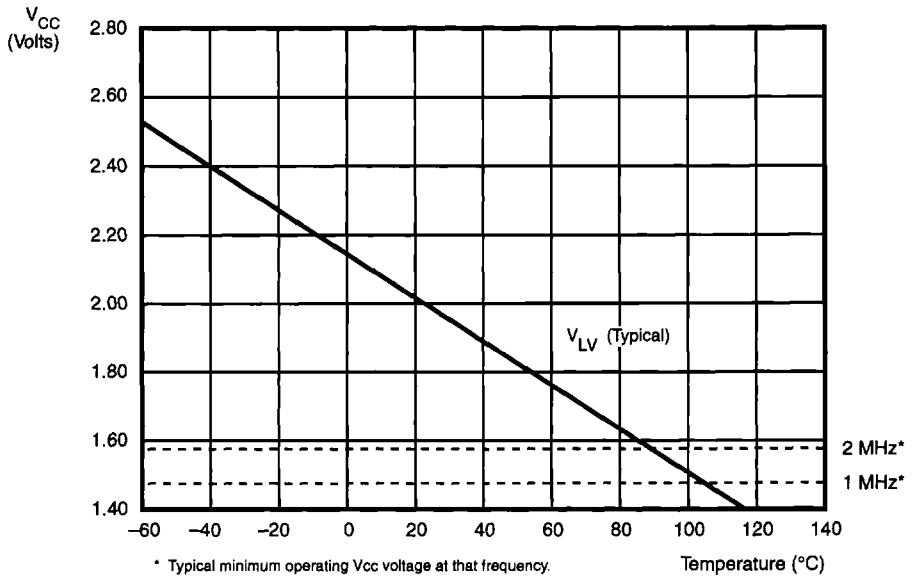

Figure 19. Typical Z86C30/C31 V_{LV} Voltage vs Temperature

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Ambient Temperature under Bias	–40	+105	C
Storage Temperature	–65	+150	C
Voltage on any Pin with Respect to V_{SS} [Note 1]	–0.6	+7	V
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V
Voltage on XTAL1 and /RESET Pins with Respect to V_{SS} [Note 2]	–0.6	V_{DD}+1	V
Total Power Dissipation		770	mW
Maximum Current out of V_{SS}		140	mA
Maximum Current into V_{DD}		125	mA
Maximum Current into an Input Pin [Note 3]	–600	+600	µA
Maximum Current into an Open-Drain Pin [Note 4]	–600	+600	µA
Maximum Output Current Sinked by Any I/O Pin		25	mA
Maximum Output Current Sourced by Any I/O Pin		25	mA

Notes:
[1] This applies to all pins except XTAL pins and where otherwise noted.
[2] There is no input protection diode from pin to V_{DD}.
[3] This excludes XTAL pins.
[4] Device pin is not at an output Low state.

Notice:
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. Total power dissipation should not exceed 770 mW for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [\, I_{DD} - (\text{sum of } I_{OH}) \,] + \text{sum of } [\, (V_{DD} - V_{OH}) \times I_{OH} \,] + \text{sum of } (V_{OL} \times I_{OL})$$

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 20).

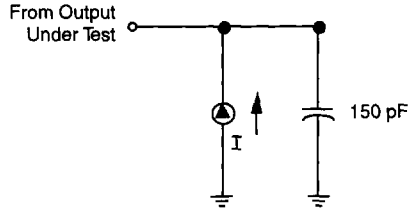

Figure 20. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

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DC ELECTRICAL CHARACTERISTICS
Z86C30/C31

Sym	Parameter	V_{CC} Note[3]	T_A =0°C to +70°C / T_A = −40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	3.0V	0.7 V_{CC}	V_{CC} +0.3	1.3	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC} +0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.0V	GND −0.3	0.2 V_{CC}	0.7	V	Driven by External Clock Generator	
		5.5V	GND −0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.3V	0.7 V_{CC}	V_{CC} +0.3	1.3	V		
		5.0V	0.7 V_{CC}	V_{CC} +0.3	2.5	V		
V_{IL}	Input Low Voltage	3.0V	GND−0.3	0.2 V_{CC}	0.7	V		
		5.5V	GND −0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	3.0V	V_{CC} −0.4		3.1	V	I_{OH} = −0.5 mA	
	(Low EMI Mode)	5.5V	V_{CC} −0.4		4.8	V	I_{OH} = −0.5 mA	
V_{OH1}	Output High Voltage	3.0V	V_{CC} −0.4		3.1	V	I_{OH} = −2.0 mA	[8]
		5.5V	V_{CC} −0.4		4.8	V	I_{OH} =−2.0 mA	[8]
V_{OL}	Output Low Voltage	3.0V		0.6	1.3	V	I_{OL} = 1.0 mA	
	(Low EMI Mode)	5.5V		0.4	2.5	V	I_{OL} = 1.0 mA	
V_{OL1}	Output Low Voltage	3.0V		0.6	0.2	V	I_{OH} = +4.0 mA	[8]
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	[8]
V_{OL2}	Output Low Voltage	3.0V		1.2	0.3	V	I_{OL} = +6 mA, 3 Pin Max	[8]
		5.5V		1.2	0.3	V	I_{OL} = +12 mA, 3 Pin Max	[8]
V_{RH}	Reset Input High Voltage	3.0V	0.8 V_{CC}	V_{CC}	1.5	V		
		5.5V	0.8 V_{CC}	V_{CC}	2.1	V		
V_{RI}	Reset Input Low Voltage	3.3V	GND−0.3	0.2 V_{CC}	1.1			
		5.0V	GND −0.3	0.2 V_{CC}	1.7			
V_{OFFSET}	Comparator Input Offset	3.0V		25	10	mV		
	Voltage	5.5V		25	10	mV		
V_{ICR}	Input Common Mode	3.0V	0	V_{CC} −1.5V		V		[10]
	Voltage Range	5.5V	0	V_{CC} −1.5V		V		[10]
		3.0	0	V_{CC} −1.0V		V		[13]
		5.5	0	V_{CC} −1.0V		V		[13]
I_{IL}	Input Leakage	3.0V	−1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.0V	−1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.0V	−1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.5V	−1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.0V		−130	−60	µA		
		5.5V		−180	−80	µA		
I_{CC}	Supply Current	3.0V		10	4	mA	@ 8 MHz	[4,5]
		5.5V		15	10	mA	@ 8 MHz	[4,5,15]
		3.0V		15	5	mA	@ 12 MHz	[4,5,15]
		5.5V		20	15	mA	@ 12 MHz	[4,5]

Sym	Parameter	V_{CC} Note[3]	T_A=0°C to +70°C Min	Max	T_A=-40°C to +105°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current	3.0V		3		3	1	mA	HALT mode V_{IN} = 0V, V_{CC} @ 8 MHz	[4,5]
		5.5V		5		5	2.4	mA	HALT mode V_{IN} = 0V, V_{CC} @ 8 MHz	[4,5]
		3.0V		4		4	1.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 12 MHz	[4,5,15]
		5.5V		6		6	3.2	mA	HALT mode V_{IN} = 0V, V_{CC} @ 12 MHz	[4,5,15]
		3.0V		2		2	0.8	mA	Clock Divide by 16 @ 8 MHz	[4,5]
		5.5V		4		4	1.8	mA	Clock Divide by 16 @ 8 MHz	[4,5]
		3.0V		3		3	1.2	mA	Clock Divide by 16 @ 12 MHz	[4,5,15]
		5.5V		5		5	2.5	mA	Clock Divide by 16 @ 12 MHz	[4,5,15]
I_{CC2}	Standby Current	3.0V		8		15	1	µA	STOP mode VIN = 0V, V_{CC} WDT is not Running	[6,11]
		5.5V		10		20	2	µA	STOP mode VIN = 0V, V_{CC} WDT is not Running	[6,11]
		3.0V		500		600	310	µA	STOP mode VIN = 0V, V_{CC} WDT is Running	[6,11]
		5.5V		800		1000	600	µA	STOP mode VIN = 0V, V_{CC} WDT is Running	[6,11]
I_{ALL}	Auto Latch Low Current	3.0V		8		25	16	µA	$0V < V_{IN} < V_{CC}$	[9]
		5.5V		15		42	23	µA	$0V < V_{IN} < V_{CC}$	[9]
I_{ALH}	Auto Latch High Current	3.0V		-5		-18	-13	µA	$0V < V_{IN} < V_{CC}$	[9]
		5.5V		-8		-26	-17	µA	$0V < V_{IN} < V_{CC}$	[9]
T_{POR}	Power-On Reset	3.0V	7	24	7	25	8.5	ms		
		5.5V	3	13	3	14	5	ms		
V_{LV}	V_{CC} Low Voltage Protection Voltage		1.5	2.8	1.5	3.0	2.1	V	2 MHz max Int. CLK Freq.	[7]

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Freq
Clock Driven	0.3 mA	5	mA	8 MHz
Crystal or Resonator	24 mA	5	mA	8 MHz

[2] GND=0V.

[3] The V_{CC} voltage specification of 3.0 guarantees 3.3V ±0.3 V and the V_{CC} voltage specification of 5.5 V guarantees 5.0 V ±0.5 V.

[4] All outputs unloaded, I/O pins floating, inputs at rail.

[5] CL1 = CL2 = 100 pF

[6] Same as note [4] except inputs at V_{CC}.

[7] The V_{LV} increases as the temperature decreases.

[8] Standard Mode (not Low EMI Mode)

[9] Auto Latch (mask option) selected

[10] For analog comparator inputs when analog comparators are enabled.

[11] Clock must be forced Low, when XTAL1 is clock-driven and XTAL2 is floating.

[12] Excludes clock pins.

[13] Temperature is 0° to +70°C.

[14] Auto Latch Delete option is not selected.

[15] Z86C30 only.

AC ELECTRICAL CHARACTERISTICS
Additional Timing Diagram

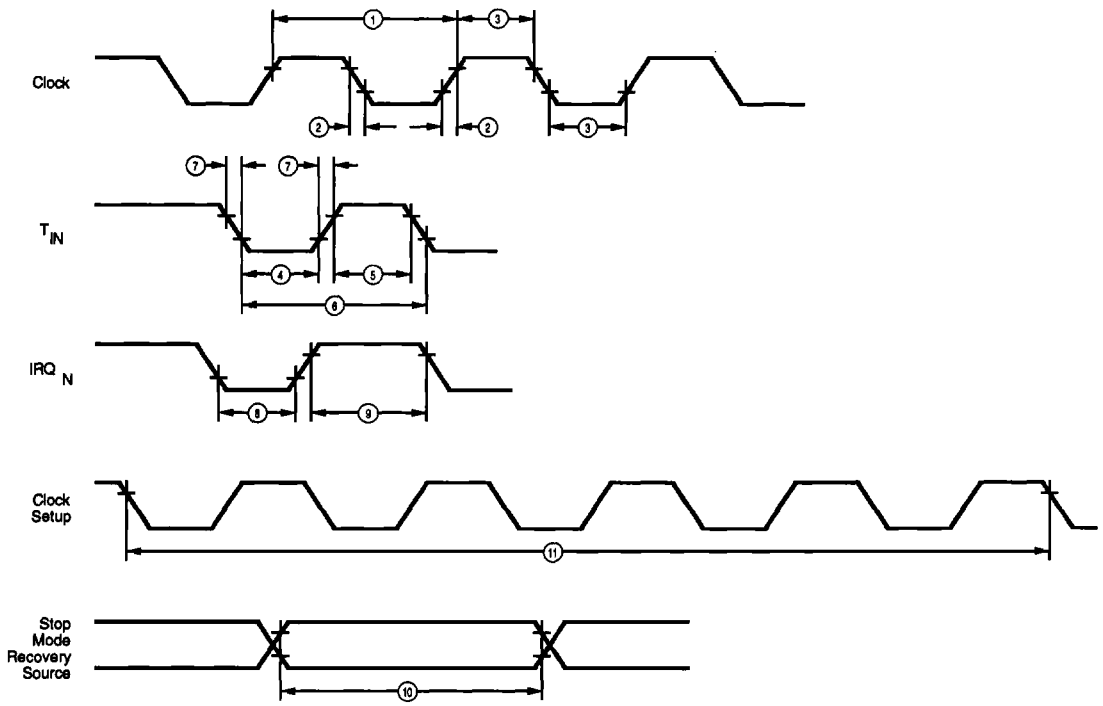

Figure 21. Additional Timing

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (For SCLK/TCLK = XTAL/2)

No	Sym	Parameter	V_{CC} Note[6]	T_A = 0°C to +70°C 8 MHz (C31) Min	Max	T_A = –40°C to +105°C 12 MHz (C30) Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	125	DC	83	DC	ns	[1,7,8]
			5.5V	125	DC	83	DC	ns	[1,7,8]
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V	25		15		ns	[1,7,8]
			5.5V	25		15		ns	[1,7,8]
3	TwC	Input Clock Width	3.0V	62.5		62.5		ns	[1,7,8]
			5.5V	62.5		62.5		ns	[1,7,8]
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	[1,7,8]
			5.5V	70		70		ns	[1,7,8]
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC			[1,7,8]
			5.5V	5TpC		5TpC			[1,7,8]
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC			[1,7,8]
			5.5V	8TpC		8TpC			[1,7,8]
7	TrTin, TfTin	Timer Input Rise and Fall Timer	3.0V		100		100	ns	[1,7,8]
			5.5V		100		100	ns	[1,7,8]
8A	TwIL	Int. Request Low Time	3.0V	100		100		ns	[1,2,7,8]
			5.5V	70		70		ns	[1,2,7,8]
8B	TwIL	Int. Request Low Time	3.0V	5TpC		5TpC			[1,3,7,8]
			5.5V	5TpC		5TpC			[1,3,7,8]
9	TwIH	Int. Request Input High Time	3.0V	5TpC		5TpC			[1,2,7,8]
			5.5V	5TpC		5TpC			[1,2,7,8]
10	Twsm	Stop-Mode Recovery Width Spec	3.0V	12		12		ns	[4,8]
			5.5V	12		12		ns	[4,8]
11	Tost	Oscillator Start-up Time	3.0V		5TpC		5TpC		[4,9]
			5.5V		5TpC		5TpC		[4,9]
12	Twdt	Watch-Dog Timer Delay Time	3.0V	6.0		6.0		ms	D0=0[5,11]
			5.5V	3.0		3.0		ms	D1=0 [5,11]
			3.0V	20		20		ms	D0=1 [5,11]
			5.5V	10		10		ms	D1=0 [5,11]
			3.0V	33		33		ms	D0=0 [5,11]
			5.5V	16		16		ms	D1=1 [5,11]
			3.0V	132		132		ms	D0=1 [5,11]
			5.5V	66		66		ms	D1=1[5,11]

Notes:

[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P30)
[3] Interrupt request through Port 3 (P30).
[4] SMR-D5 = 1, POR STOP mode delay is on.
[5] Reg. WDTMR.
[6] The V_{CC} voltage specification of 3.0 guarantees 3.3V ±0.3V and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
[7] SMR D1=0.
[8] Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-1 mode.
[9] For RC and LC oscillator, and for oscillator driven by clock driver.
[10] Standard mode (not Low EMI output ports).
[11] Using internal RC
[12] Z86C31 max. freq. = 8 MHz; Z86C30 max. freq. = 12 MHz.

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AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (Divide-By-One Mode)

No	Symbol	Parameter	V_{CC} Note [6]	T_A = 0°C to +70°C 4 MHz Min	Max	T_A = -40°C to +105°C 4 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	3.0V	250	DC	250	DC	ns	[1,7,8]
			5.5V	250	DC	250	DC	ns	[1,7,8]
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		25	ns	[1,7,8]
			5.5V		25		25	ns	[1,7,8]
3	TwC	Input Clock Width	3.0V	100		100		ns	[1,7,8]
			5.5V	100		100		ns	[1,7,8]
4	TwTinL	Timer Input Low Width	3.0V	100		100		ns	[1,7,8]
			5.5V	70		70		ns	[1,7,8]
5	TwTinH	Timer Input High Width	3.0V	3TpC		3TpC			[1,7,8]
			5.5V	3TpC		3TpC			[1,7,8]
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC			[1,7,8]
			5.5V	4TpC		4TpC			[1,7,8]
7	TrTin,	Timer Input Rise and Fall Timer	3.0V		100		100	ns	[1,7,8]
	TfTin		5.5V		100		100	ns	[1,7,8]
8A	TwIL	Int. Request Low Time	3.0V	100		100		ns	[1,2,7,8]
			5.5V	70		70		ns	[1,2,7,8]
8B	TwIL	Int. Request Low Time	3.0V	3TpC		3TpC			[1,3,7,8]
			5.5V	3TpC		3TpC			[1,3,7,8]
9	TwIH	Int. Request Input High Time	3.0V	3TpC		3TpC			[1,2,7,8]
			5.5V	3TpC		2TpC			[1,2,7,8]
10	Twsm	STOP-Mode Recovery Width Spec	3.0V	12		12		ns	[4,8]
			5.5V	12		12		ns	[4,8]
11	Tost	Oscillator Startup Time	3.0V		5TpC		5TpC		[4,8,9]
			5.5V		5TpC		5TpC		[4,8,9]

Notes:

[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

[2] Interrupt request via Port 3 (P33-P31).

[3] Interrupt request via Port 3 (P30).

[4] SMR-D5 = 1, POR STOP mode delay is on.

[5] Reg. WDTMR.

[6] The V_{CC} voltage specification of 3.0 guarantees 3.3V ±0.3V and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.

[7] SMR D1 = 0.

[8] Maximum frequency for internal system clock is 4 MHz when using XTAL divide-by-1 mode.

[9] For RC and LC oscillator, and for oscillator driven by clock driver.

AC ELECTRICAL CHARACTERISTICS
Handshake Timing Table

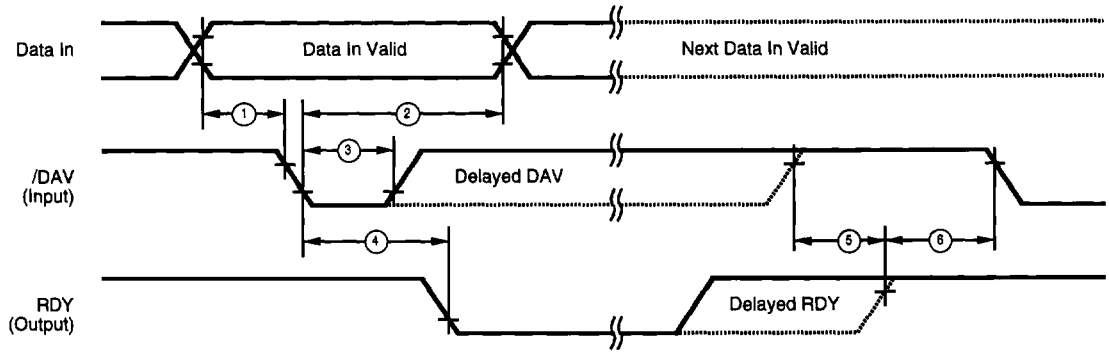

Figure 22. Input Handshake Timing

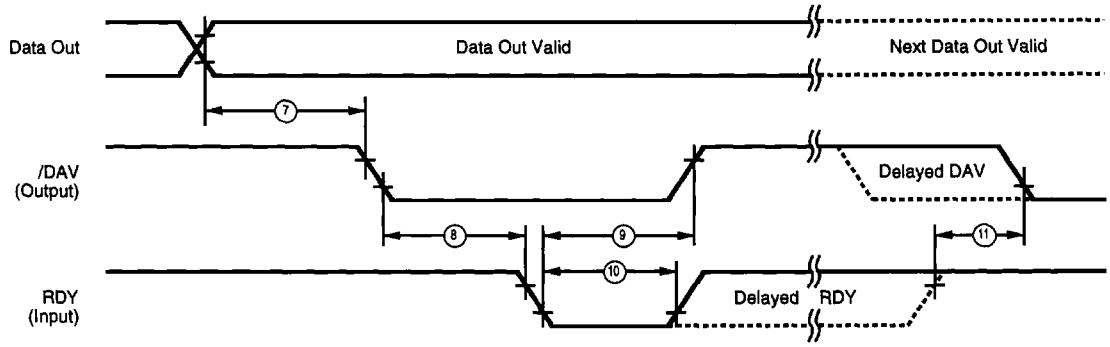

Figure 23. Output Handshake Timing

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AC ELECTRICAL CHARACTERISTICS (Continued)
Handshake Timing Table

No	Sym	Parameter	V_{CC} Note[1]	T_A =0°C to +70°C 8 MHz (C31) Min	Max	T_A = –40°C to +105°C 12 MHz (C30) Min	Max	Data Direction	Notes
1	TsDI(DAV)	Data In Setup Time	3.0V	0		0		IN	[2]
			5.5V	0		0		IN	[2]
2	ThDI(DAV)	Data In Hold Time	3.0V	160		160		IN	[2]
			5.5V	115		115		IN	[2]
3	TwDAV	Data Available Width	3.0V	155		155		IN	[2]
			5.5V	110		110		IN	[2]
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	3.0V		160		160	IN	[2]
			5.5V		115		115	IN	[2]
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay	3.0V		120		120	IN	[2]
			5.5V		80		80	IN	[2]
6	RDY0d(DAV)	RDY Rise to DAV Fall Delay	3.0V	0		0		IN	[2]
			5.5V	0		0		IN	[2]
7	TdDO(DAV)	Data Out to DAV Fall Delay	3.0V	63		42		OUT	[2]
			5.5V	63		42		OUT	[2]
8	TdDAV0(RDY)	DAV Fall to RDY Fall Delay	3.0V	0		0		OUT	[2]
			5.5V	0		0		OUT	[2]
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	3.0V		160		160	OUT	[2]
			5.5V		115		115	OUT	[2]
10	TwRDY	RDY Width	3.0V	110		110		OUT	[2]
			5.5V	80			80	OUT	[2]
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	3.0V		110		110	OUT	[2]
			5.5V		80		80	OUT	[2]

Notes:
[1] The V_{CC} voltage specification of 3.0 guarantees 3.3V ±0.3V and the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
[2] Standard Mode (not Low EMI mode on output ports).
[3] Z86C31 max. freq. = 8 MHz; Z86C30 max. freq. = 12 MHz.

EXPANDED REGISTER FILE CONTROL REGISTERS

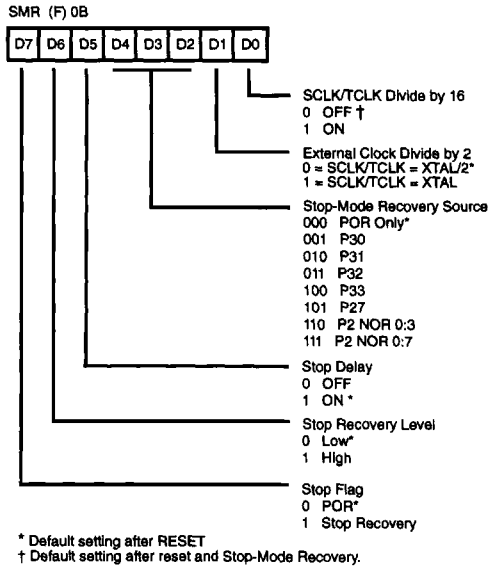

Figure 24. Stop-Mode Recovery Register (Write only Except Bit D7 Which is Read Only)

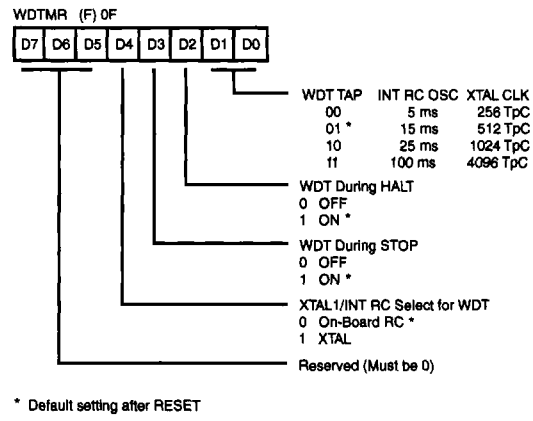

Figure 25. Watch-Dog Timer Mode Register (Write Only)

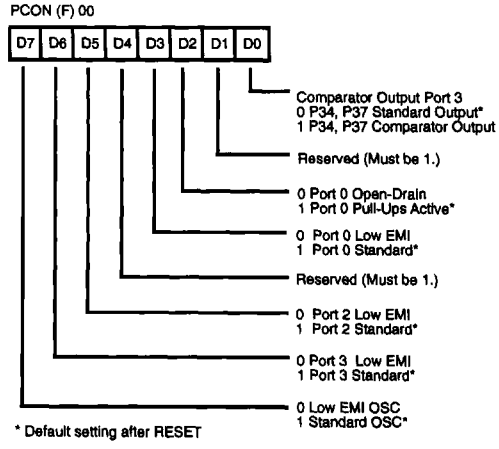

Figure 26. Port Configuration Register (Write Only)

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Z8® CONTROL REGISTER DIAGRAMS

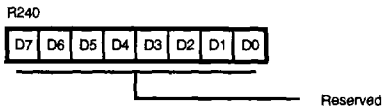

Figure 27. Reserved

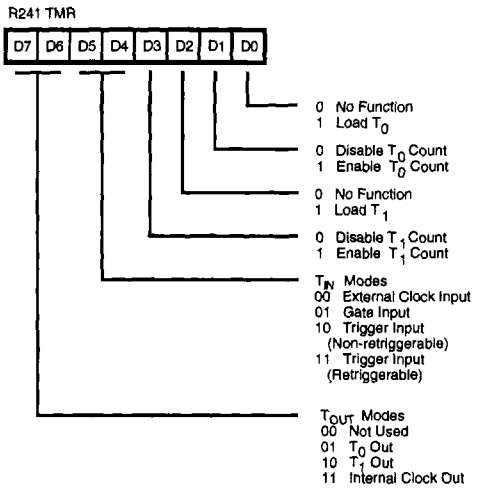

Figure 28. Timer Mode Register ($F1_H$: Read/Write)

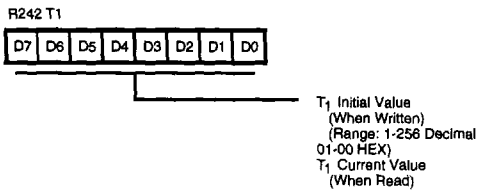

Figure 29. Counter Timer 1 Register ($F2_H$: Read/Write)

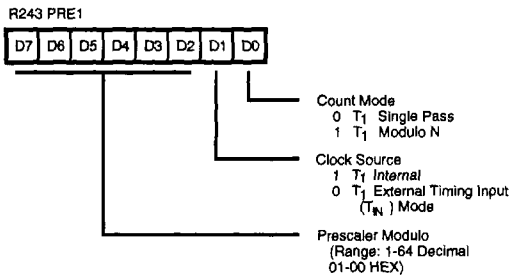

Figure 30. Prescaler 1 Register ($F3_H$: Write Only)

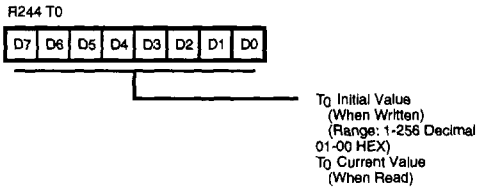

Figure 31. Counter/Timer 0 Register ($F4_H$: Read/Write)

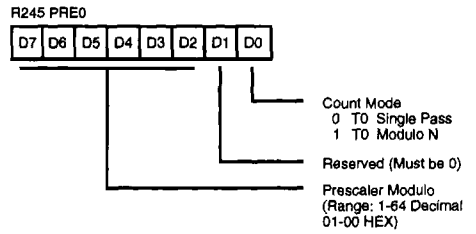

Figure 32. Prescaler 0 Register ($F5_H$: Write Only)

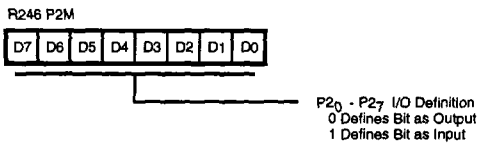

Figure 33. Port 2 Mode Register ($F6_H$: Write Only)

Z8® CONTROL REGISTER DIAGRAMS (Continued)

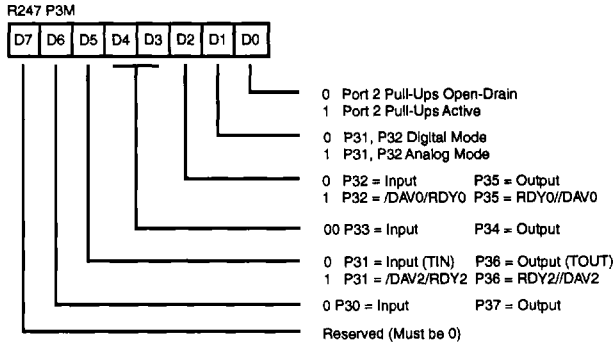

Figure 34. Port 3 Mode Register ($F7_H$: Write Only)

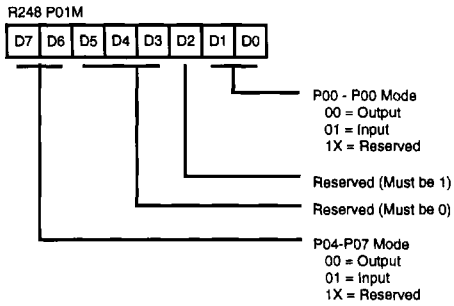

Figure 35. Port 0 and 1 Mode Register ($F8_H$: Write Only)

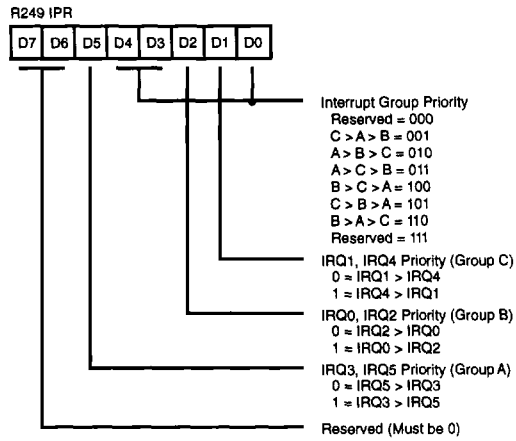

Figure 36. Interrupt Priority Register ($F9_H$: Write Only)

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Z8® CONTROL REGISTER DIAGRAMS (Continued)

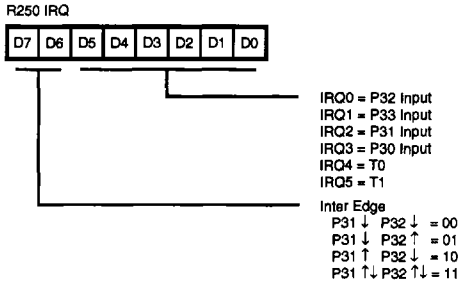

Figure 37. Interrupt Request Register (FA_H: Read/Write)

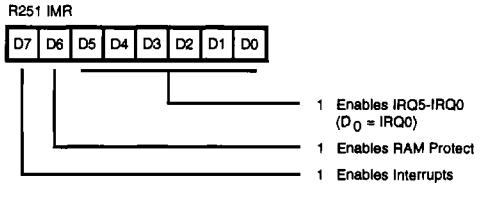

Figure 38. Interrupt Mask Register (FB_H: Read/Write)

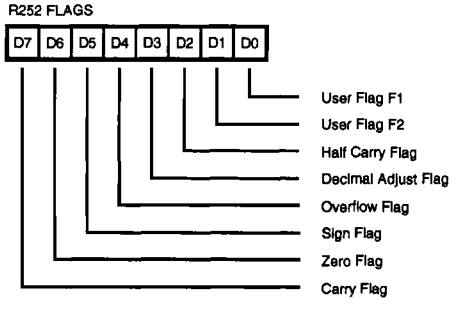

Figure 39. Flag Register (FC_H: Read/Write)

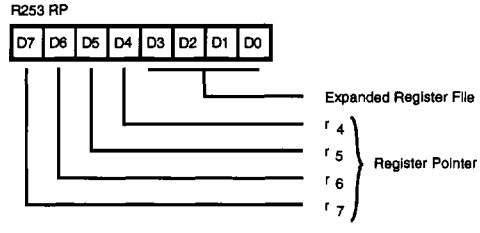

Figure 40. Register Pointer (FD_H: Read/Write)

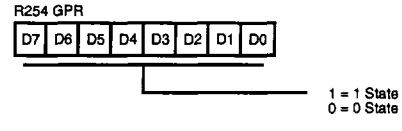

Figure 41. General-Purpose Register

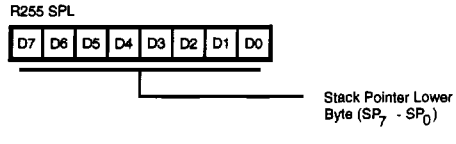

Figure 42. Stack Pointer (FF_H: Read/Write)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

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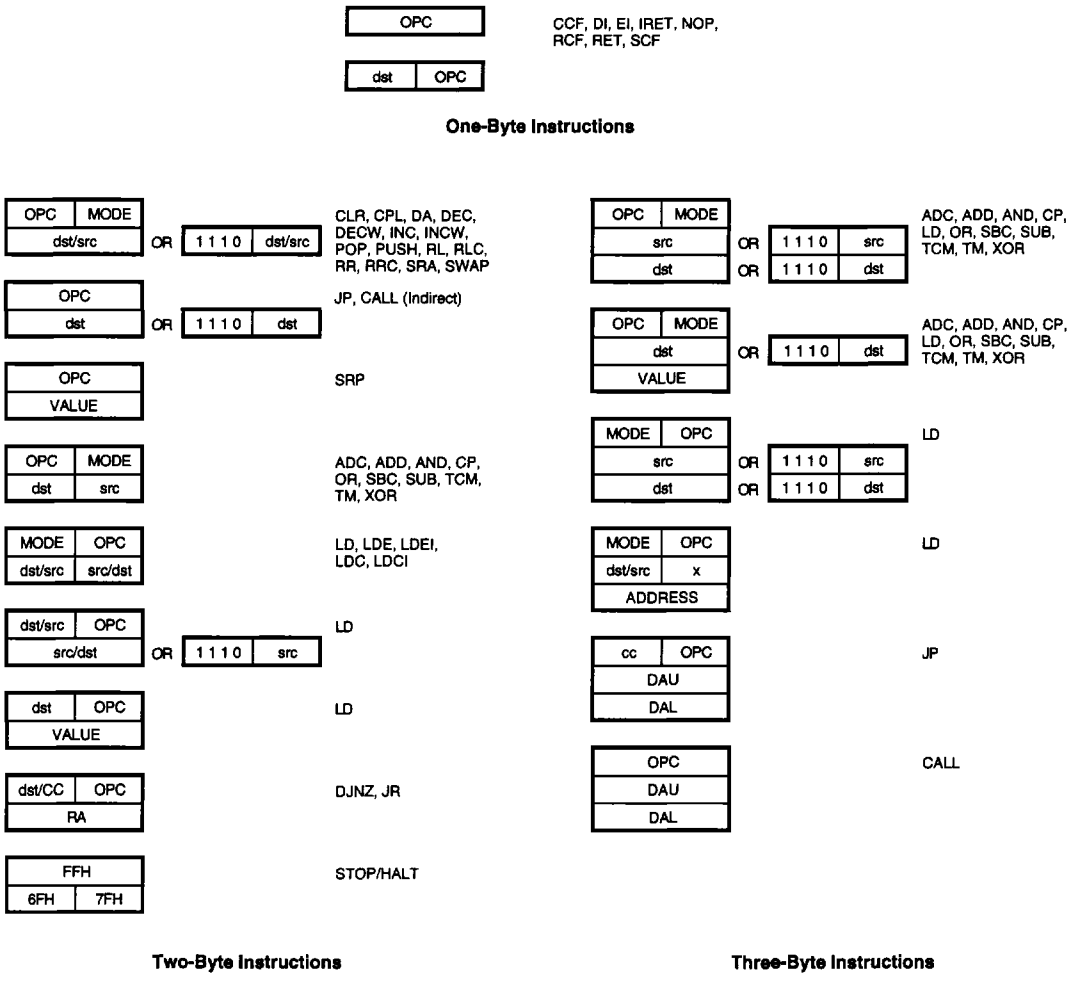
CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	

INSTRUCTION FORMATS



INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location.

The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

refers to bit 7 of the destination operand.

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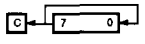
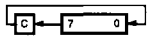
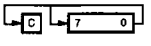
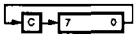
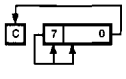
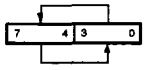
INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst←dst + src +C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP - 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst - src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst - 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst - 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r - 1 if r ≠ 0 PC←PC + dst Range: +127, -128	RA		rA r = 0 - F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
INC dst dst←dst + 1	r R IR		rE r = 0 - F 20 21	-	*	*	*	-	-
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true PC←dst	DA IRR		cD c = 0 - F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, -128	RA		cB c = 0 - F	-	-	-	-	-	-
LD dst, src dst←src	r r R r X r Ir R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 - F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r +1; rr←rr + 1	Ir	Irr	C3	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
NOP			FF	-	-	-	-	-	-
OR dst, src dst←dst OR src	†		4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP - 1; @SP←src		R IR	70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-
RL dst 	R IR		90 91	*	*	*	*	-	-
RLC dst 	R IR		10 11	*	*	*	*	-	-
RR dst 	R IR		E0 E1	*	*	*	*	-	-
RRC dst 	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dstf←dst – src – C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst 	R IR		D0 D1	*	*	*	0	-	-
SRP src RP←src		Im	31	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
STOP			6F	-	-	-	-	-	-
SUB dst, src dst←dst–src	†		2[ ]	*	*	*	*	1	*
SWAP dst 	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
XOR dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-
WDT			5F	-	X	X	X	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	Address Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

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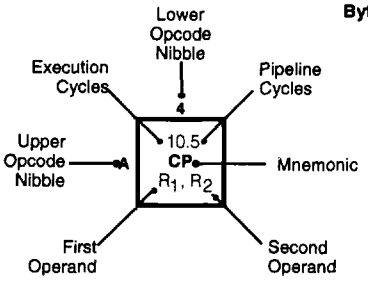
OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1														6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1														6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1			20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2			3					2					3	1	



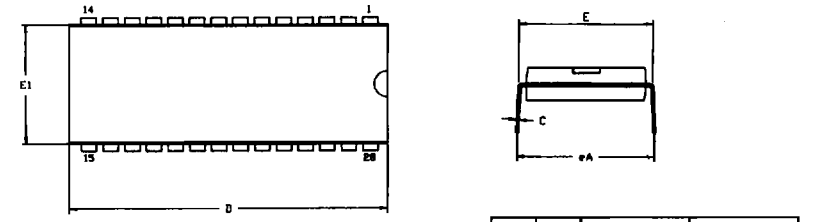
Legend:
R = 8-bit address
r = 4-bit address
R1 or r1 = Dst address
R2 or r2 = Src address

Sequence:
Opcode, First Operand, Second Operand

Note: The blanks are reserved.

* 2-byte instruction appears as a 3-byte instruction

PACKAGE INFORMATION

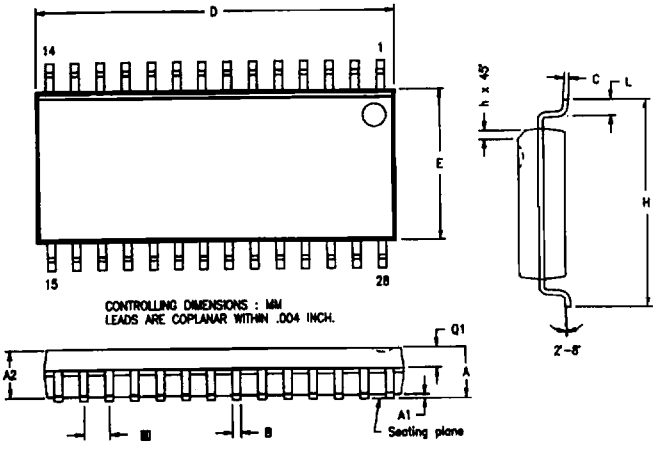


SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.51	0.81	.020	.032
A2		3.18	3.94	.125	.155
B		0.38	0.53	.015	.021
B1	01	1.52	1.78	.060	.070
	02	1.27	1.52	.050	.060
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
⊞		2.54 TYP		.100 TYP	
eA		15.49	16.51	.610	.650
L	-	3.18	3.81	.125	.150
Q1	01	1.52	1.91	.060	.075
	02	1.52	1.78	.060	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

CONTROLLING DIMENSIONS : INCH

28-Pin DIP Package Diagram

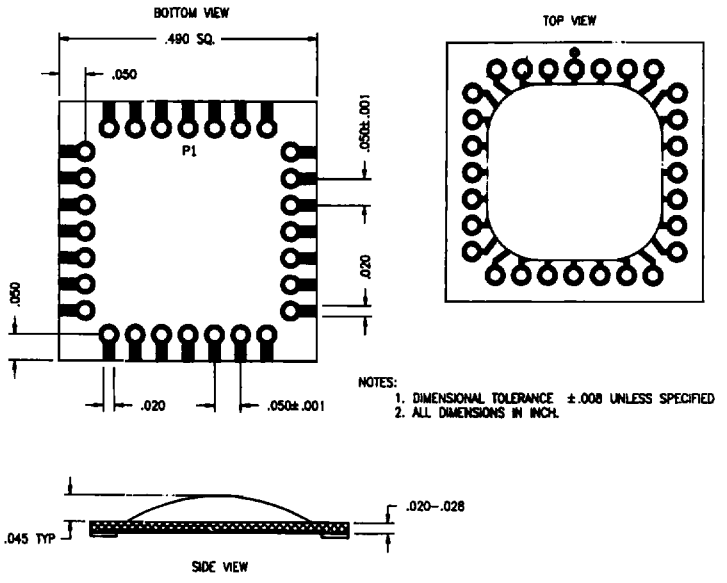


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
⊞	1.27 typ		.050 typ	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.81	1.00	.024	.039
Q1	0.97	1.07	.038	.042

28-Pin SOIC Package Diagram

7

PACKAGE INFORMATION (Continued)



28-Pin PCB Chip Carrier Package Diagram

ORDERING INFORMATION

Z86C30 (12 MHz)

Standard Temperature 28-Pin DIP	Extended Temperature 28-Pin DIP	Standard Temperature 28-Pin SOIC	Extended Temperature 28-Pin SOIC
Z86C3012PSC	Z86C3012PEC	Z86C3012SSC	Z86C3012SEC

Standard Temperature 28-Pin PCB Chip Carrier	Extended Temperature 28-Pin PCB Chip Carrier
Z86C3012TSC	Z86C3012TEC

Z86C31 (8 MHz)

Standard Temperature 28-Pin DIP	Extended Temperature 28-Pin DIP	Standard Temperature 28-Pin SOIC	Extended Temperature 28-Pin SOIC
Z86C3108PSC	Z86C3108PEC	Z86C3108SSC	Z86C3108SEC

Standard Temperature 28-Pin PCB Chip Carrier	Extended Temperature 28-Pin PCB Chip Carrier
Z86C3108TSC	Z86C3108TEC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

CODES

Preferred Package
P = Plastic DIP

Longer Lead Time
S = SOIC
T = PCB Chip Carrier

Preferred Temperature
S = 0° C to +70° C

Longer Lead Time
E = –40° C to +105° C

Speeds
08 = 8 MHz
12 = 12 MHz

Environmental
C = Plastic Standard

Example:

Z 86C30 12 P S C is a Z86C30, 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow