Dual Operational Amplifier Dual Comparator and Adjustable Voltage Reference

FTSM102A

OPERATIONAL AMPLIFIERS

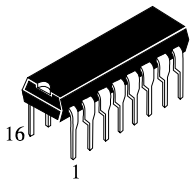
- LOW SUPPLY CURRENT : 200μA/amp.
- MEDIUM SPEED : 2.1MHz
- LOW LEVEL OUTPUT VOLTAGE CLOSE TO Vcc : 0.1V typ
- INPUT COMMON MODE VOLTAGE RANGE INCLUDES GROUND

COMPARATORS

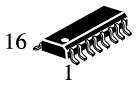
- LOW SUPPLY CURRENT : 200μA/amp. (Vcc = 5V)
- INPUT COMMON MODE VOLTAGE RANGE INCLUDES GROUND
- LOW OUTPUT SATURATION VOLTAGE : 250mB (Io = 4mA)

REFERENCE

- ADJUSTABLE OUTPUT VOLTAGE : Vref to 32V
- SINK CURRENT CAPABILITY : 1 to 100mA
- 1% and 0.4% VOLTAGE PRECISION
- LACTH-UP IMMUNITY



DIP-16
(Plastic Package



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ORDERING NUMBER:

FTSM102AN	Plastic Package
FTSM102AD	Plastic Micropac

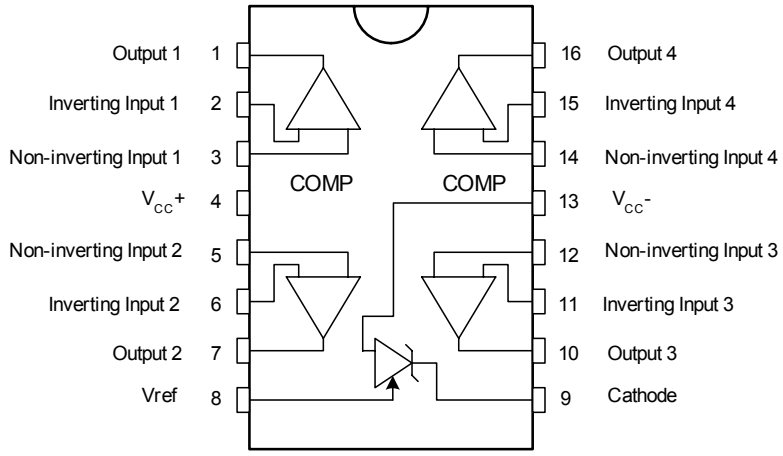
DESCRIPTION

The FTSM102A is a monolithic IC that includes two op-amps, two comparators and a precision voltage reference.This device is offering space and cost saving in many applications like power supply management or data acquisition systems.

ORDER CODES

Part number	Temperature Range	Package	
		N	D
FTSM102A	-40 ºC, +85ºC	•	•

PIN CONNECTIONS



Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
Vcc	Supply Voltage	36	V
V_{id}	Differential Input Voltage	36	V
V_i	Input Voltage	-0.3 to +36	V
Tj	Maximum Junction Temperature	150	ºC

Electrical Characteristics

Vcc^+ = 5V, Vcc^- = 0V, Tamb = 25°C (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
Icc	Total Supply Current Tmin < Tamb < Tmax		0.8	1.5 2	mA

OPERATIONAL AMPLIFIERS

Vcc^+ = 5 V, Vcc = GND, R1 connected to $V_{CC/2}$, Tamb = 25 ºC (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
V_{io}	Input Offset Voltage $T_{min} \le T_{amb} \le T_{max}$		1	4.5 6.5	mV
DV_{io}	Input Offset Voltage Drift		10		µV/ ºC
I_{ib}	Input Bias Current $T_{min.} \le T_{amb} \le T_{max}$		20	100 200	nA
I_{io}	Input Offset Current $T_{min.} \le T_{amb} \le T_{max}$		5	20 40	nA
Avd	Large Signal Voltage Gain Vcc = 30V, R1 = 10kΩ, V_o = 5V to 25V $T_{min.} \le T_{amb} \le T_{max}$	50 25	100		V/mV
SVR	Supply Voltage Rejection Ratio Vcc = 5V to 30V	80	100		dB
Vicm	Input Common Mode Voltage Range $T_{min.} \le T_{amb} \le T_{max}$	(Vcc^-) to (Vcc^+) -1.8 (Vcc^-) to (Vcc^+) -2.2			V
CMR	Common Mode Rejection Ratio Vcc^+ = 30V, Vicm = 0V to (Vcc^+) -1.8V	70	90		dB
I_{sc}	Output Short Circuit Current V_{id} = ±1V, Vo = 2.5V Source Sink	 3 3	 6 6		mA
V_{OH}	High Level Output Voltage Vcc^+ = 30V, R_L = 10k $T_{min.} \le T_{amb} \le T_{max}$	 27 26	 28		V
V_{OL}	Low Level Output Voltage R_L = 10kΩ $T_{min.} \le T_{amb} \le T_{max}$		100	150 210	mV
SR	Slew Rate Vcc = ±15V V_i = ±10V, R_L = 10kΩ, C_L = 100pF	1.6	2		V/ µs
GBP	Gain Bandwidth Product R_L = 10kΩ, C_L = 100pF, f = 100kHz	1.4	2.1		MHz
∅m	Phase Margin R_L = 10kΩ, C_L = 100pF		45		Degrees
THD	Total Harmonic Distortion		0.05		%
en	Equivalent Input Noise Voltage f = 1kHz		29		$\frac{nV}{\sqrt{Hz}}$
C_S	Channel Separation		120		dB

COMPARATORS

Vcc^+ = +5V, Vcc = Ground, Tamb = 25 ºC (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
V_{io}	Input Offset Voltage $T_{min} \le T_{amb} \le T_{max}$			5 9	mV
I_{io}	Input Offset Current $T_{min.} \le T_{amb} \le T_{max}$			50 150	nA
I_{ib}	Input Bias Current $T_{min.} \le T_{amb} \le T_{max}$			250 400	nA
I_{OH}	High Level Output Current Vid = 1V, Vcc = Vo = 30V $T_{min.} \le T_{amb} \le T_{max}$		0.1	 1	nA µA
V_{OL}	Low Level Output Voltage Vid = -1V, Isink = 4mA $T_{min.} \le T_{amb} \le T_{max}$		 250	 400 700	mV
Avd	Large Signal Voltage Gain Vcc = 15V, R1 = 15kΩ, V_o = 1V to 11V		 200		V/mV
I_{sink}	Output Current Sink V_{id} = -1V, Vo = 1.5V	6	16		mA
Vicm	Input Common Mode Voltage Range $T_{min.} \le T_{amb} \le T_{max}$	0 0		Vcc^+ -1.5 Vcc^+ -2	V
Vid	Differential Input Voltage			Vcc^+	V
t_{re}	Response Time – (note 1) R1 = 5.1kΩ to Vcc^+, Vref = 1.4V		1.3		µs
t_{rel}	Large Signal Response Time Vref = 1.4V, Vi =TTL, R1 = 5.1kΩ to Vcc^+		300		ns

Note 1 : The response time specified is for 100mV input step with 5mV overdrive.
For larger overdrive signals, 300ns can be obtained.

VOLTAGE REFERENCE

Symbol	Parameter	Value	Unit
V_{KA}	Cathode to Anode Voltage	Vref to 36	V
I_k	Cathode Current	1 to 100	mA

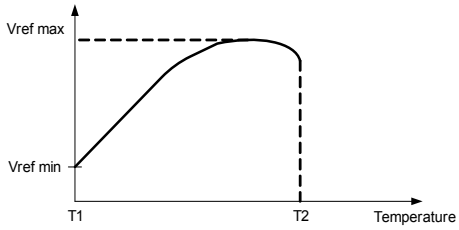
ELECTRICAL CHARACTERISTICS

Tamb = 25 ºC (unless otherwise specified)

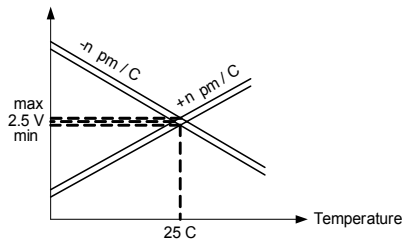
Symbol	Parameter	Min	Typ	Max	Unit
V_{ref}	Reference Input Voltage – (figure 1) - Tamb = 25 ºC V_{KA} = Vref, I_K = 10mA	2.490	2.500	2.510	V
ΔV_{ref}	Reference Input Voltage Deviation Over Temperature Range (figure 1, note 1) $V_{KA} = V_{ref}$, I_k = 10mA, $T_{min} \le T_{amb} \le T_{max}$		7	30	mV
$\frac{\Delta Vref}{\Delta T}$	Temperature Coefficient of Reference Input Voltage – (note 2) $V_{KA} = V_{ref}$, I_k = 10mA, $T_{min} \le T_{amb} \le T_{max}$		±22	±100	ppm/ºC
$\frac{\Delta Vref}{\Delta V_{KA}}$	Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage – (figure 2) I_K = 10mA, ΔV_{KA} = 36 to 3V		-1.1	-2	mV/V
I_{ref}	Reference Input Current – (figure 2) I_K = 10mA, R1 = 10kΩ, R2 = ∞ Tamb = 25 ºC $T_{min} \le T_{amb} \le T_{max}$		1.5	2.5 3	µA
ΔI_{ref}	Reference Input Current Deviation over Temperature Range – (figure 2) I_K = 10mA, R1 = 10kΩ, R2 = ∞ $T_{min} \le T_{amb} \le T_{max}$		0.5	1	µA
I_{min}	Minimum Cathode Current for Regulation – (figure 1) $V_{KA} = V_{ref}$		0.5	1	mA
I_{off}	Off-State Cathode Current – (figure 3)		180	500	nA

Notes : 1. ΔVref is defined as the difference between the maximum and minimum values obtained over the full temperature range.

ΔVref = Vref max - Vref min



2. The temperature coefficient is defined as the slopes (positive and negative) of the voltage vs temperature limits within which the reference voltage is quaranteed.



3. The dynamic Impedance is defined as $\left|Z_{KA}\right| = \frac{\Delta V_{KA}}{\Delta I_K}$

Figure 1 : Test Circuit for $V_{KA} = V_{ref}$

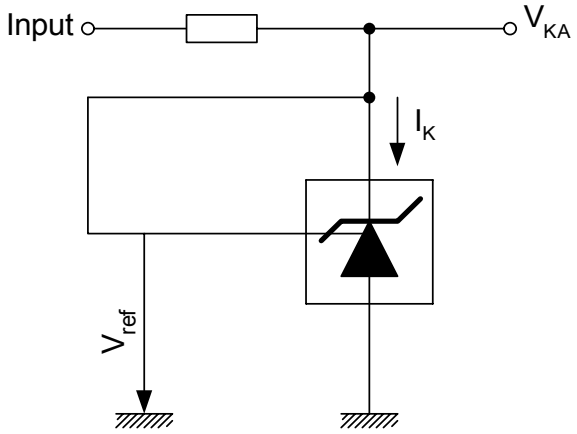
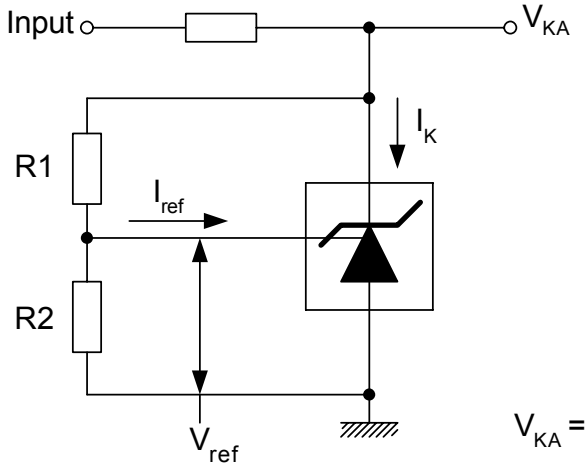
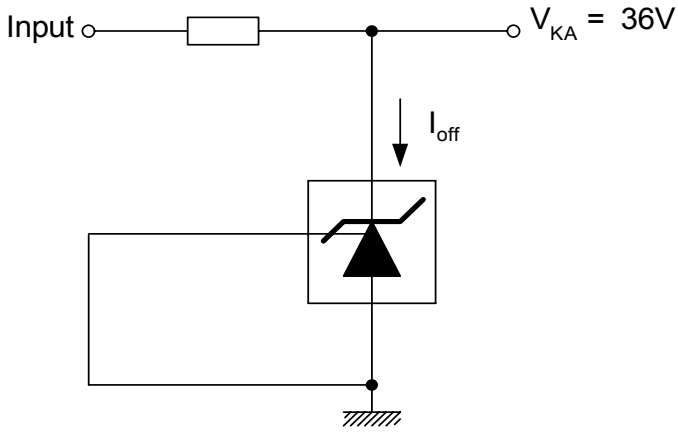


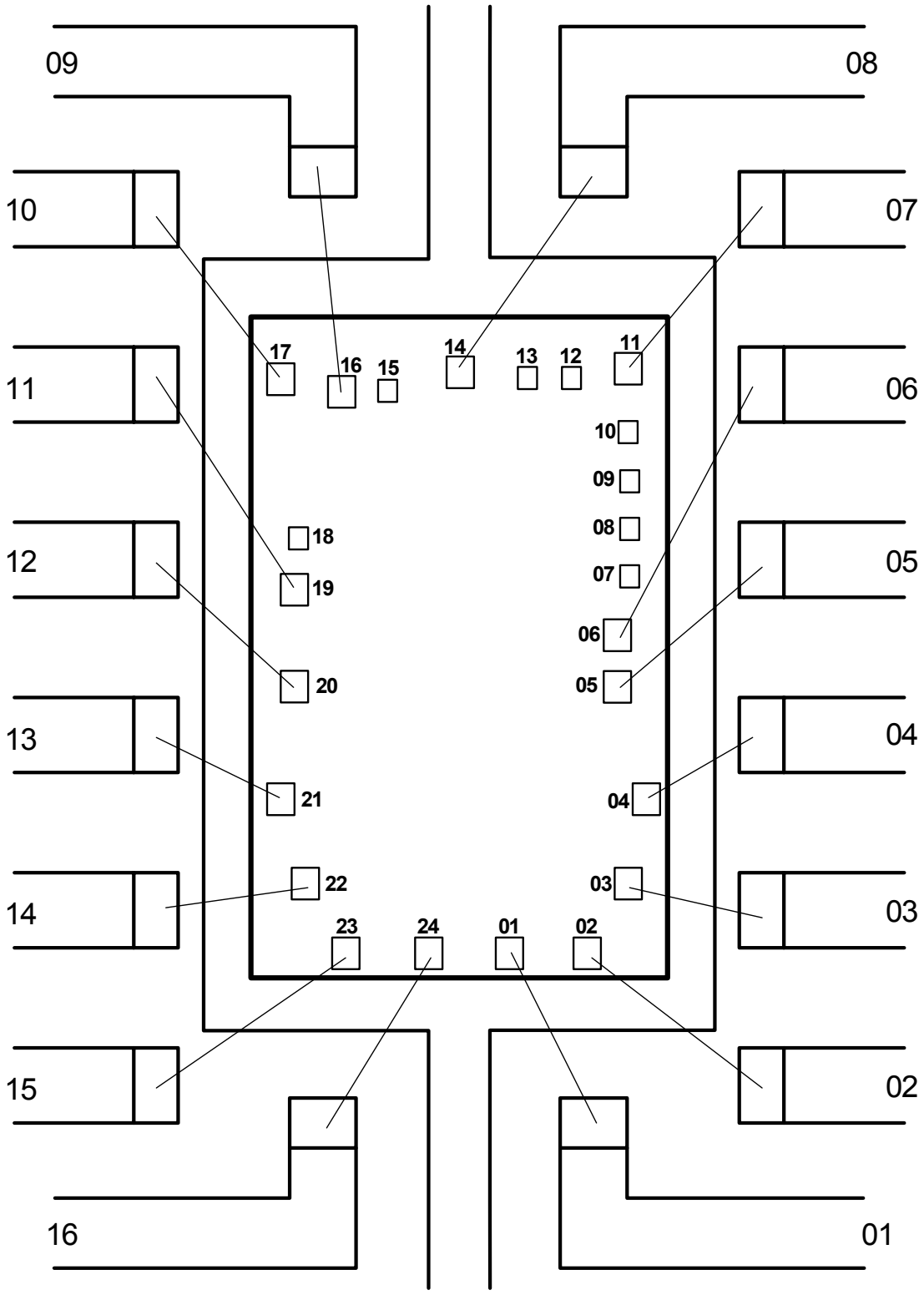
Figure 2 : Test Circuit for $V_{KA} > V_{ref}$



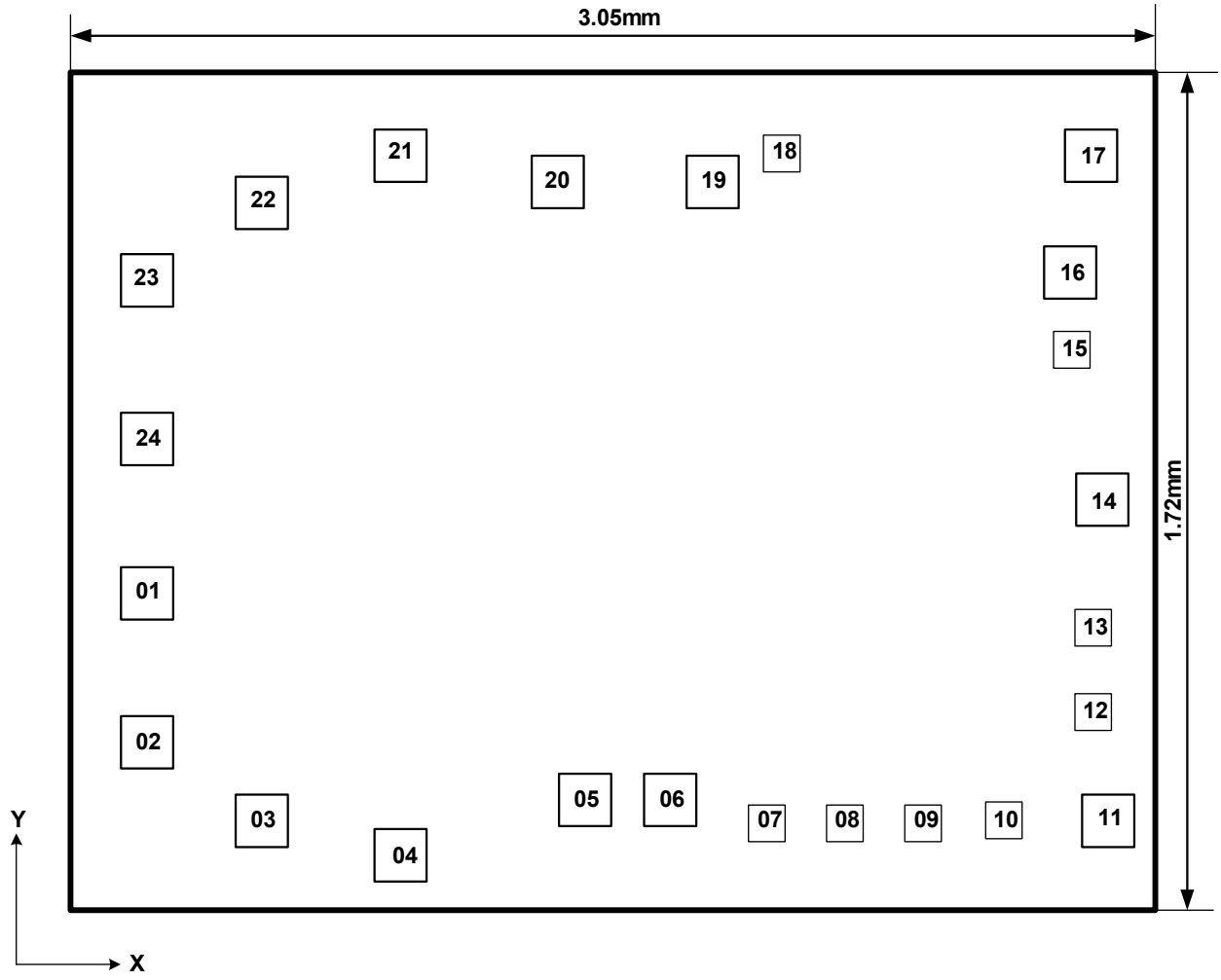
$$V_{KA} = V_{ref} (1 + R1/R2) + I_{ref}R1$$

Figure 3 : Test Circuit for I_{off}





Bonding diagram of FTSM102A



Pad size 01 - 06, 11, 14, 16, 17, 19 - 24 - have been bounded
Pad size 07 - 10, 12, 13, 15, 18 - have not been bounded

Pads location of FTSM102A

Die size Xr = 3.05mm, Yr = 1.72mm (pad size measured by layer “passivation”)
Coordinates of pads

No of pad (by layer “passivation”)	Coordinates left bottom, mkm		pad size, mkm
	X	Y	
01	144	454	100×100
02	119	129	100×100
03	407	129	100×100
04	567	129	100×100
05	736	161	100×100
06	1624	150	100×100
07	2125	121	70×70
08	2313	121	70×70
09	2501	121	70×70
10	2689	121	70×70
11	2819	2819	100×100
12	2835	2835	70×70
13	2835	2835	70×70
14	2818	2818	100×100
15	2797	2797	70×70
16	2778	2778	100×100
17	2807	2807	100×100
18	1798	1798	70×70
19	1624	1624	100×100
20	736	736	100×100
21	567	567	100×100
22	407	407	100×100
23	119	119	100×100
24	144	144	100×100

No of pad	Pin	Function
01	01	Output 1
02	02	Inverting input 1
03	03	Non-inverting input 1
04	04	Vcc^+
05	05	Non-inverting input 2
06	06	Inverting input 2
11	07	Output 2
14	08	Vref
16	09	Cathode
17	10	Output 3
19	11	Inverting input 3
20	12	Non-inverting input 3
21	13	Vcc^-
22	14	Non-inverting input 4
23	15	Inverting input 4
24	16	Output 4