512Kx32 SRAM 3.3V MULTICHIP PACKAGE

FEATURES

- Access Times of 15, 17, 20ns
- Low Voltage Operation
- Packaging
  - 66-pin, PGA Type, 1.075 inch square, Hermetic Ceramic HIP (Package 400)
  - 8 lead, 22.4mm (0.880 inch) CQFP, (G2U), 3.56mm (0.140"), (Package 510)
- Organized as 512Kx32; User Configurable as 2x512Kx16 or 4x512Kx8
- Commercial, Industrial and Military Temperature Ranges
- Low Voltage Operation:
  - 3.3V ± 10% Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Fully Static Operation:
  - No clock or refresh required.
- Three State Output.
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  - WS512K32V-XG2UX - 8 grams typical
    WS512K32NV-XH1X - 13 grams typical

* This product is subject to change without notice.

PIN CONFIGURATION FOR WS512K32NV-XH1X

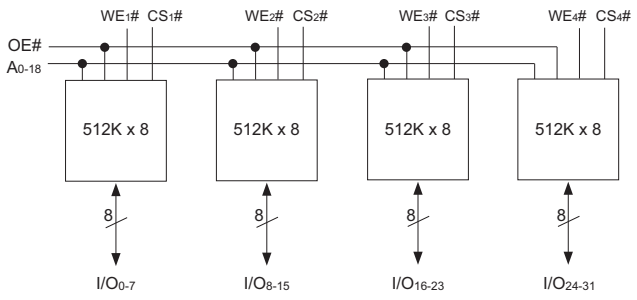
Top View

1	12	23		34	45	56
I/O_8	WE_2#	I/O_{15}		I/O_{24}	V_{CC}	I/O_{31}
I/O_9	CS_2#	I/O_{14}		I/O_{25}	CS_4#	I/O_{30}
I/O_{10}	GND	I/O_{13}		I/O_{26}	WE_4#	I/O_{29}
A_{13}	I/O_{11}	I/O_{12}		A_6	I/O_{27}	I/O_{28}
A_{14}	A_{10}	OE#		A_7	A_3	A_0
A_{15}	A_{11}	A_{18}		NC	A_4	A_1
A_{16}	A_{12}	WE_1#		A_8	A_5	A_2
A_{17}	V_{CC}	I/O_7		A_9	WE_3#	I/O_{23}
I/O_0	CS_1#	I/O_6		I/O_{16}	CS_3#	I/O_{22}
I/O_1	NC	I/O_5		I/O_{17}	GND	I/O_{21}
I/O_2	I/O_3	I/O_4		I/O_{18}	I/O_{19}	I/O_{20}
11	22	33		44	55	66

Pin Description

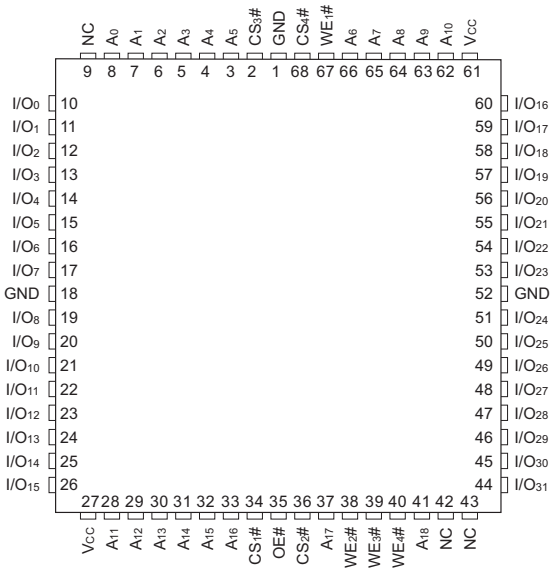
I/O_{0-31}	Data Inputs/Outputs
A_{0-18}	Address Inputs
WE_{1-4}#	Write Enables
CS_{1-4}#	Chip Selects
OE#	Output Enable
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

Block Diagram



PIN CONFIGURATION FOR WS512K32V-XG2UX

Top View



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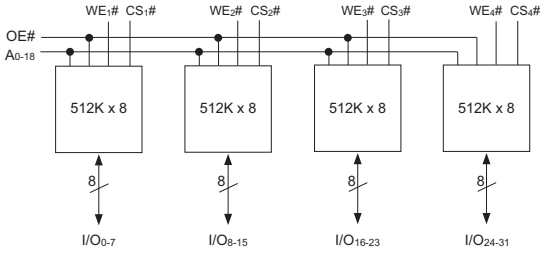


ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	4.6	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	4.6	V

TRUTH TABLE

CS	OE	WE	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C_{OE}	V_{IN} = 0V, f = 1.0 MHz	50	pF
WE_{1-4}# capacitance	C_{WE}	V_{IN} = 0V, f = 1.0 MHz		pF
HIP (PGA)			20	
CQFP G2U			20	
CS_{1-4}# capacitance	C_{CS}	V_{IN} = 0V, f = 1.0 MHz	20	pF
Data# I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

V_{CC} = 3.3V ± 0.3V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	CS# = V_{IH}, OE# = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current	I_{CC} x 32	CS# = V_{IL}, OE# = V_{IH}, f = 5MHz, V_{CC} = 3.6		400	mA
Standby Current	I_{SB}	CS# = V_{IH}, OE# = V_{IH}, f = 5MHz, V_{CC} = 3.6		200	mA
Output Low Voltage	V_{OL}	I_{OL} = 4.0mA		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V.
Contact factory for low power option.

AC CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter Read Cycle	Symbol	-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		17		20		ns
Address Access Time	t_{AA}		15		17		20	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns
Chip Select Access Time	t_{ACS}		15		17		20	ns
Output Enable to Output Valid	t_{OE}		8		8		10	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	1		1		1		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		8		8		10	ns
Output Disable to Output in High Z	t_{OHZ}[1]		8		8		10	ns

1. This parameter is guaranteed by design but not tested.

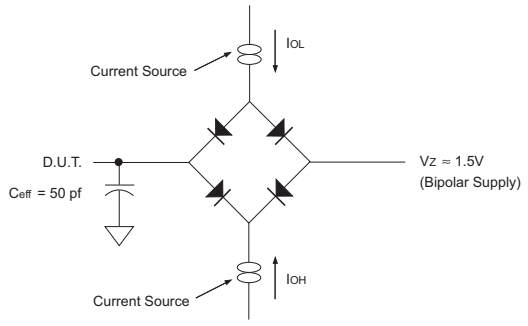
AC CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter Write Cycle	Symbol	-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		17		20		ns
Chip Select to End of Write	t_{CW}	12		12		14		ns
Address Valid to End of Write	t_{AW}	12		12		14		ns
Data Valid to End of Write	t_{DW}	9		9		10		ns
Write Pulse Width	t_{WP}	12		14		14		ns
Address Setup Time	t_{AS}	0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		ns
Output Active from End of Write	t_{OW}[1]	2		3		3		ns
Write Enable to Output in High Z	t_{WHZ}[1]		8		8		9	ns
Data Hold Time	t_{DH}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT

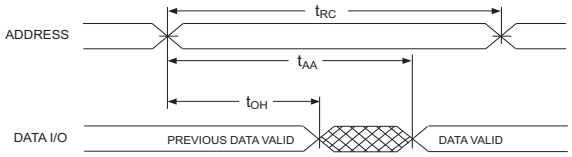


AC Test Conditions

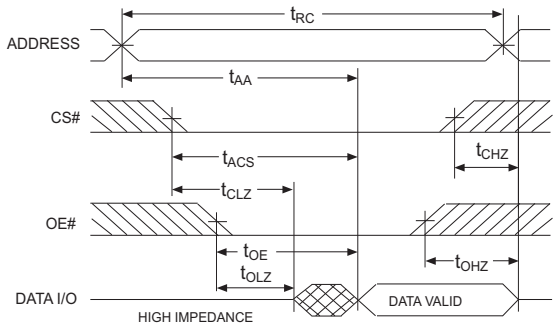
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

TIMING WAVEFORM – READ CYCLE

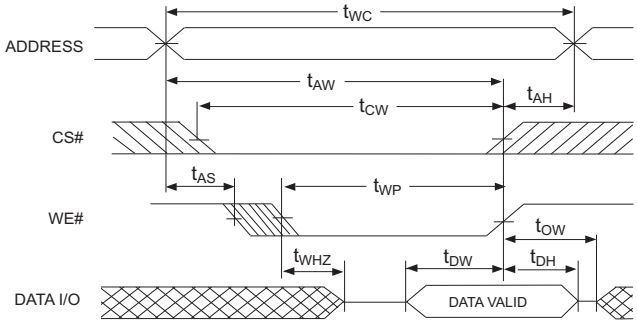


READ CYCLE 1 (CS# = OE# = V_{IL}, WE# = V_{IH})



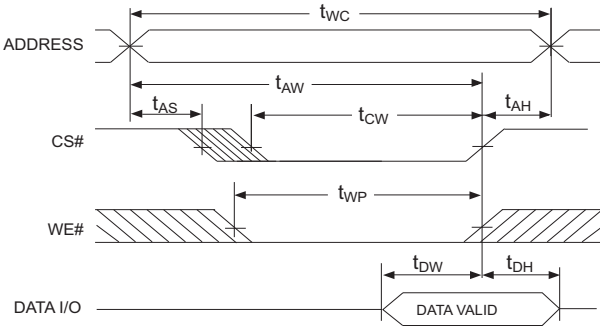
READ CYCLE 2 (WE# = V_{IH})

WRITE CYCLE – WE# CONTROLLED



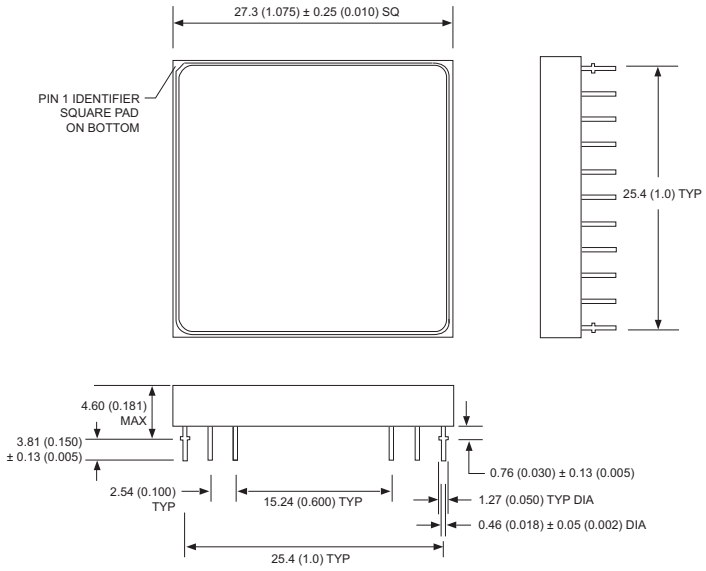
WRITE CYCLE 1, WE# CONTROLLED

WRITE CYCLE – CS# CONTROLLED



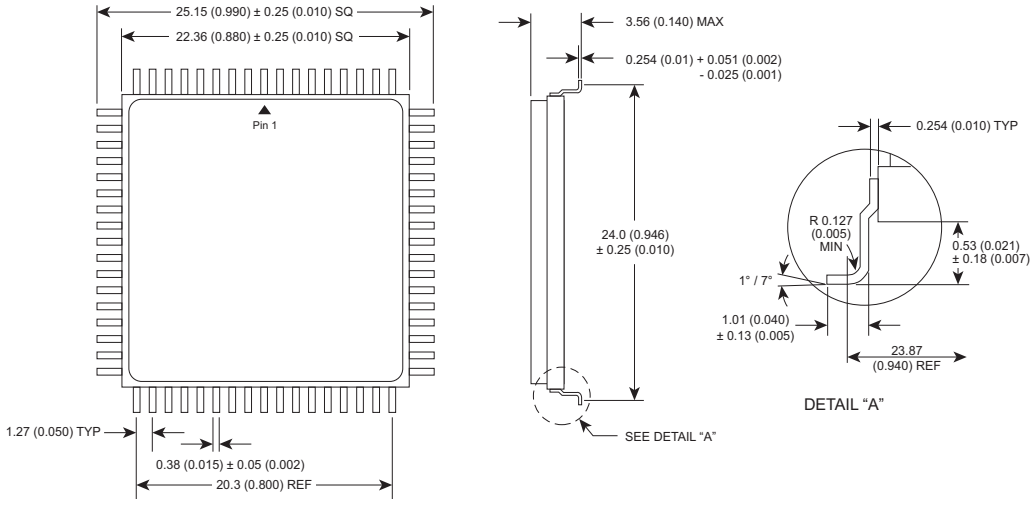
WRITE CYCLE 2, CS# CONTROLLED

PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 510: 68 LEAD, LOW PROFILE CERAMIC QUAD FLAT PACK, CQFP (G2U)



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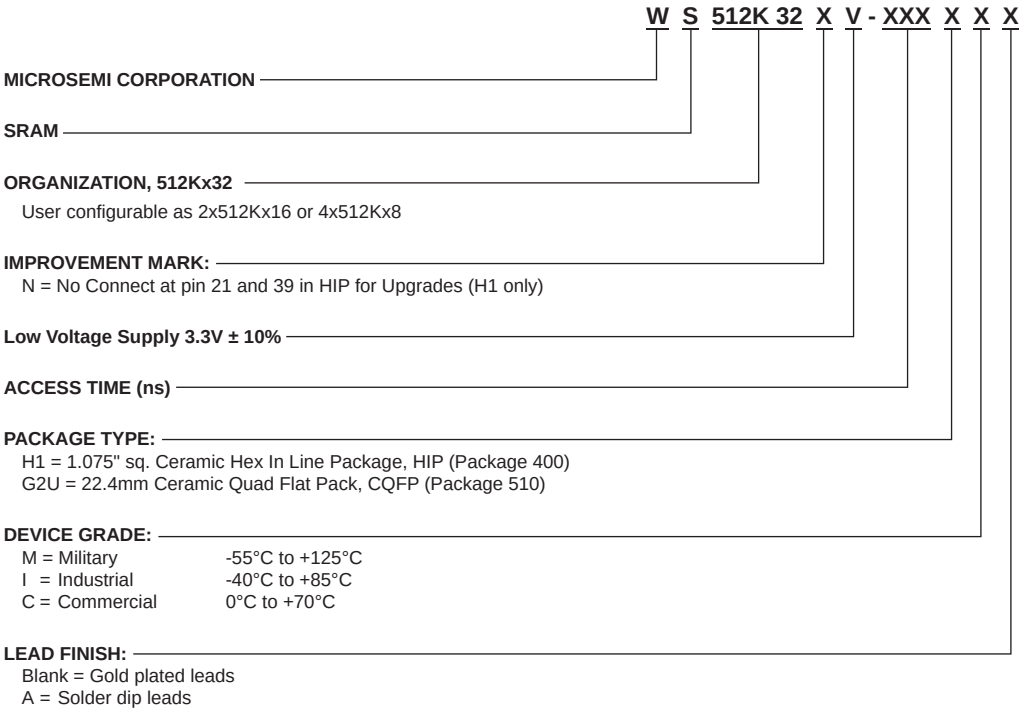
ORDERING INFORMATION



Document Title

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Revision History

Rev #	History	Release Date	Status
Rev 14	Changes (Pg. 6) (ECN 9936) 14.1 Add document Revision History page 14.2 Update package dimensions	April 2016	Final